

FIG. 1

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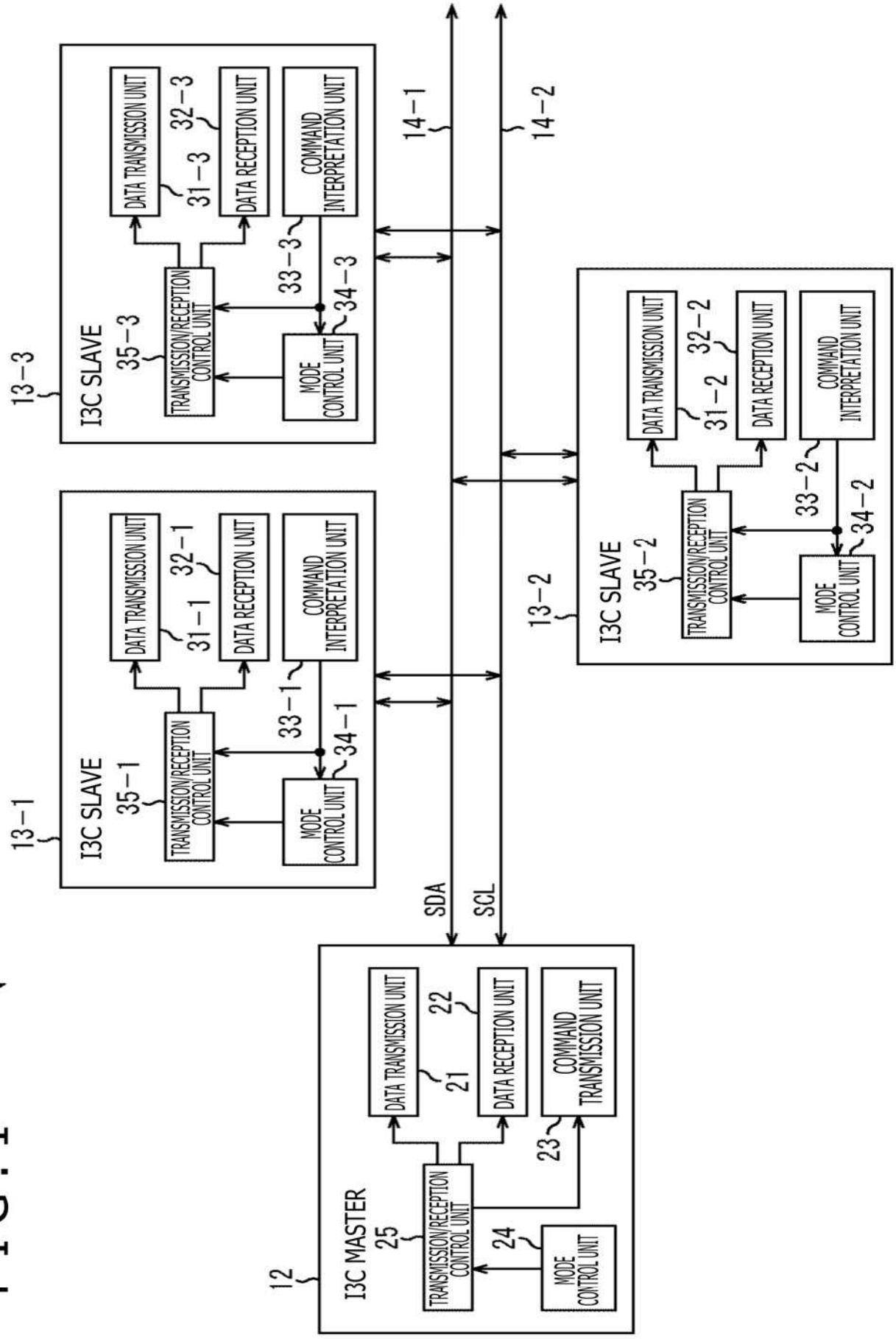


FIG. 2

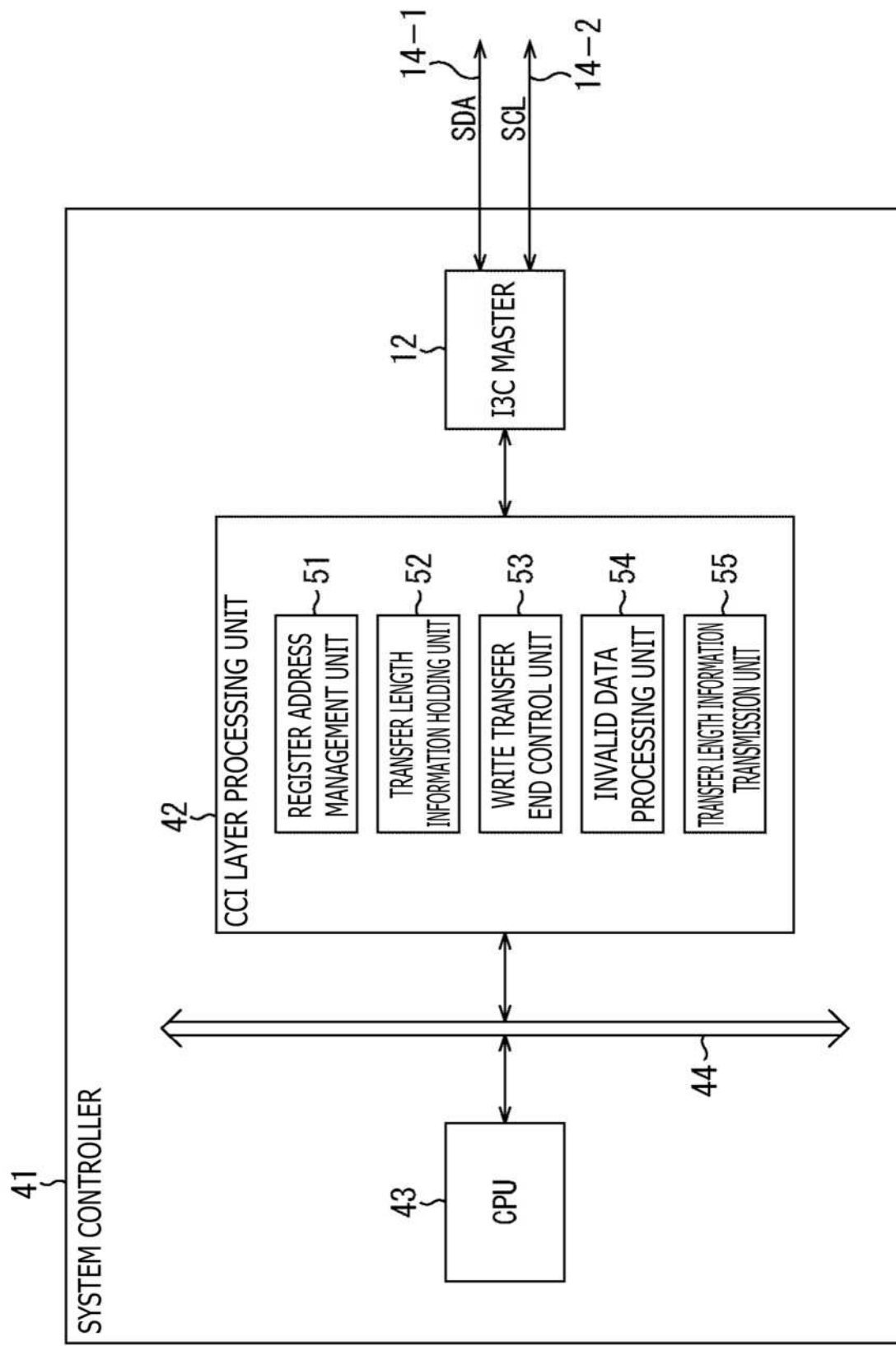


FIG. 3

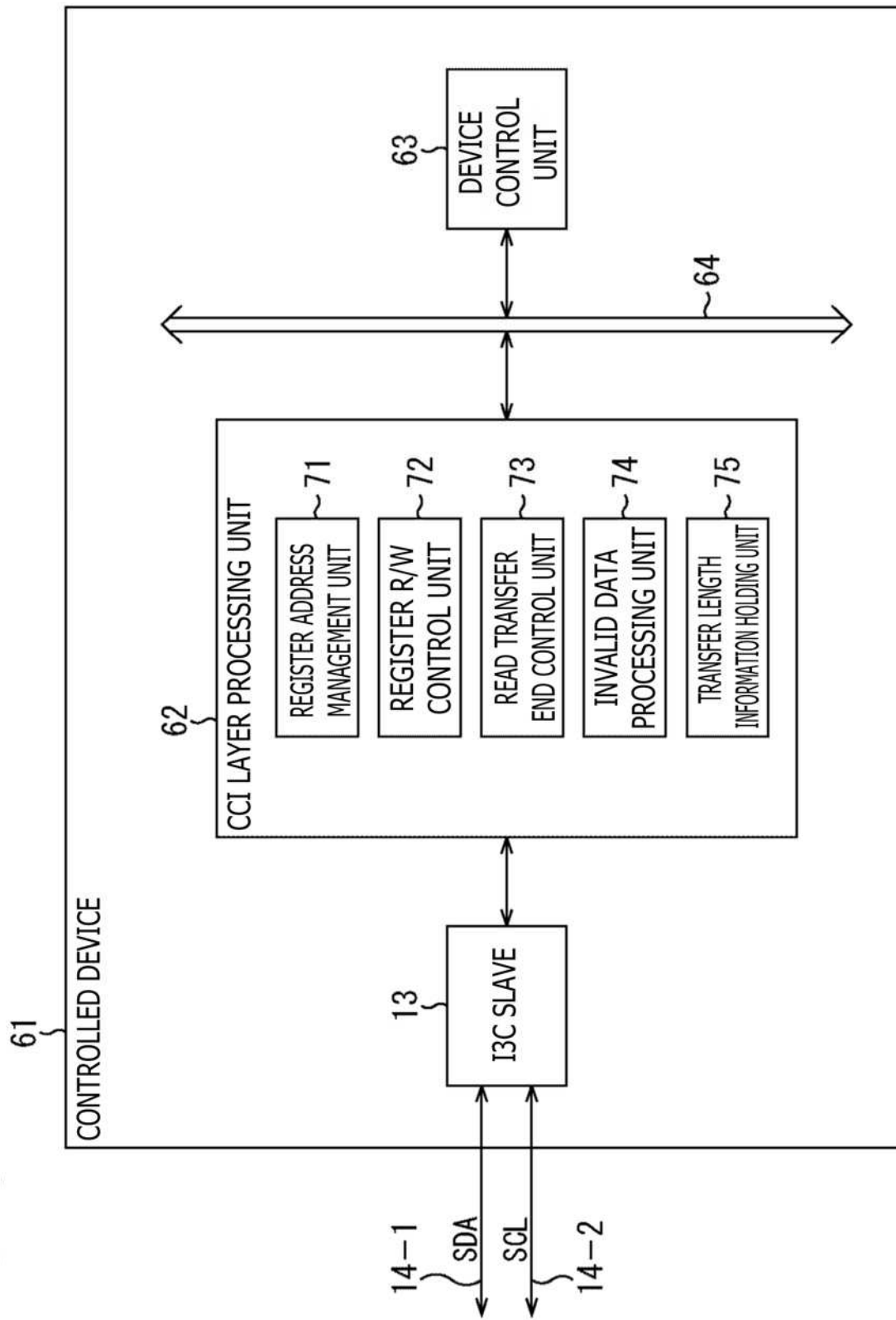


FIG. 4

DDR Sequential Read/Write from random location

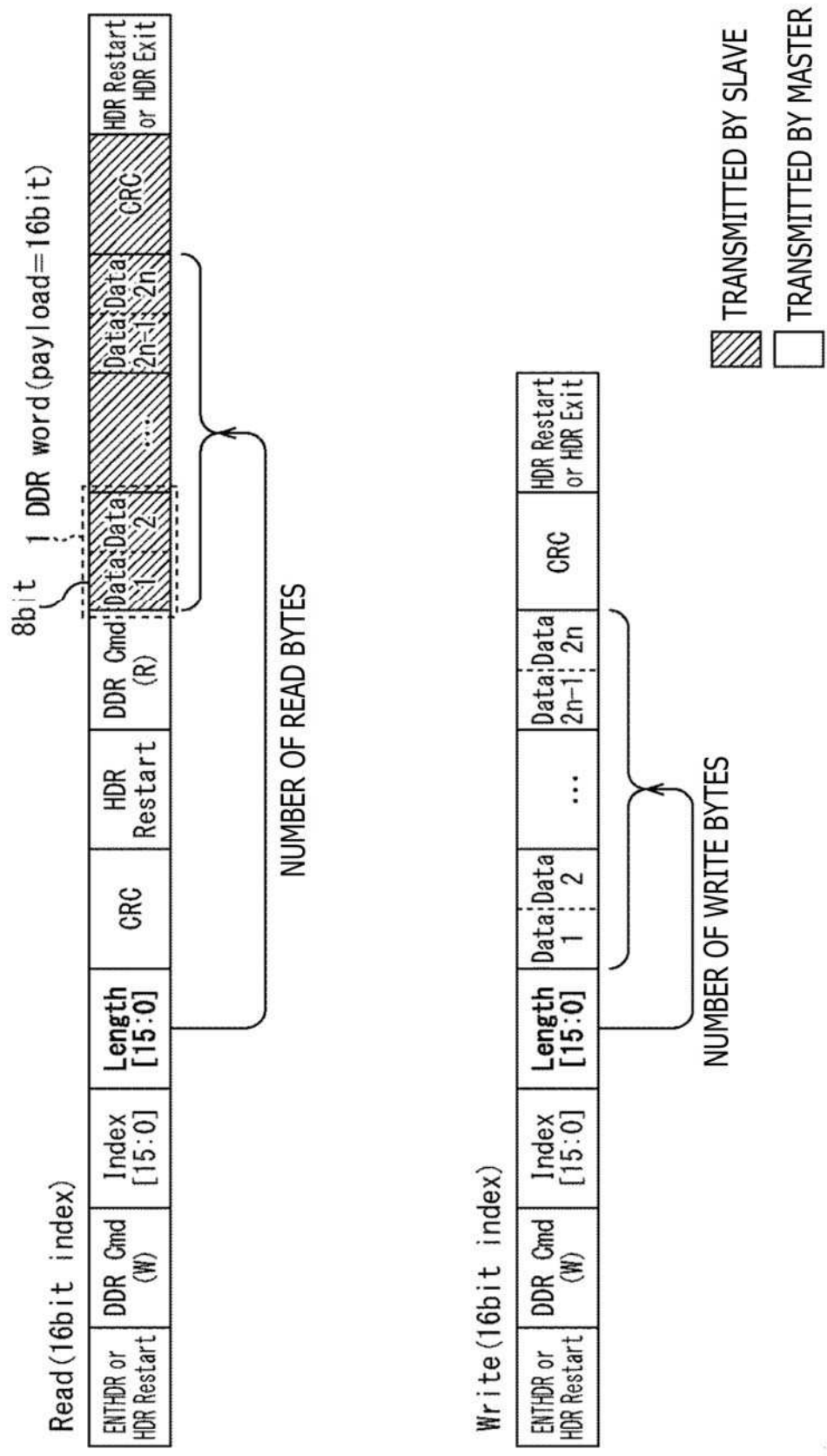


FIG. 5

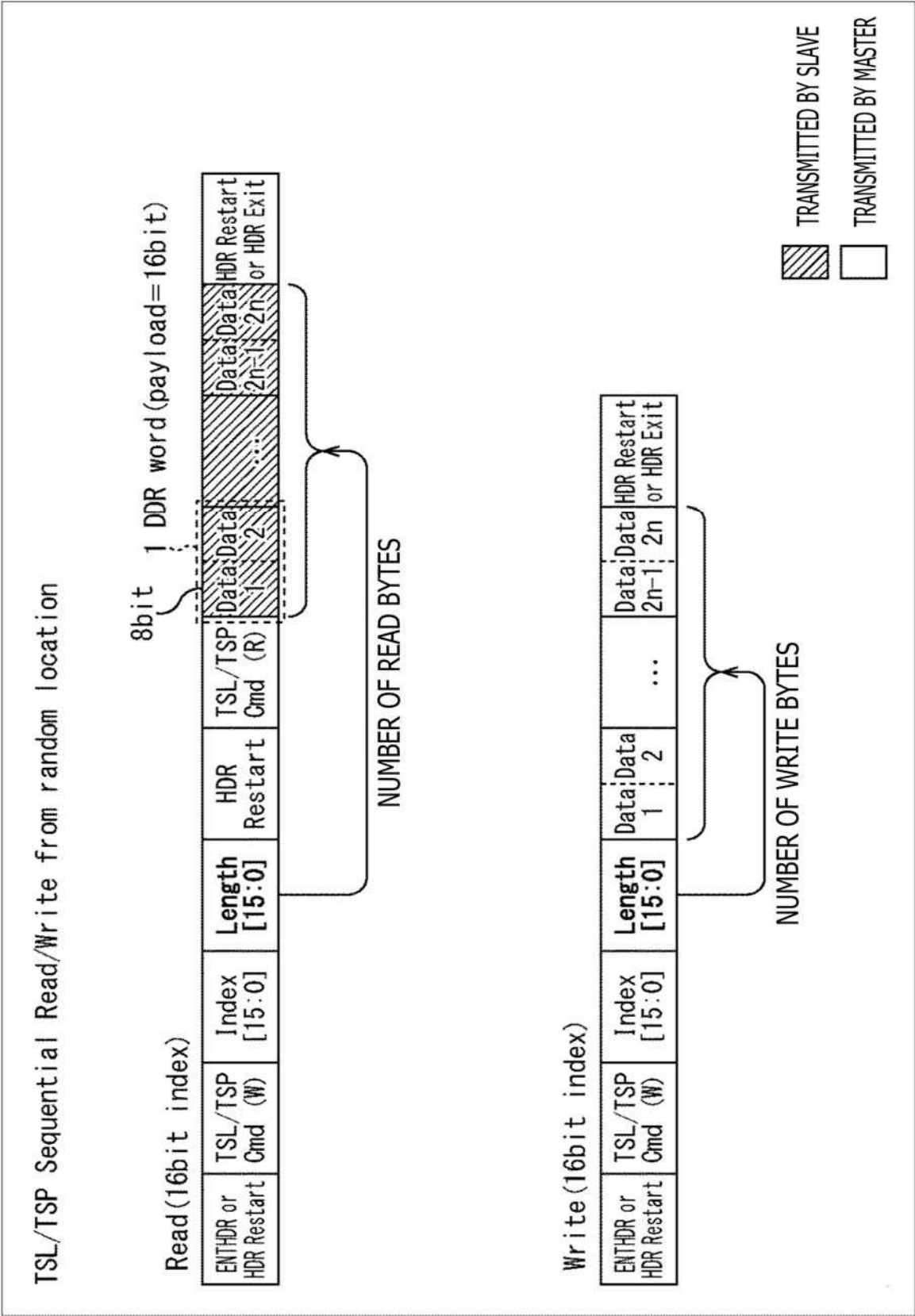


FIG. 6

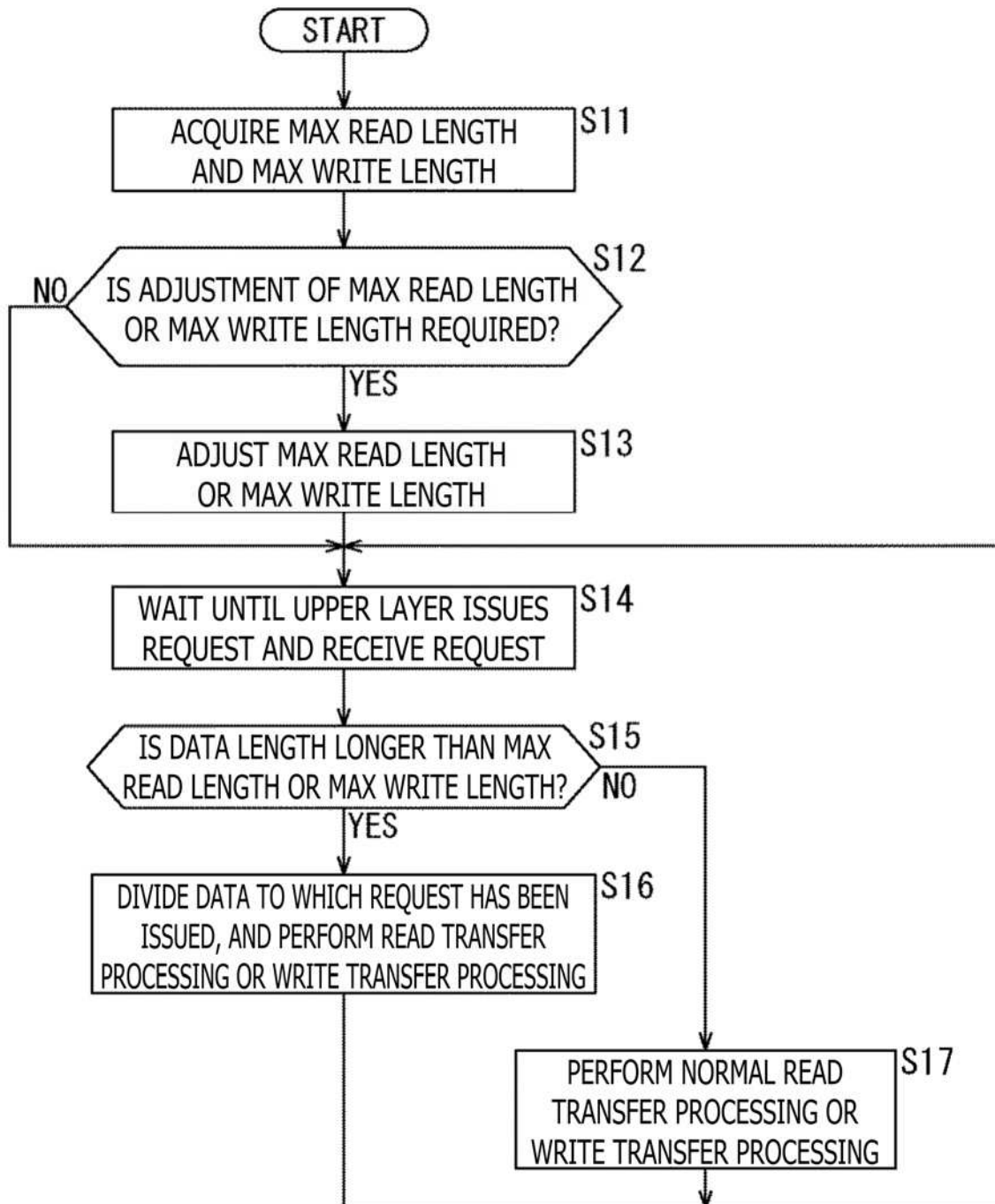


FIG. 7

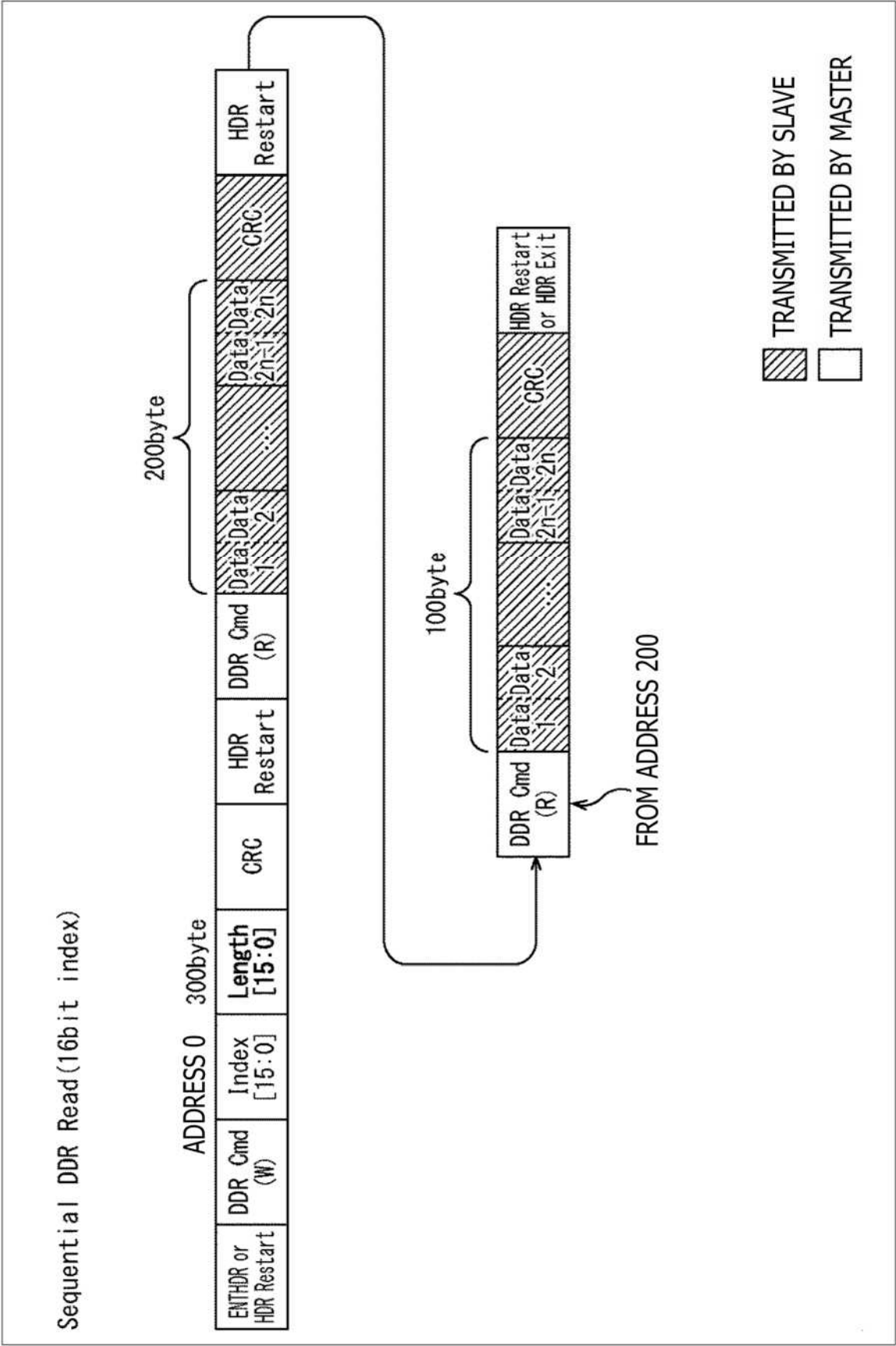


FIG. 8

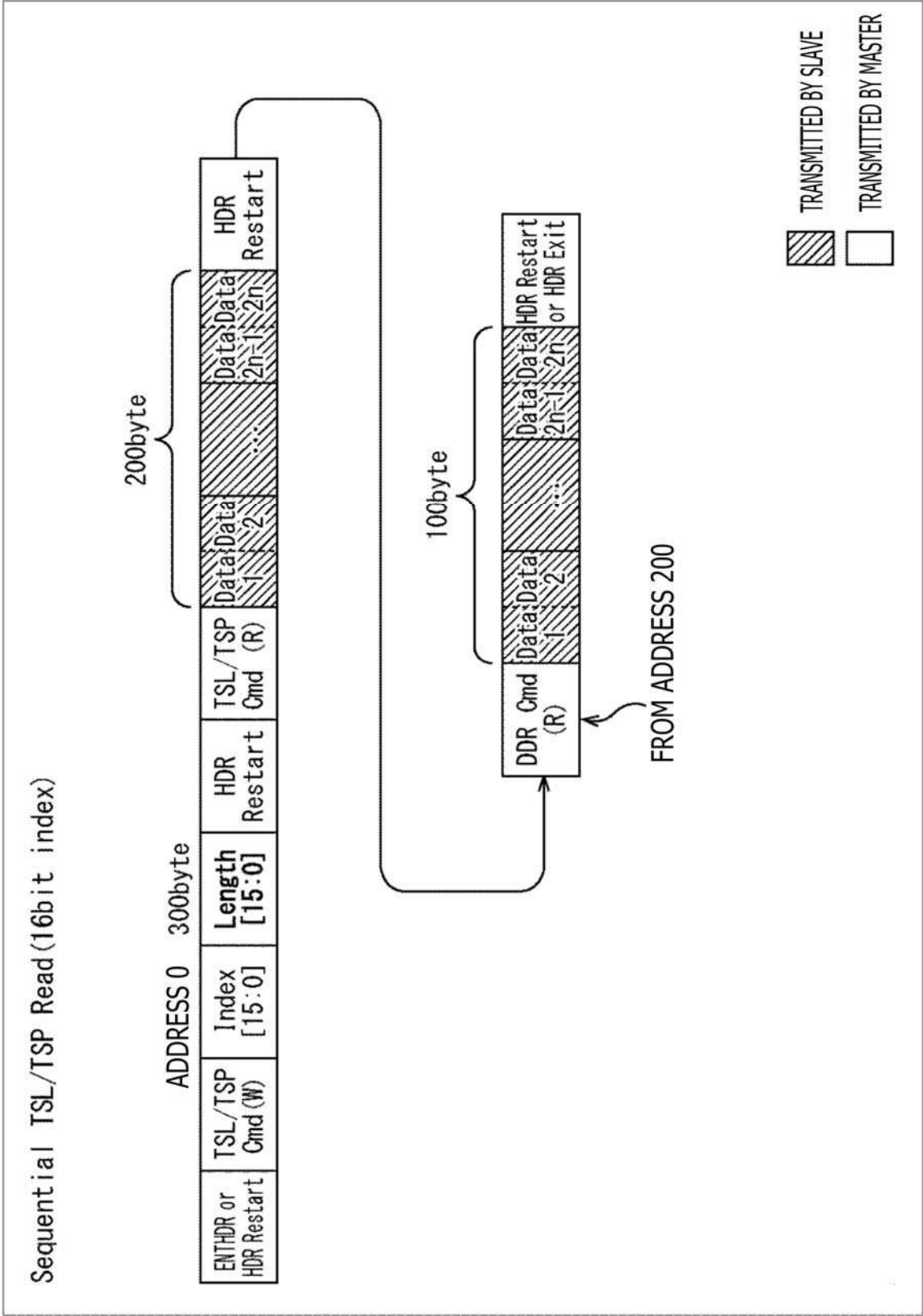


FIG. 9

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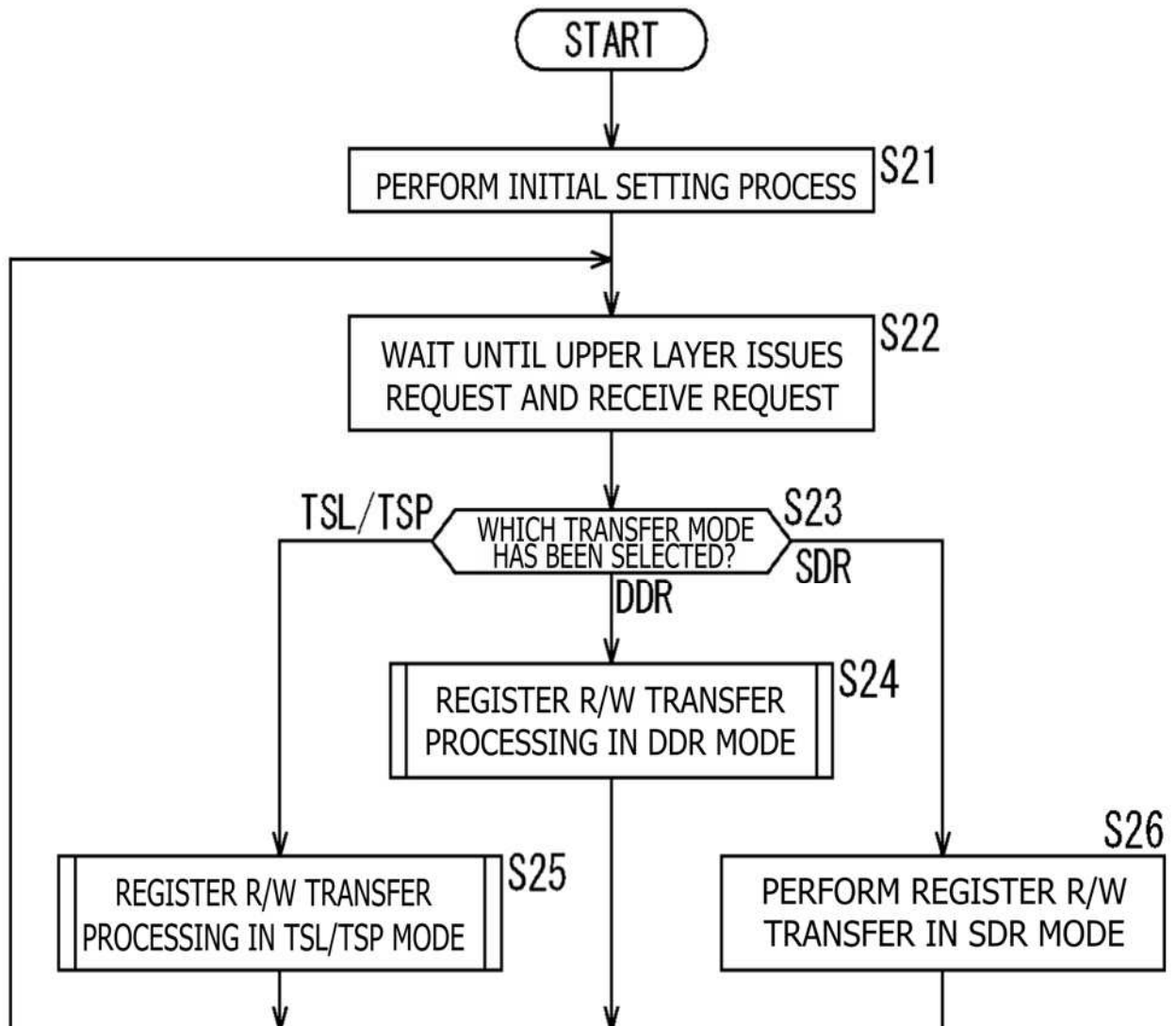
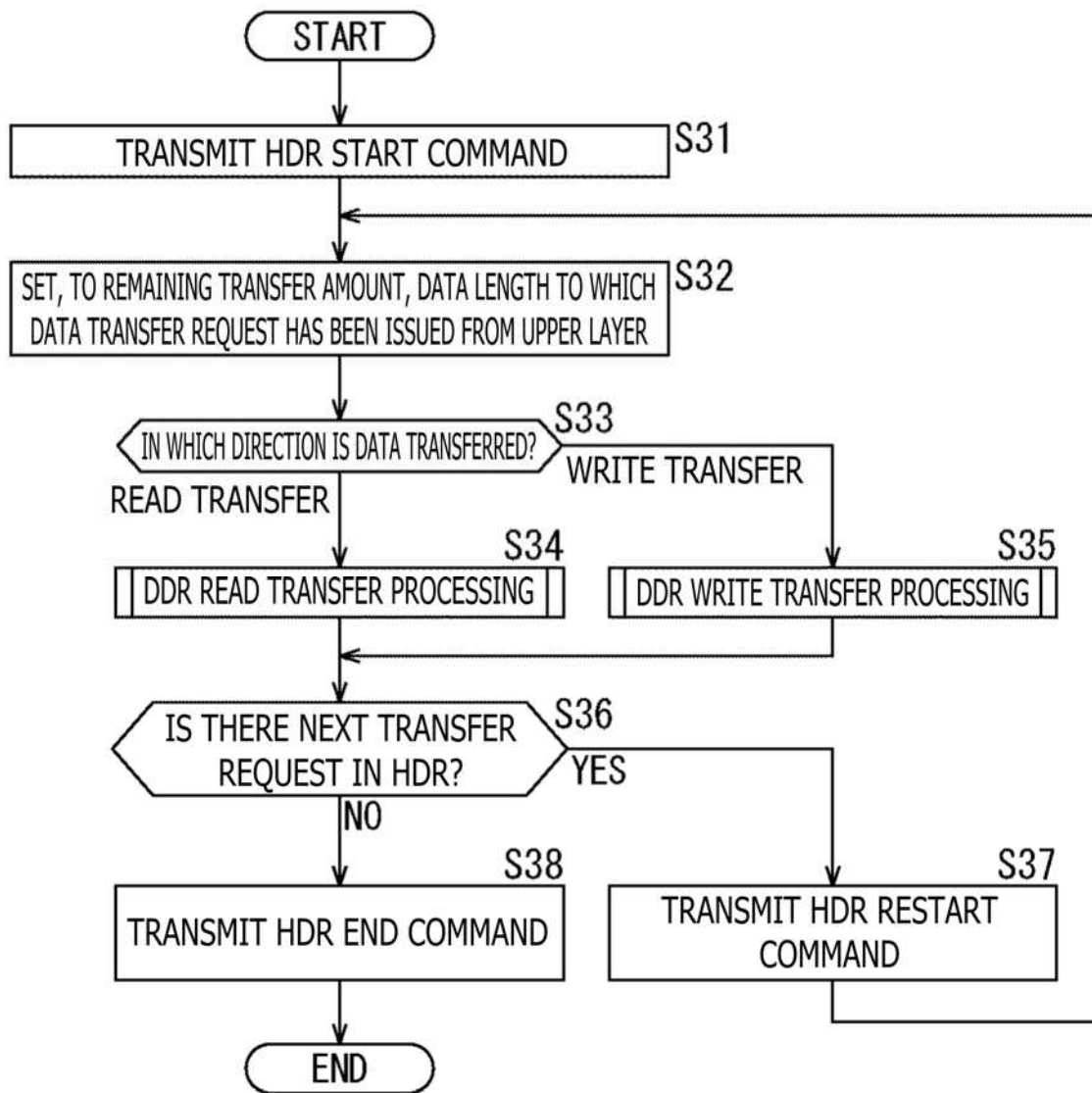


FIG. 10



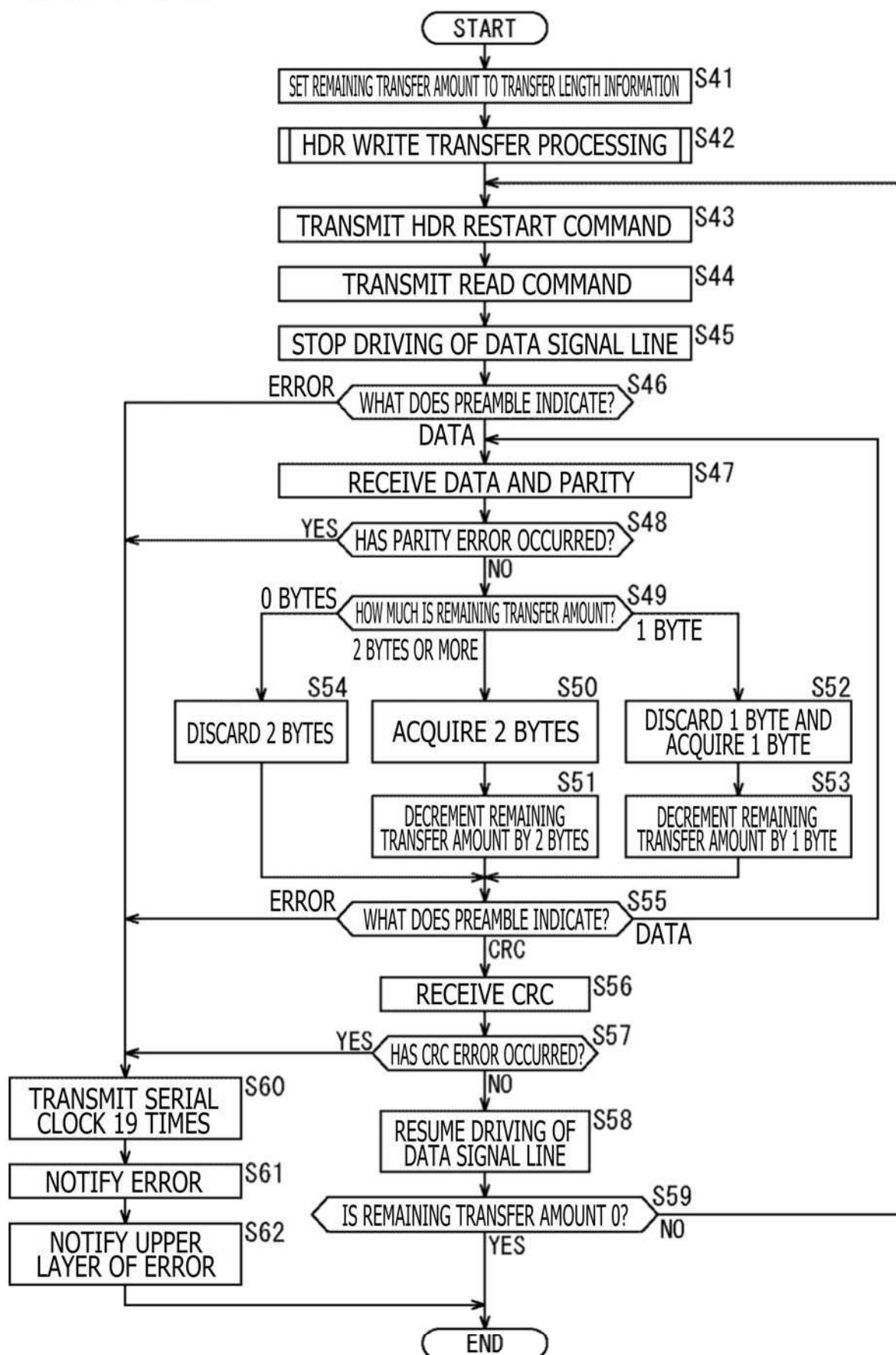


FIG. 12

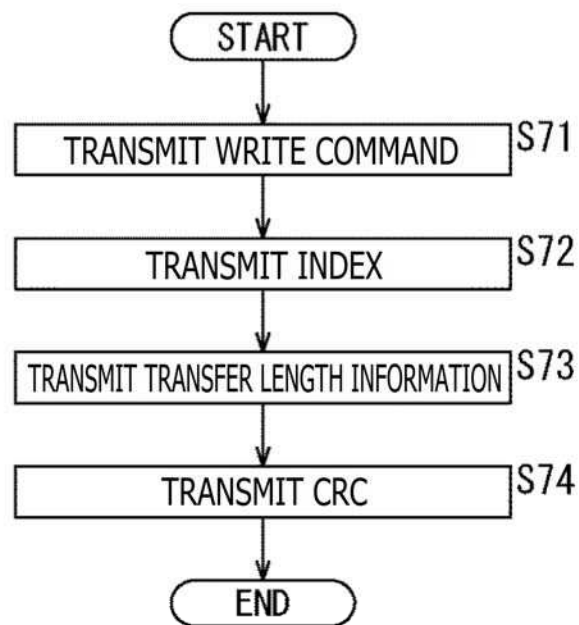


FIG. 13

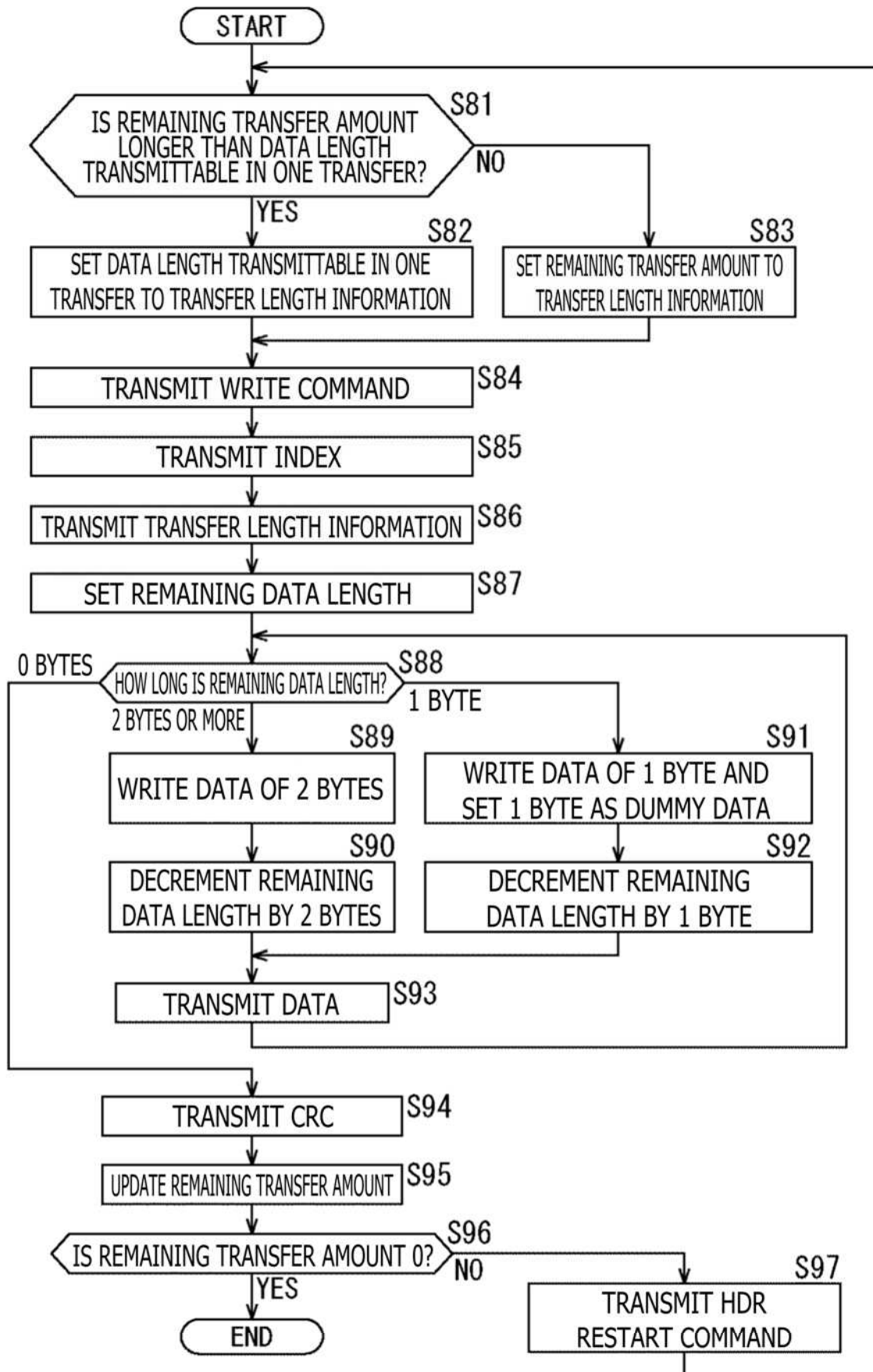


FIG. 14

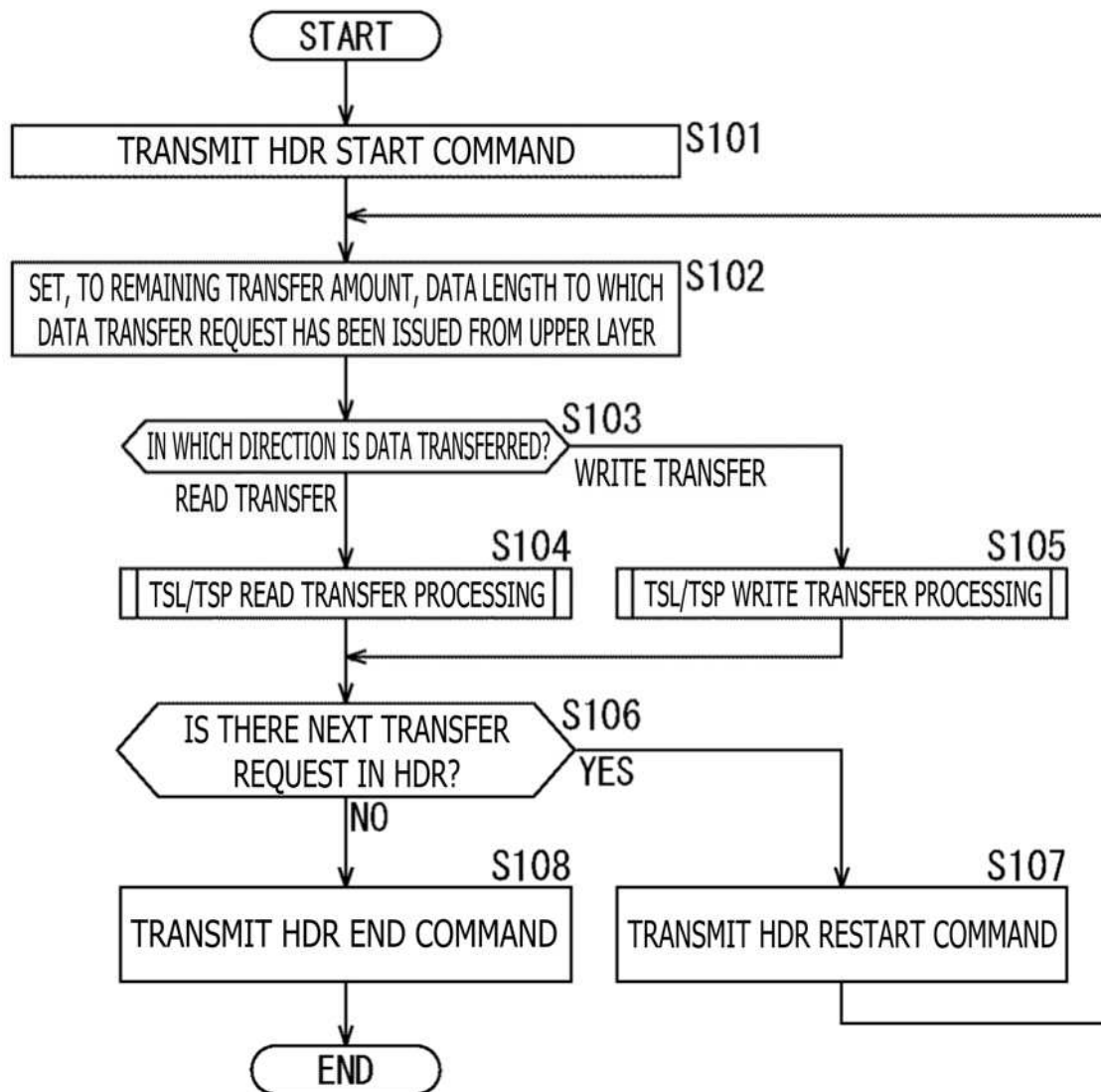


FIG. 15

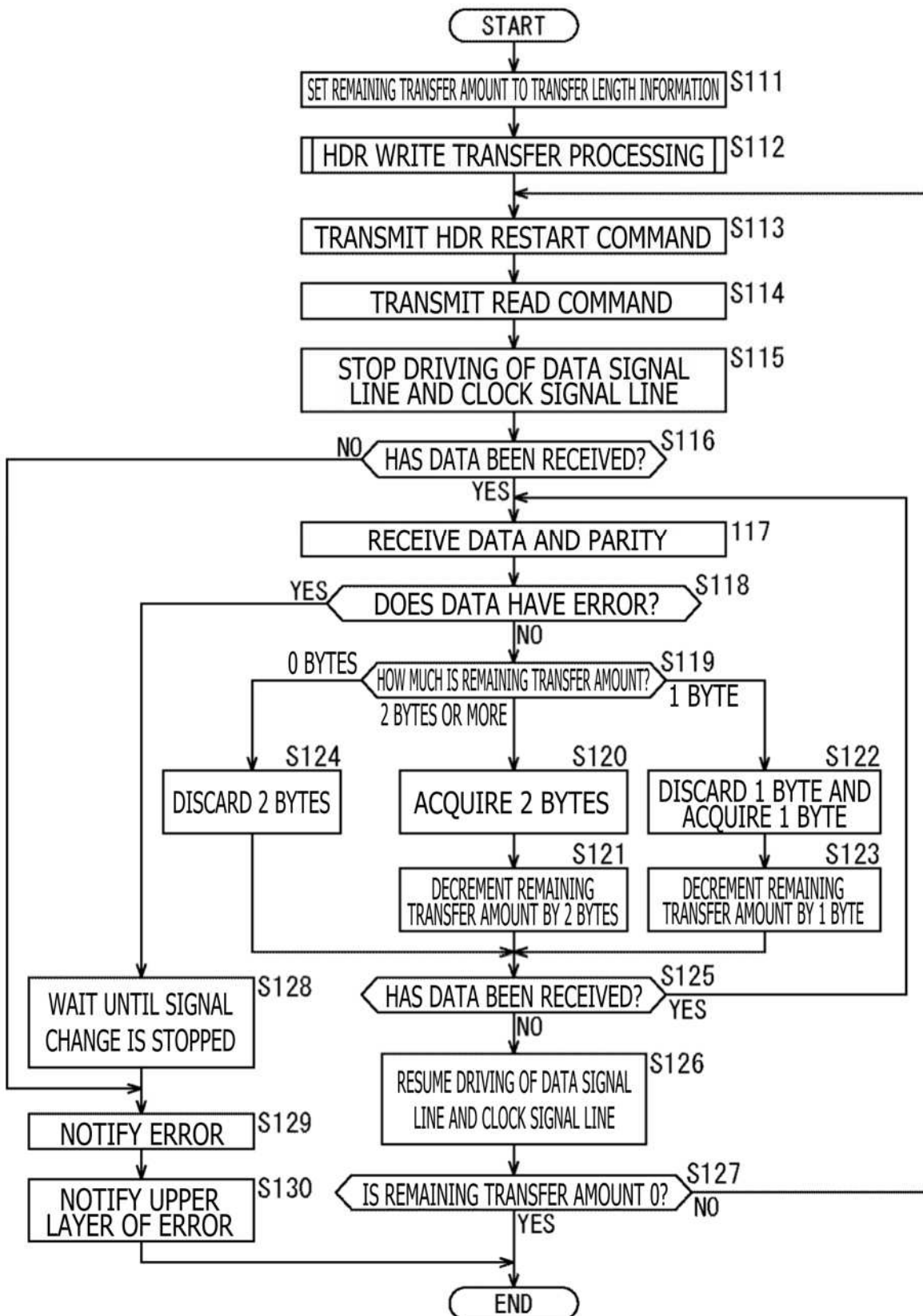


FIG. 16

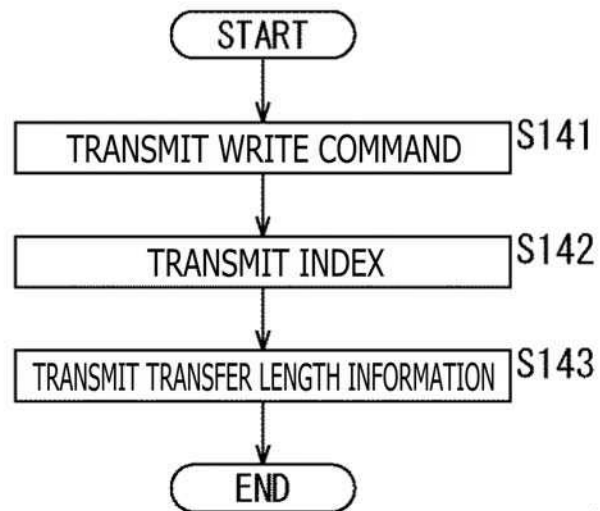


FIG. 17

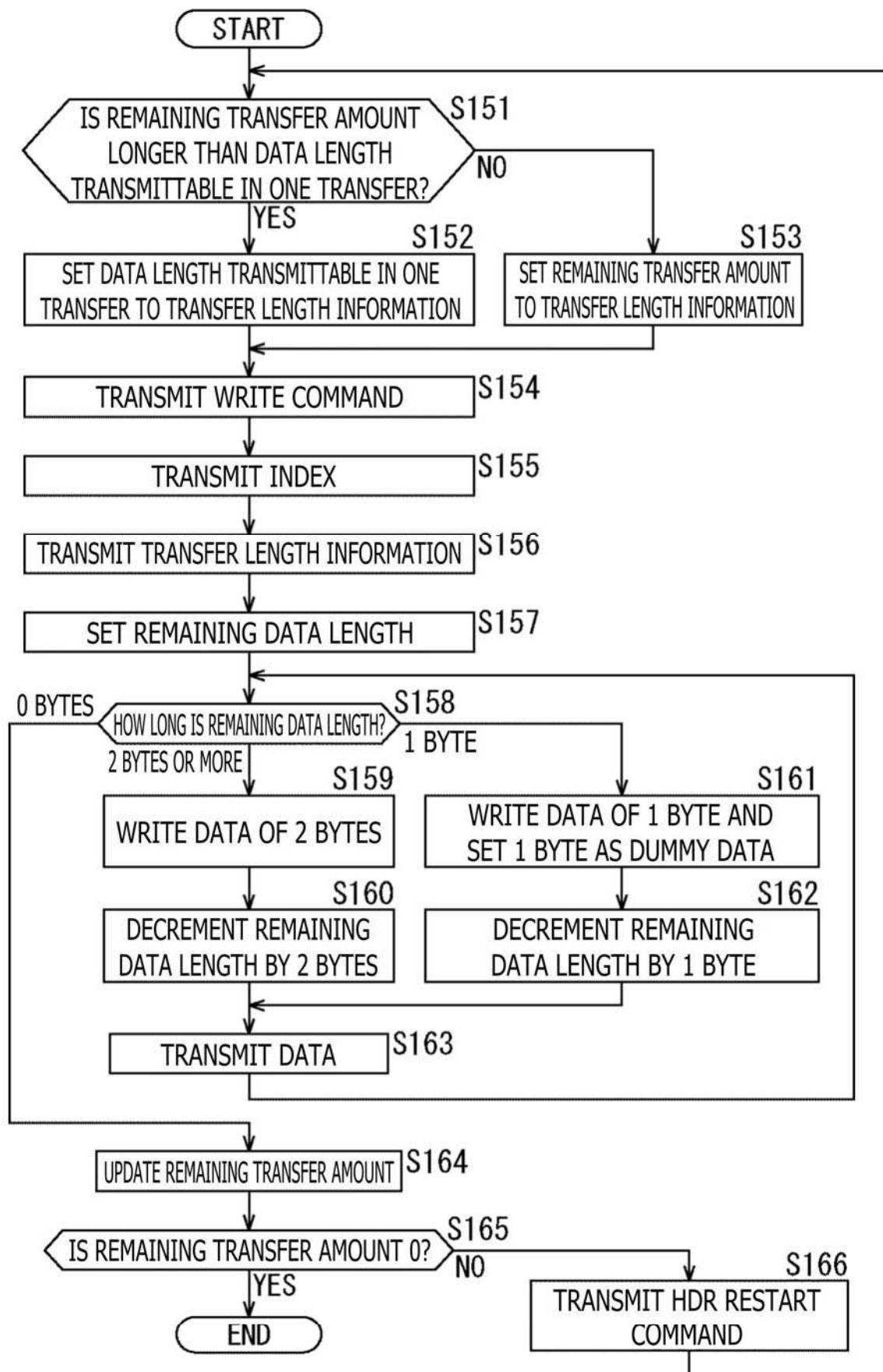


FIG. 18

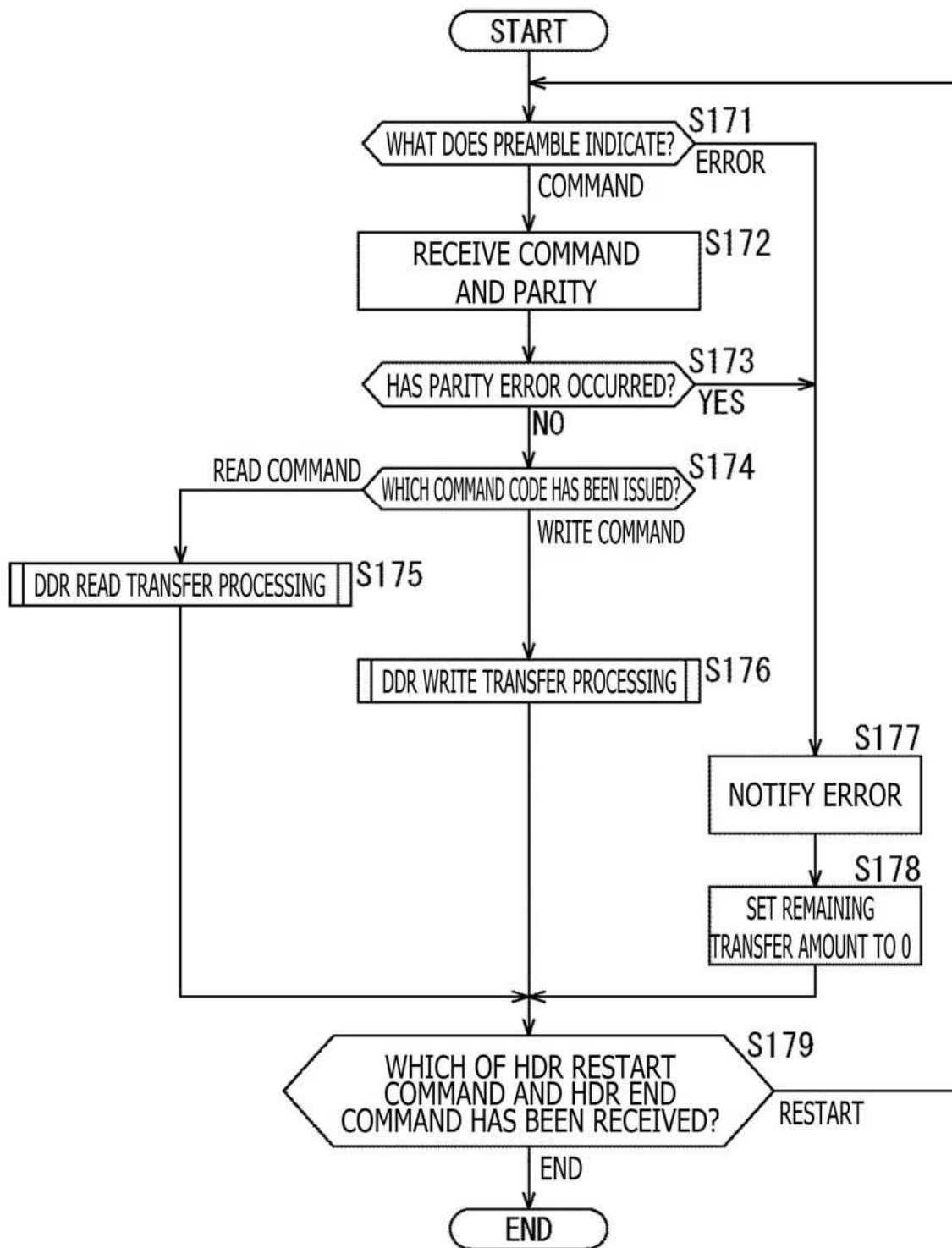


FIG. 19

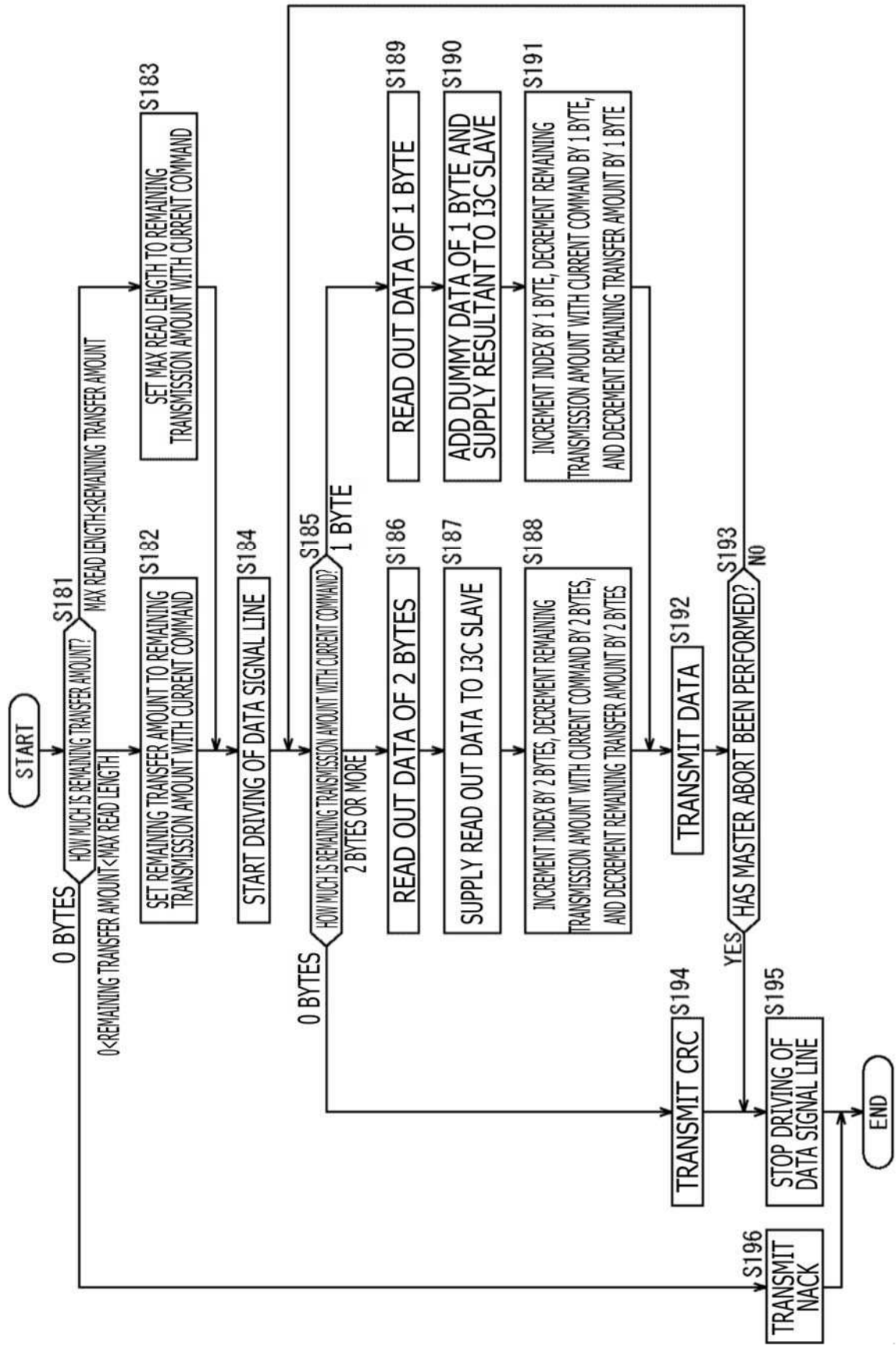


FIG. 20

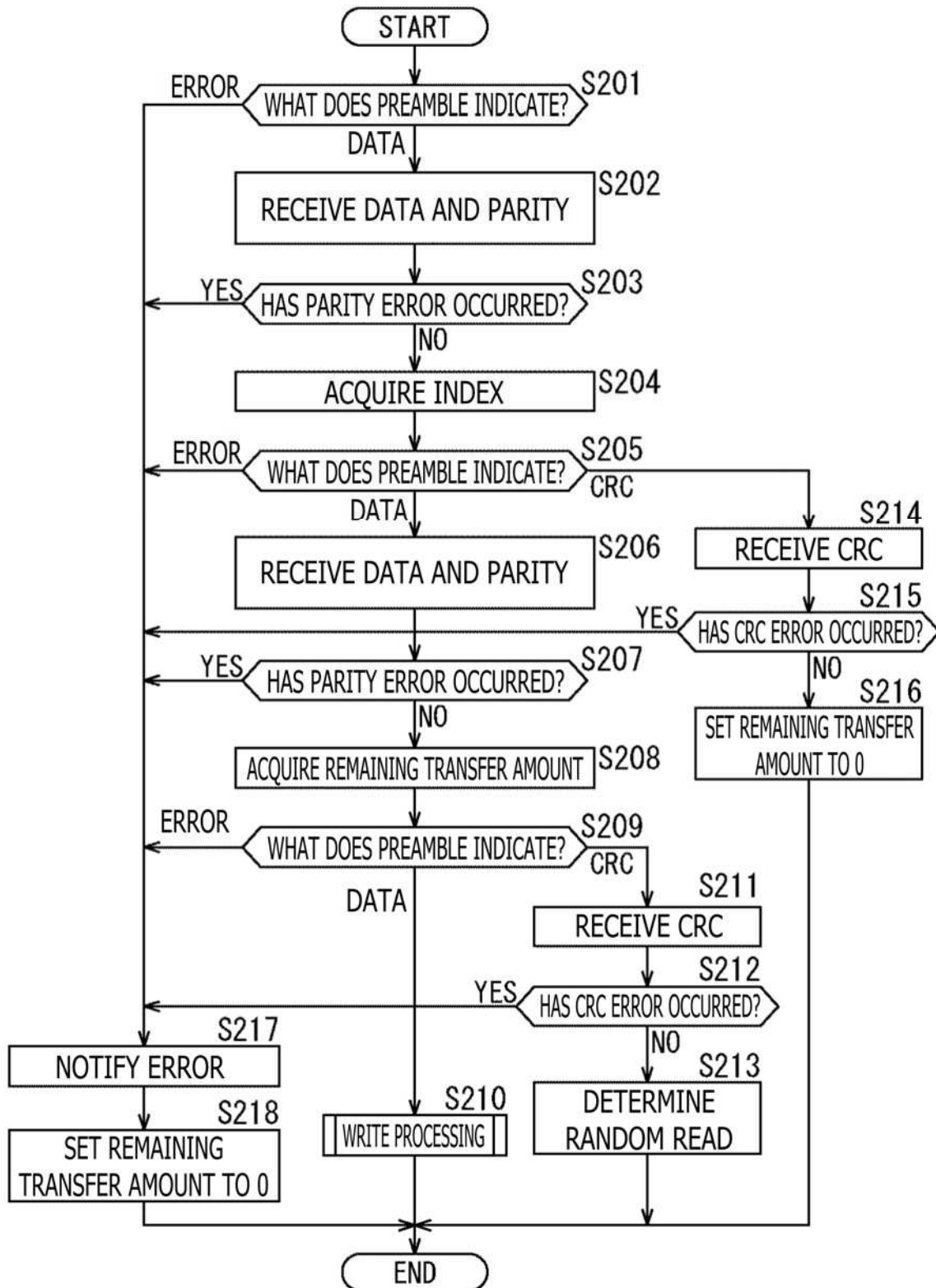


FIG. 21

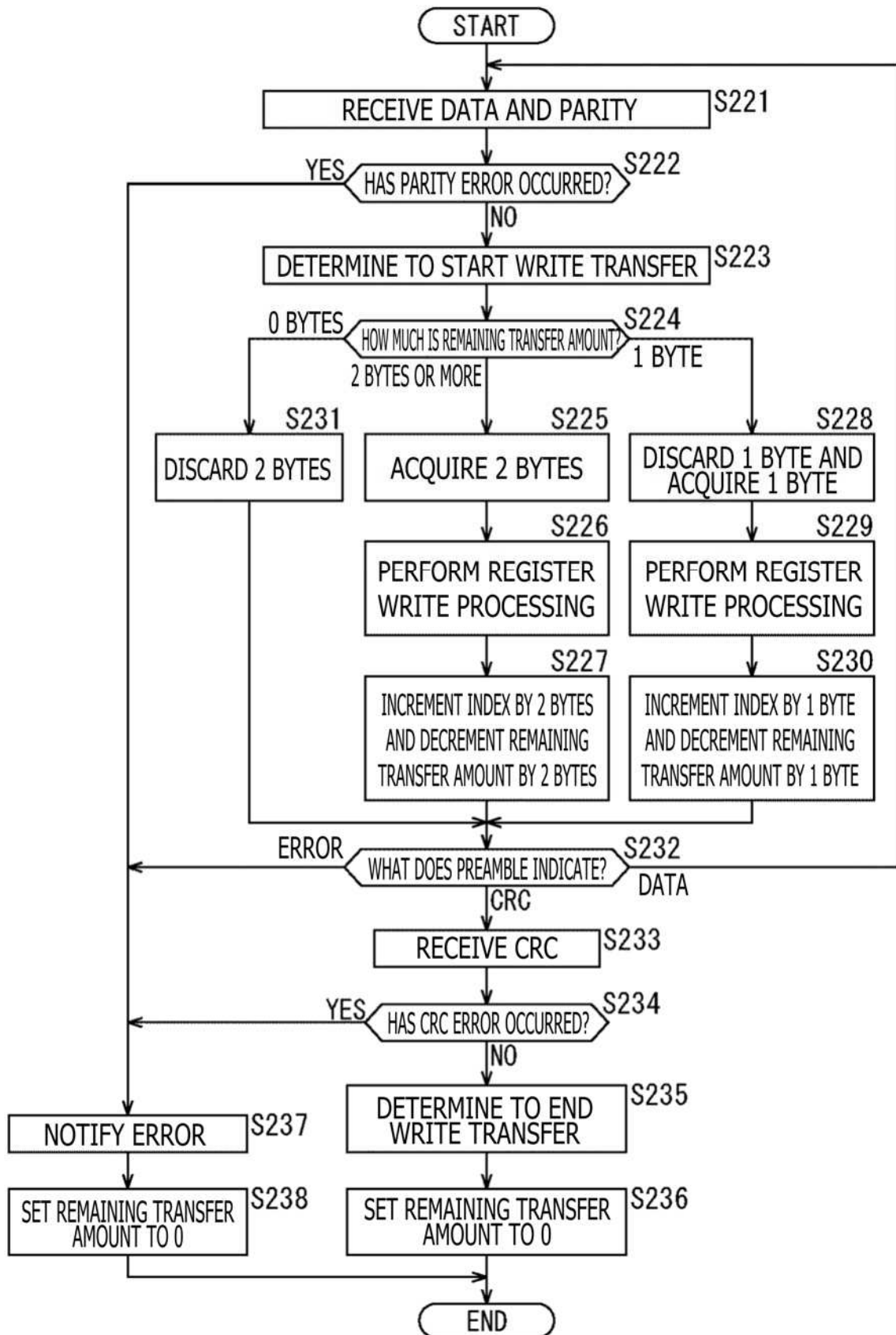


FIG. 22

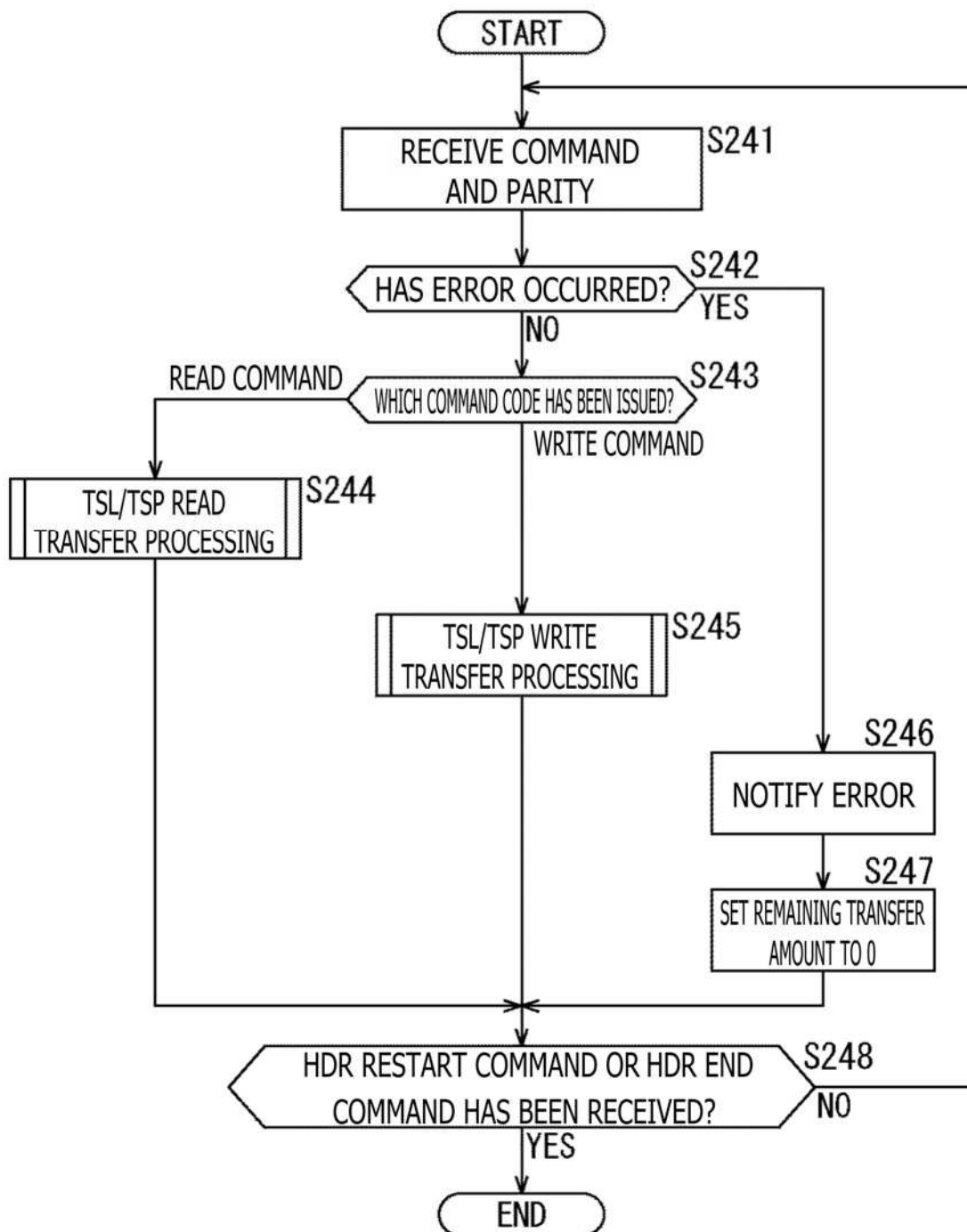


FIG. 23

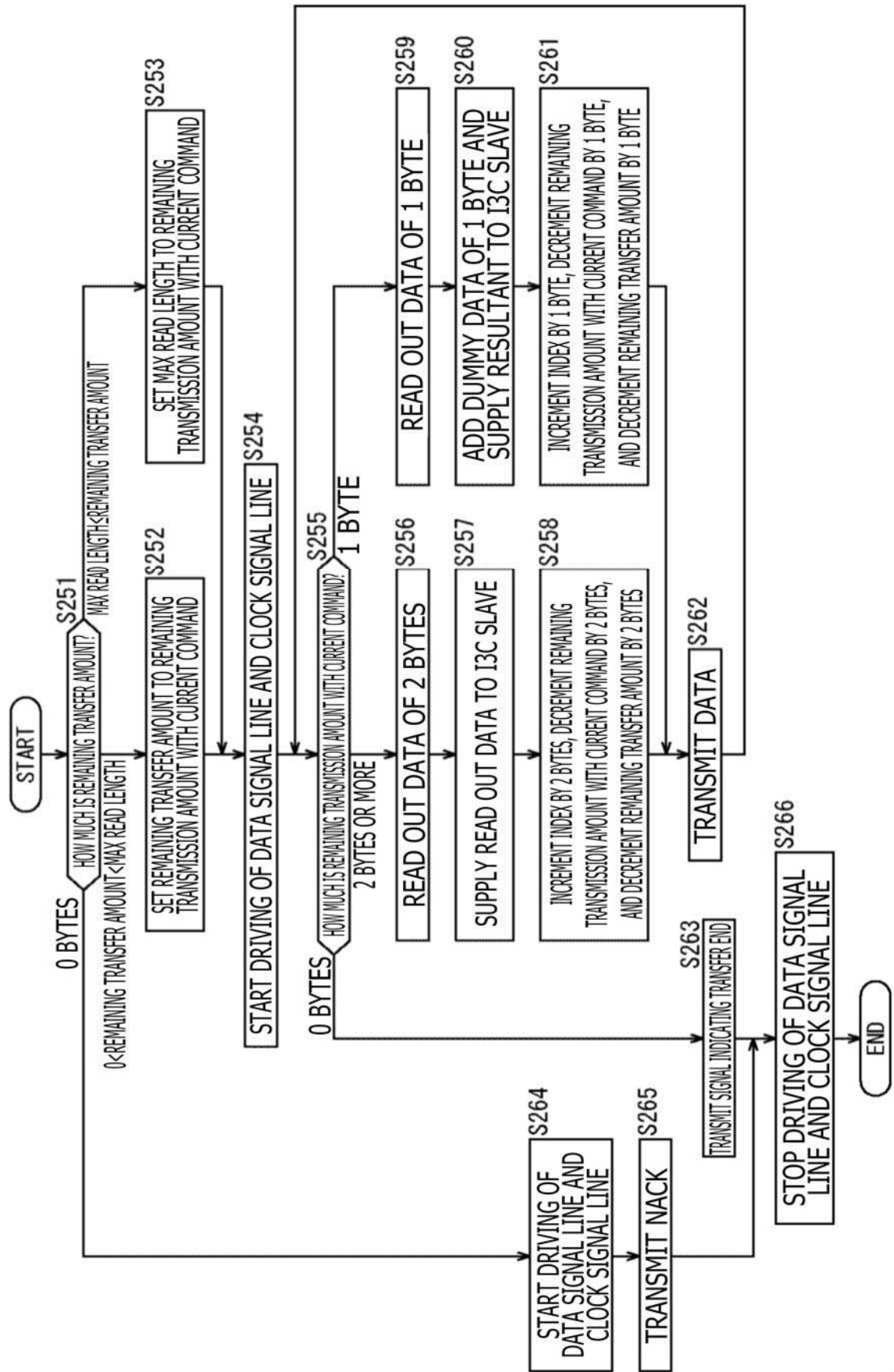


FIG. 24

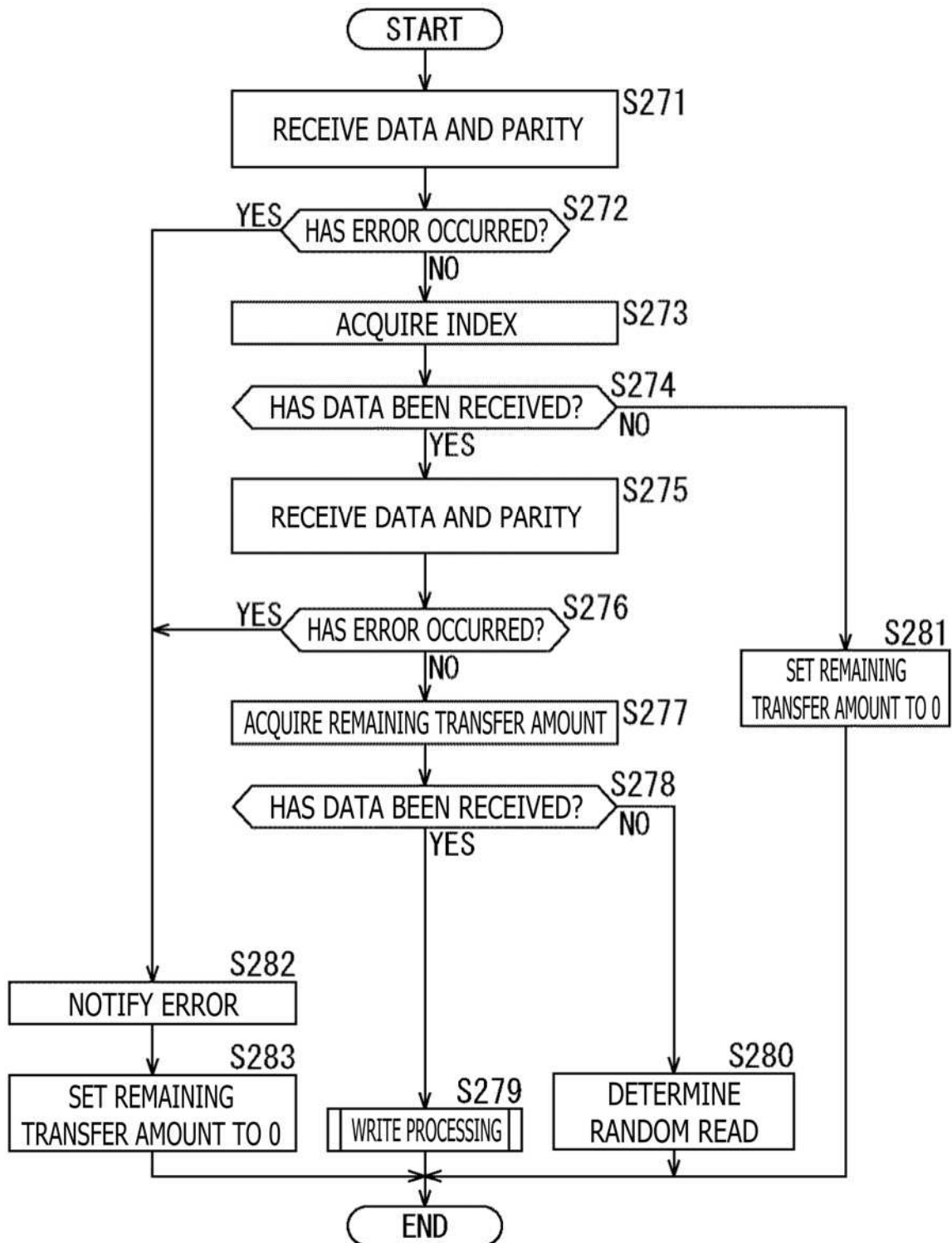


FIG. 25

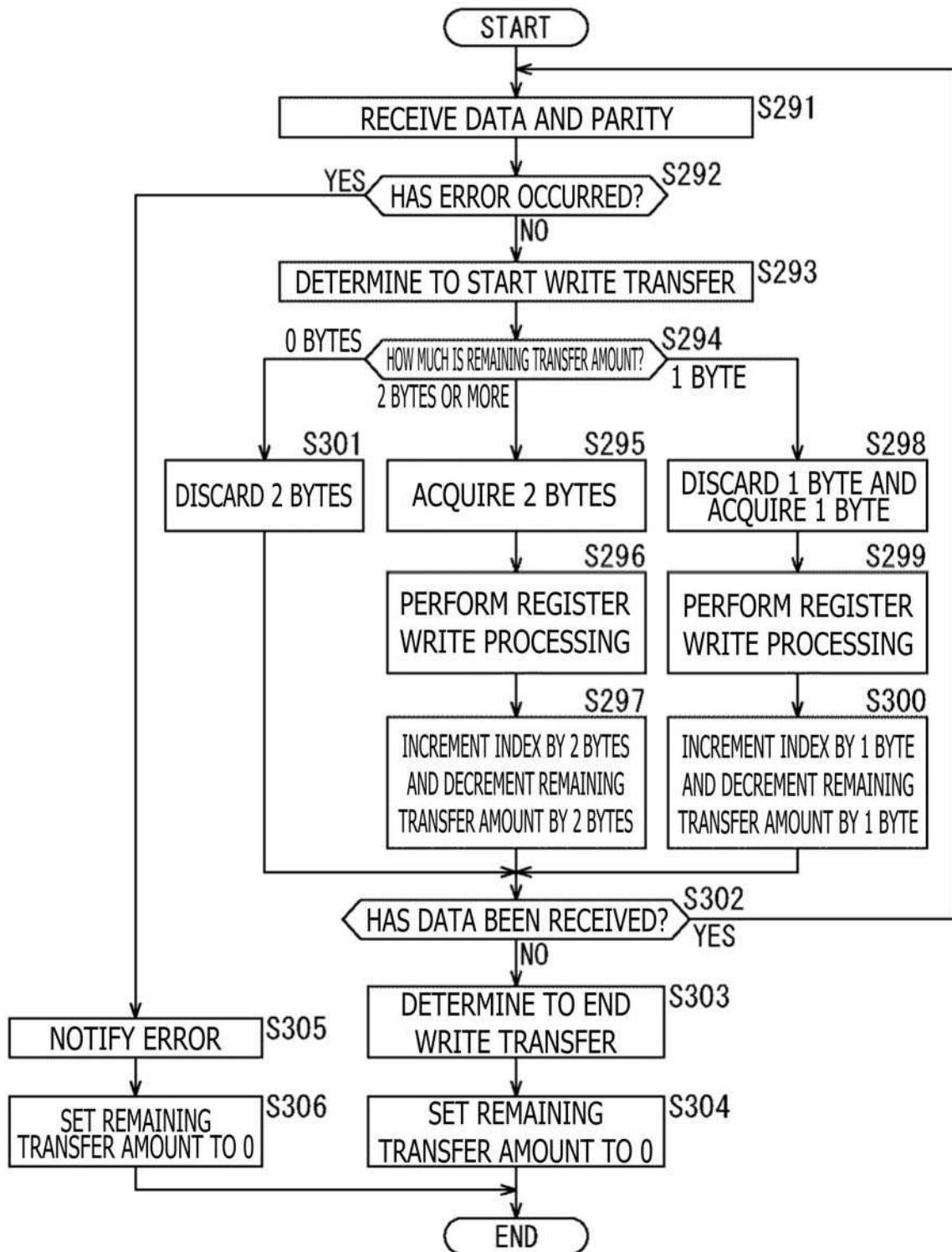


FIG. 26

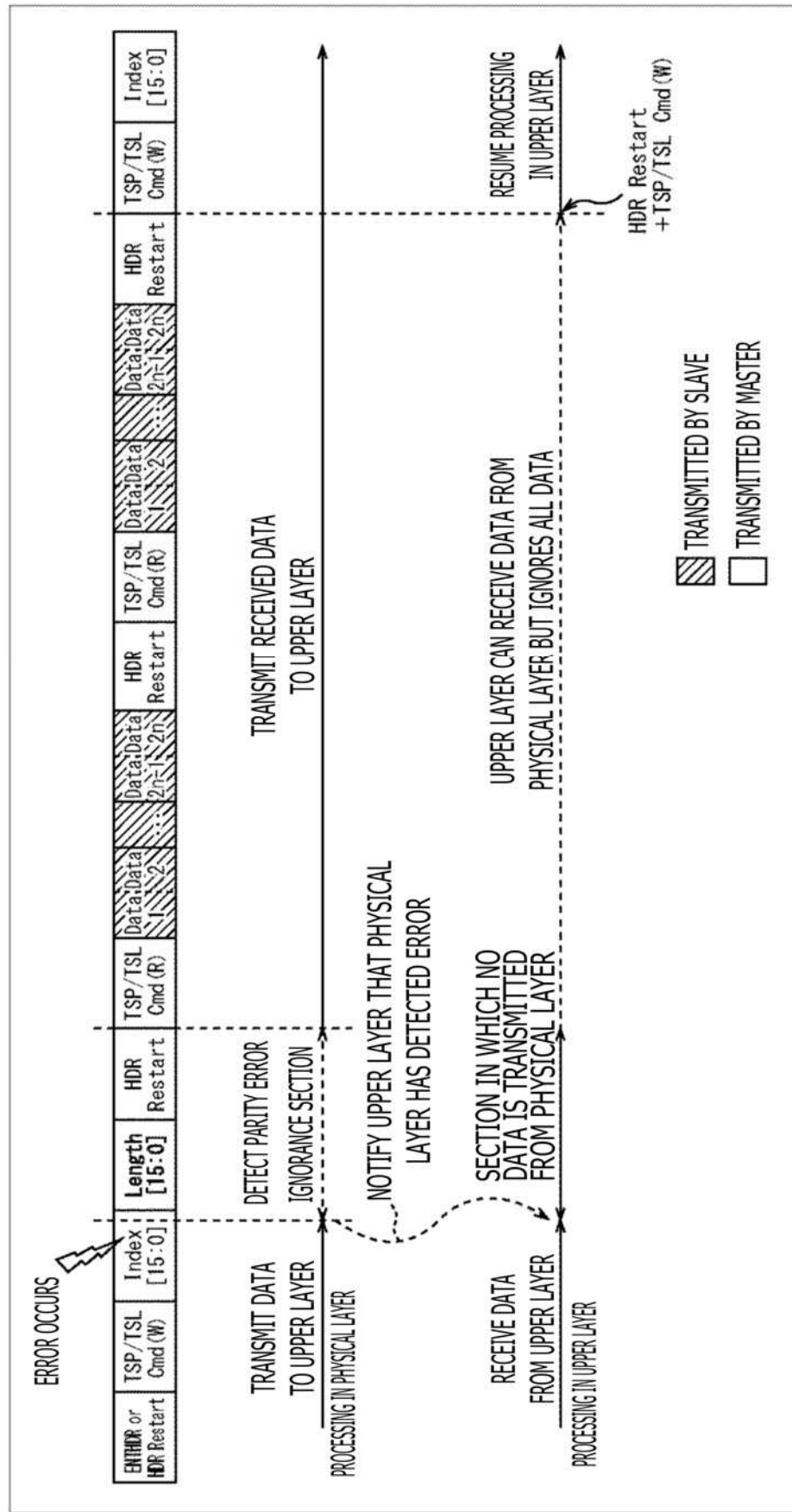


FIG. 27

