

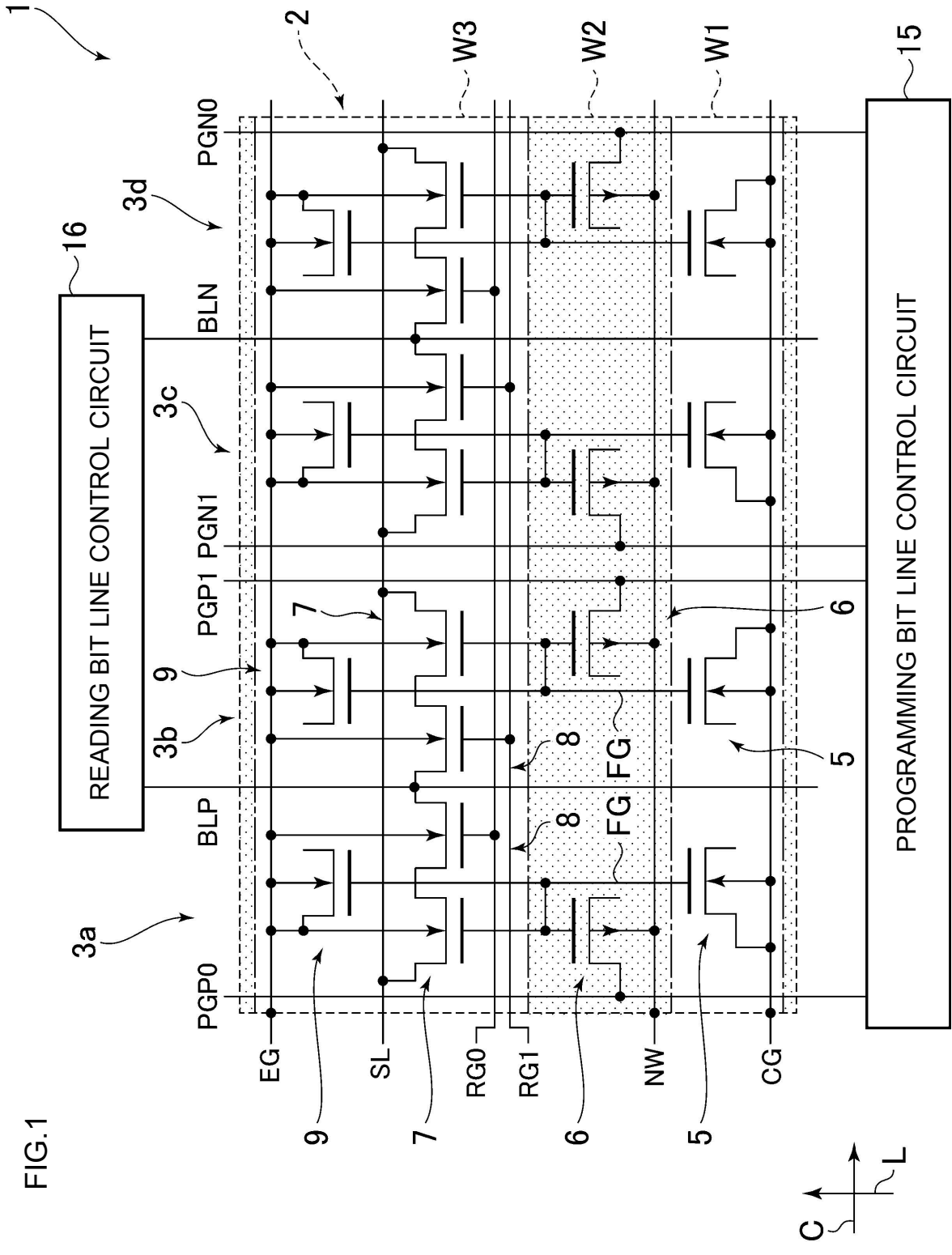


FIG. 2

	PROGRAMMING OPERATION		READING OPERATION		ERASING OPERATION
	SELECTED	NONSELECTED	SELECTED	NONSELECTED	
PROGRAMMING BIT LINE (PG)	V _p (12V)	V _i (4V)	0V	0V	V _i (4V)
READING BIT LINE (BL)	0V	0V	V _{dd} (1.5V)	0V	0V
CONTROL GATE LINE (CG)	V _n (-8V)	V _{dd} (1.5V)	V _{dd} (1.5V)	V _{dd} (1.5V)	V _p (12V)
SUBSTRATE VOLTAGE LINE (NW)	V _p (12V)	V _p (12V)	V _{dd} (1.5V)	V _{dd} (1.5V)	V _p (12V)
FIRST SWITCH GATE LINE (RG0) (SELECTED READ CELL)	0V	0V	V _{dd} (1.5V)	V _{dd} (1.5V)	0V
SECOND SWITCH GATE LINE (RG1) (NONSELECTED READ CELL)	0V	0V	0V	0V	0V
SOURCE LINE (SL)	0V	0V	0V	0V	0V
ERASE GATE LINE (EG)	0V	0V	0V	0V	V _n (-8V)

FIG. 3

