

ABSTRACT OF THE DISCLOSURE

Provided are a non-volatile memory device and an erasing method thereof. The erasing method of the non-volatile memory device including a plurality of cell strings in which memory cells and selection transistors are connected, includes: performing a first erase operation based on an erase voltage provided to a first electrode of at least one of the selection transistors and an erase control voltage provided to a second electrode of the at least one of the selection transistors; determining whether there are slow erase cells by performing a multiple erase verify operation based on first and second verify voltages, the second verify voltage being higher than the first verify voltage; adjusting, when there are slow erase cells, the erase control voltage such that a voltage difference between the erase voltage and the erase control voltage increases; and performing a second erase operation based on the adjusted erase control voltage.

FIG. 6