Description

The present invention relates to a bit-error correcting memory system employing a non-volatile memory.

An EEPROM includes a storage MOS transistor as a memory cell and a sense amplifier. The storage MOS transistor has a thin oxide film (tunneling oxide film) and a floating gate. The arrangement and operation of the EEPROM is described in, for example, "16K Bit EEPROM Electrically Erasable In a Bit Unit", Nikkei Electronics, June 23, 1980, pp. 198 to 207 and Japanese Laid-open Patent Application No. 1987/32823.

Fig. 1 shows typical characteristics of the memory cell of an EEPROM. A threshold voltage of the memory cell might change due to leakage of charge. Such leakage may be caused by degradation of the breakdown voltage of the tunneling oxide film after a large number of write-erase cycles, or by a pinhole of the tunneling oxide film. A threshold voltage Vt1 of the memory cell in a write state is about -2 V. On the other hand, a threshold voltage Vt2 of the memory cell in an erase state is about 8 V. When the threshold voltage Vt1 is deteriorated, it changes from about -2 V to about 2 V as shown at (a). When the threshold voltage Vt2 is deteriorated, it changes from about 8 V to about 2 V as shown at (b).

The sense amplifier of the EEPROM detects the threshold voltage of the memory cell and outputs data. When the threshold voltage Vt1 is lower than a sense voltage Vr, the sense amplifier outputs "1". On the other hand, when the threshold voltage Vt1 is not lower than the sense voltage Vr, the sense amplifier outputs "0". Therefore, when a low sense voltage Vr1, for example 1 V, is applied in case of the deterioration of the memory cell in write state, the output data is changed from "1" to "0". However, when a high sense voltage Vr2, for example 4 V, is applied in case of the deterioration of the memory cell in the write state, the output data is unchanged.

EP-A-0305897 discloses a known bit-error correcting memory system comprising: a non-volatile memory having a plurality of sets of cells, each set comprising a plurality of data bit cells and a parity bit cell; a control circuit for requesting read access to the non-volatile memory; a memory address latch for latching the address in the memory to be read; parity checking means for detecting bit-errors in data read from the non-volatile memory and producing an error signal during a first memory read instruction cycle if a bit-error is detected; and sense voltage generating means for changing the memory cell sense voltage in dependence on said error signal for a second succeeding memory read instruction cycle.

Considering EP-A-305897 in more detail, the disclosed memory system needs special control signals such as EACC, WACC, EROM etc., as set forth in the specification. Further, the disclosed memory system has complex hardware as shown in Figs. 6 and 7. Furthermore, the disclosed EEPROM has only one addressing mode because of the complex hardware of the bit error correcting circuit.

It is an object of the present invention to provide a bit error correcting circuit for a non-volatile memory having simple hardware.

The present invention is characteried in that the control circuit is responsive to said error signal indicating a bit-error during said first memory read instruction cycle to perform said second memory read instruction cycle; and the memory address latch is responsive to said error signal indicating a bit-error during said first memory read instruction cycle to retain its contents during said second memory read instruction cycle.

The detailed features of the present invention are defined in the independent claim, with preferred features as defined in the dependent claims.

An embodiment of the present invention will now be described, by way of example, with reference to the accompanying drawings, in which:

Fig. 1 is a graph showing typical characteristics of a deteriorated memory cell of a known EEPROM;

Fig. 2 is a block diagram of a microcomputer with a bit error correcting circuit for an EEPROM according to the preferred embodiment of the present invention;

Fig. 3 is a schematic diagram of a parity checking and parity bit generating circuit according to the preferred embodiment of the present invention; and

Fig. 4 is a timing chart showing how data are read from an EEPROM in Fig. 2.

Fig. 2 is a block diagram of a microcomputer with a bit error correcting circuit for an EEPROM according to the preferred embodiment of this invention. The entire circuit of this diagram may be formed in one semiconductor chip or a plurality of semiconductor chips as will be apparent to those skilled in the art.

A microcomputer 10 has a central processing unit (hereafter CPU) 12, first data terminals D0-D7, a first address terminal ADR, a first write signal terminal WR, a first read signal terminal RD, an output signal terminal OUT and an input signal terminal IN. An EEPROM 20 has a memory cell array 21, a row decoder 22, a column decoder 23, a multiplexer 24, a sense amplifier 25 and an input/output control circuit 26. The memory cell array 21 comprises a plurality of sets of cells, each set comprising a plurality of memory cells 28 for storing data and a parity cell 27 for storing a parity bit corresponding to the stored data. The input/output control circuit 26 has second data terminals D0-D7, a parity data terminal D8, a second write signal terminal WR, a second read signal terminal RD. The sense amplifier 25 has a sense voltage

switching signal terminal RD2. The row decoder 22 and the column decoder 23 each have a second address terminal ADR. The first data terminals D0-D7 are connected to the second data terminals D0-D7 via a data bus 30. The data bus 30 writes data to the EEPROM 20 and inputs and/or outputs data of the EEPROM 20 between microcomputer 10. The data bus 30 is connected to a parity checking and parity bit generating circuit 40. The parity checking and parity bit generating circuit 40 detects an error of data read from the EEPROM 20 and corrects the error.

Fig. 3 is a schematic diagram of the parity checking and parity bit generating circuit 40 showing in Fig. 1. The parity checking and parity bit generating circuit 40 comprises eight exclusive NOR gates. Each of exclusive NOR gate 100, 102, 104 and 106 has two input terminals connected to the data bus and an output terminal. An exclusive NOR gate 108 has two input terminals connected to the output terminals of the exclusive NOR gate 100 and 102 and an output terminal. An exclusive NOR gate 110 has two input terminals connected to the output terminals of the exclusive NOR gate 104 and 106 and an output terminal. An exclusive NOR gate 112 has two input terminals connected to the output terminals of the exclusive NOR gate 108 and 110 and an output terminal.

Referring again to Fig. 2, the output of the parity checking and parity bit generating circuit 40 (the output terminal of the exclusive NOR gate 112) is connected to the parity data terminal D8 of EEPROM 20, via a driver circuit 52 and a parity bit data line 54. The parity bit data line 54 inputs and/or outputs parity bit data of the EEPROM 20.

The first read signal terminal RD is connected to the second read signal terminal RD via a read signal line 58. The first write signal terminal WR is connected to the second write terminal WR via a write signal line 56. The write signal line 56 is also connected to a control terminal of the driver circuit 52. An input terminal and an output terminal of the driver circuit 52 are connected to input terminals of a comparison circuit 60. An output terminal of the comparison circuit 60 is connected to a data input terminal D of a data holding and sense voltage switching circuit 70. The comparison circuit 60 compares the parity bit data read from the EEPROM 20 and the output of the parity checking and parity bit generating circuit 40. In this embodiment, the comparison circuit 60 is an exclusive NOR gate.

The data holding and sense voltage keeping circuit 70 holds the output of the comparison circuit 60 and switches a sense voltage of the sense amplifier 25 in accordance with the read signal. The data holding and sense voltage switching circuit 70 comprises a flip-flop circuit. A clock terminal of the data holding and sense voltage switching circuit 70 is connected to the read signal line 58. An output terminal Q of the data holding and sense voltage switching circuit 70 is connected to the sense voltage switching signal terminal RD2 of the EEPROM 20. A reset terminal of the data holding and sense voltage switching circuit 70 is connected to the output signal terminal OUT of the microcomputer 10.

The input signal terminal IN of the microcomputer 10 is connected to the sense voltage switching signal terminal AD2 of the EEPROM 20 and to a latch terminal L of an address latch circuit 80. The first address terminal ADR of the microcomputer 10 is connected to an input terminal of the address latch circuit 80 via an address bus 82. An output terminal of the address latch circuit 80 is connected to the second address terminal ADR of the EEPROM 20. The address latch circuit 80 receives an address signal from the microcomputer and outputs it to the EEPROM 20. When the output of the data holding and sense voltage switching circuit 70 is "1", the address latch circuit 80 holds the inputed address.

The write and read operations performed by the microcomputer with the bit error correction circuit in Fig. 2 will be explained.

(1) Write operation

In case of writing data to the EEPROM 20, eight bits of writing data D0 to D7 are outputed from the microcomputer 10 to the data bus 30. Each bit of the writing data is either "1" or "0". The parity checking and parity bit generating circuit 40 checks the data D0 to D7 on the data bus 30 (parity check) and outputs a logic "1" or "0" (parity bit). The outputed logic determines whether the number of the writing data is an even number or an odd number. When the write signal WR is outputed from the microcomputer 10, the driver circuit 52 is turned on and 8 bits of the writing data D0 to D7 on the data bus 30 and a parity bit D8 which is outputed from the parity checking and parity bit generating circuit 40 via the driver circuit 52 and is on the parity bit data line 54, are read into the EEPROM 20 as one word. That is, the word written in the EEPROM 20 comprises the data D0 to D8 (8 bits of write data and 1 bit of parity data).

The read operation will be explained with reference to Fig. 4. Fig. 4 is a timing chart which shows how data are read from the EEPROM. Fig. 4 shows two read cycle A and B. A read cycle is completed in four machine cycles M1 to M4 which are synchronized with a system clock CLK of the microcomputer 10.

(2) Read operation

A read operation of the data D0 to D7 from the EEPROM 20 is carried out in one cycle A if no error in the read data is detected and in two cycles A and B if an error is detected.

i) The first read cycle A

The read operation is carried out synchronized with the system clock CLK of the microcomputer. The read cycle A is divided in four machine cycles M1 to M4. In machine cycles M3 and M4, a read command signal RD and an address ADR of desired data are outputed from the microcomputer 10. The data D0 to D7 stored in the addressed set of data cells 28 in the EEPROM 20 are read out to the data bus 30. The corresponding parity data D8 stored in the EEPROM 20 is read out to one input terminal of the comparison circuit 60 through the parity bit line 54. The read out data D0 to D7 on the data bus 30 is checked by the parity checking and parity bit generating circuit 40 (parity check). The result of the checking (parity bit) is outputed to the other input terminal of the comparison circuit 60.

If the two inputs of the comparison circuit 60 are equal, (i.e. the parity bit of the read data corresponds to the parity bit of the written data), there is no error in the read data. In this case, the comparison circuit 60 outputs "0". The data holding and sense voltage switching circuit 70 holds its output Q at the logic "0" level until the read command signal RD is inputed in the data holding and sense voltage switching circuit 70. Then, another first read cycle A will be carried out.

If the two inputs of the comparison circuit 60 are different, there is an error in storing. The comparison circuit 60 outputs a logic "1" and the data holding and sense voltage switching circuit 70 holds its output Q at the logic "1" level until the read command signal RD is inputed in the data holding and sense voltage switching circuit 70. When the sense amplifier 25 receives the logic "1", it changes the sense voltage, for example, from +1V (the low sense voltage Vr1 in Fig. 2) to +4V (the high sense voltage Vr2 in Fig. 2). When the address latch circuit 80 receives the logic "1", it holds the address ADR received from the address bus 82. Furthermore, when the microcomputer 10 receives the logic "1" at the input signal terminal IN, it acknowledges the error in the stored data and carries out the second read cycle B.

ii) The second read cycle B

The operation of the second read cycle B is similar to that of the first read cycle A except for the changed sense voltage and the origin of the address. In the second read cycle B, the sense voltage is initially +4V and the address is not from the microcomputer 10 but rather is the address held in address latch circuit 80 from the first read cycle A. Therefore, in the second read cycle, the same data is again read out, but with a high sense voltage rather than a low sense voltage as in read cycle A, so that the outputed data D0 to D7 on the data bus 30 are correct.

The first and the second read cycles A and B are preferably carried out continuously. However, another operation (e.g. calculate operation etc.) may be carried out between the first and second read cycles as shown in Fig. 3, without adverse effect. The above mentioned read operation can be carried out by an ordinary move operation and/or load operation which are included in standard commercial microcomputers having the usual write signal WR, read signal RD, input signal IN and output signal OUT ports.

The bit error correcting circuit of the present invention is comprised of simple hardware as shown in Fig. 2. Futhermore, the bit error circuit of the present invention can be applied in a plurality of addressing modes. That is, addressing the EEPROM through the address latch circuit is not critical. Other addressing modes will be apparent to those skilled in the art. Further, while in the disclosed embodiment a microcomputer is described, a control circuit such as a microprocessor and CPU core can be substituted for the microcomputer.

Claims

1. A bit-error correcting memory system comprising:
   a non-volatile memory (21) having a plurality of sets of cells, each set comprising a plurality of data bit cells (28) and a parity bit cell (27);
   a control circuit (10) for requesting read access to the non-volatile memory (21);
   a memory address latch (80) for latching the address in the memory (21) to be read;
   parity checking means (40,60,70) for detecting bit-errors in data read from the non-volatile memory (21) and producing an error signal during a first memory read instruction cycle if a bit-error is detected; and
   sense voltage generating means (25) for changing the memory cell sense voltage in dependence on said error signal for a second succeeding memory read instruction cycle;
   characterised in that
   the control circuit (10) is responsive to said error signal indicating a bit-error during said first memory read instruction cycle to perform said second memory read instruction cycle; and
   the memory address latch (80) is responsive to said error signal indicating a bit-error during said first memory read instruction cycle to retain its contents during said second memory read instruction cycle.

2. A system according to claim 1, wherein said parity checking means (40,60,70) comprises a parity bit generating circuit (40) for generating a parity bit for data read from the memory (21), and comparison means (60) for comparing the parity bit

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The bit error correcting circuit of the present invention is comprised of simple hardware as shown in Fig. 2. Futhermore, the bit error circuit of the present invention can be applied in a plurality of addressing modes. That is, addressing the EEPROM through the address latch circuit is not critical. Other addressing modes will be apparent to those skilled in the art. Further, while in the disclosed embodiment a microcomputer is described, a control circuit such as a microprocessor and CPU core can be substituted for the microcomputer.

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   a control circuit (10) for requesting read access to the non-volatile memory (21);
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   sense voltage generating means (25) for changing the memory cell sense voltage in dependence on said error signal for a second succeeding memory read instruction cycle;
   characterised in that
   the control circuit (10) is responsive to said error signal indicating a bit-error during said first memory read instruction cycle to perform said second memory read instruction cycle; and
   the memory address latch (80) is responsive to said error signal indicating a bit-error during said first memory read instruction cycle to retain its contents during said second memory read instruction cycle.

2. A system according to claim 1, wherein said parity checking means (40,60,70) comprises a parity bit generating circuit (40) for generating a parity bit for data read from the memory (21), and comparison means (60) for comparing the parity bit

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generated by the parity checking circuit (40) with the parity bit read from the memory (21) and outputting the error signal indicating the result of the comparison.

3. A system according to claim 1 or 2, wherein the parity checking means (40,60,70) includes a flip-flop (70) for outputting the error signal.

4. A system according to claim 1, 2 or 3, wherein the control circuit (10) comprises a microcomputer (10).

Patentansprüche

1. Bitfehlerkorrektur-Speichersystem, das folgendes aufweist:

einen nichtflüchtigen Speicher (21) mit einer Vielzahl von Zellensätzen, wobei jeder Satz eine Vielzahl von Datenbitzellen (28) und eine Paritätsbitzelle (27) aufweist;

eine Steuerschaltung (10), um einen Lesezugriff auf den nichtflüchtigen Speicher (21) anzufordern;

einen Speicheradressen-Latch (80) zum Zwischenspeichern der Adresse in dem zu lesenden Speicher (21);

eine Paritäts-Prüfeinrichtung (40, 60, 70), um Bitfehler in Daten festzustellen, die aus dem nichtflüchtigen Speicher (21) gelesen wurden, und um während eines ersten Speicherlesebefehlszyklus ein Fehlersignal zu erzeugen, wenn ein Bitfehler festgestellt wird; und

eine Lesespannungs-Erzeugungseinrichtung (25), um die Speicherzellen-Lesespannung in Abhängigkeit vom Fehlersignal für einen zweiten, nachfolgenden Speicherlesebefehlszyklus zu verändern;

dadurch gekennzeichnet, daß

die Steuerschaltung (10) anspricht, wenn das Fehlersignal während des ersten Speicherlesebefehlszyklus einen Bitfehler anzeigt, um den zweiten Speicherlesebefehlszyklus durchzuführen; und dadurch, daß

der Speicheradressen-Latch (80) anspricht, wenn das Fehlersignal während des ersten Speicherlesebefehlszyklus einen Bitfehler anzeigt, um seinen Inhalt während des zweiten Speicherlesebefehlszyklus aufrechtzuerhalten.

2. System nach Anspruch 1, bei dem die Paritäts-Prüfeinrichtung (40, 60, 70) eine Paritätsbit-Erzeugungsschaltung (40) zum Erzeugen eines Paritätsbits für aus dem Speicher (21) gelesene Daten sowie eine Vergleichseinrichtung (60) zum Vergleichen des von der Paritäts-Prüfeinrichtung (40) erzeugten Paritätsbits mit dem aus dem Speicher (21) gelesenen Paritätsbit und zum Ausgeben des Fehlersignals aufweist, das das Ergebnis des Vergleichs angibt.

3. System nach Anspruch 1 oder 2, bei dem die Paritäts-Prüfeinrichtung (40, 60, 70) ein Flip-Flop (70) zum Ausgeben des Fehlersignals aufweist.

4. System nach Anspruch 1, 2 oder 3, bei dem die Steuerschaltung (10) einen Mikrocomputer (10) aufweist.

Revendications

1. Système de mémoire corrigeant les erreurs sur les bits comprenant:

une mémoire (21) non volatile ayant plusieurs ensembles de cellules, chaque ensemble comprenant plusieurs cellules (28) de bits de données et une cellule (27) de bit de parité;

un circuit (10) de commande pour demander un accès en lecture à la mémoire (21) non volatile;

un registre (80) à verrouillage d'adresse de mémoire pour verrouiller l'adresse dans la mémoire (21) à lire;

un moyen (40,60,70) de contrôle de parité pour détecter des erreurs sur les bits dans les données lues dans la mémoire (21) non volatile et produire un signal d'erreur pendant un premier cycle d'instruction de lecture de mémoire si une erreur sur un bit est détectée; et

un moyen (25) générateur de tension de lecture pour modifier la tension de lecture de cellules de mémoire en fonction dudit signal d'erreur lors d'un second cycle d'instruction de lecture de mémoire suivant;

caractérisé en ce que

le circuit (10) de commande est sensible audit signal d'erreur indiquant une erreur s;ur un bit pendant ledit premier cycle d'instruction de lecture de mémoire pour effectuer ledit second cycle d'instruction de lecture de mémoire; et

le registre (80) à verrouillage d'adresse de mémoire est sensible audit signal d'erreur indiquant une erreur sur un bit pendant ledit premier cycle d'instruction de lecture de mémoire pour retenir son contenu pendant ledit second cycle d'instruction de lecture de mémoire.

2. Système selon la revendication 1, dans lequel ledit moyen (40,60,70) de contrôle de parité comprend un circuit (40) générateur de bit de parité pour générer un bit de parité pour les données lues dans la mémoire (21) et un moyen (60) de comparaison pour comparer le bit de parité généré par le circuit (40) de contrôle de parité au bit

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de parité lu dans la mémoire (21) et fournir en sortie le signal d'erreur indiquant le résultat de la comparaison.

3. Système selon la revendication 1 ou 2, dans lequel le moyen (40,60,70) de contrôle de parité comporte une bascule (70) pour fournir en sortie le signal d'erreur.

4. Système selon la revendication 1, 2 ou 3, dans lequel le circuit (10) de commande comprend un microcalculateur (10).