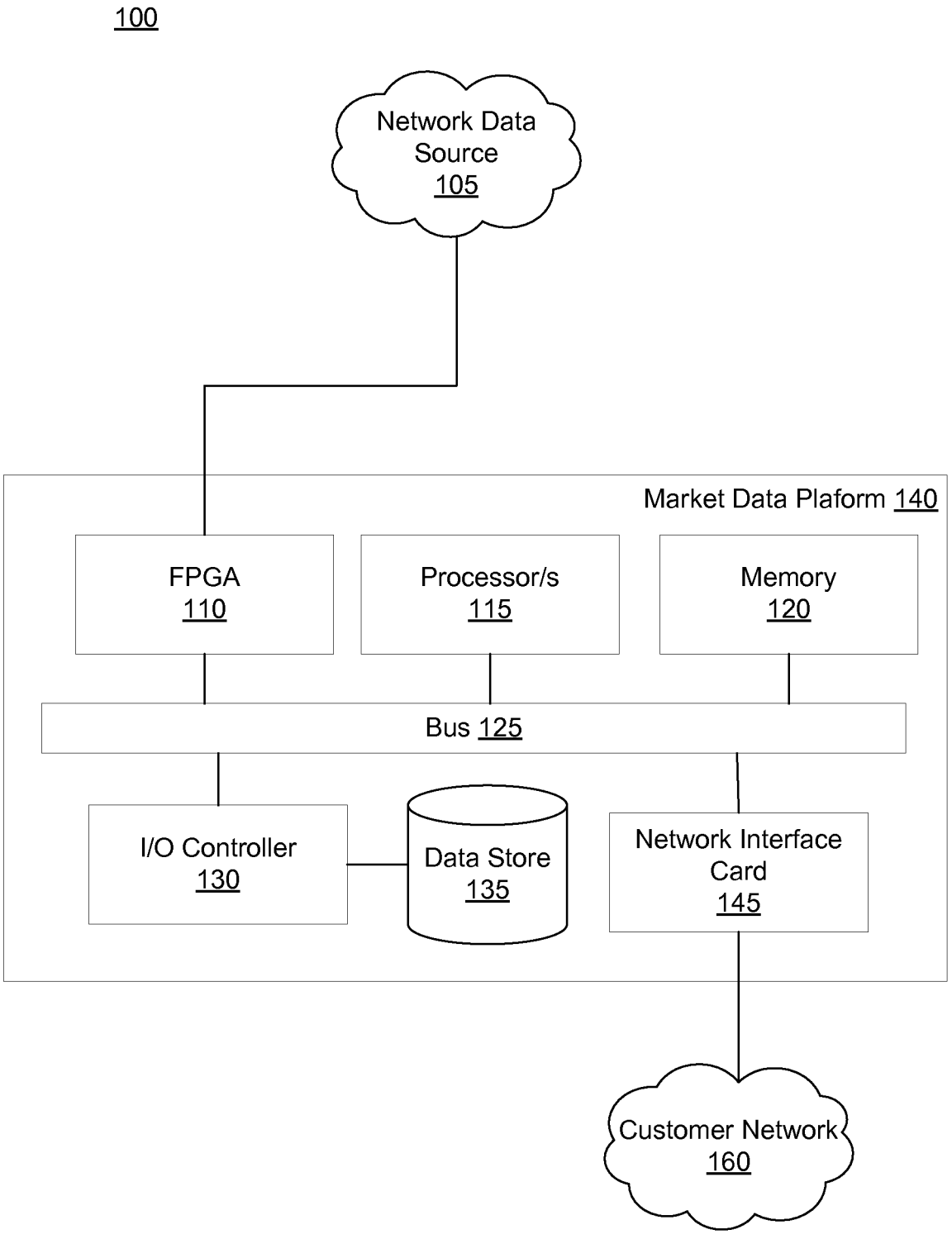

100
Network Data Source 105
Market Data Plaform 140
FPGA 110
Processor/s 115
Memory 120
Bus 125
I/O Controller 130
Data Store 135
Network Interface Card 145
Customer Network 160

FIG. 1

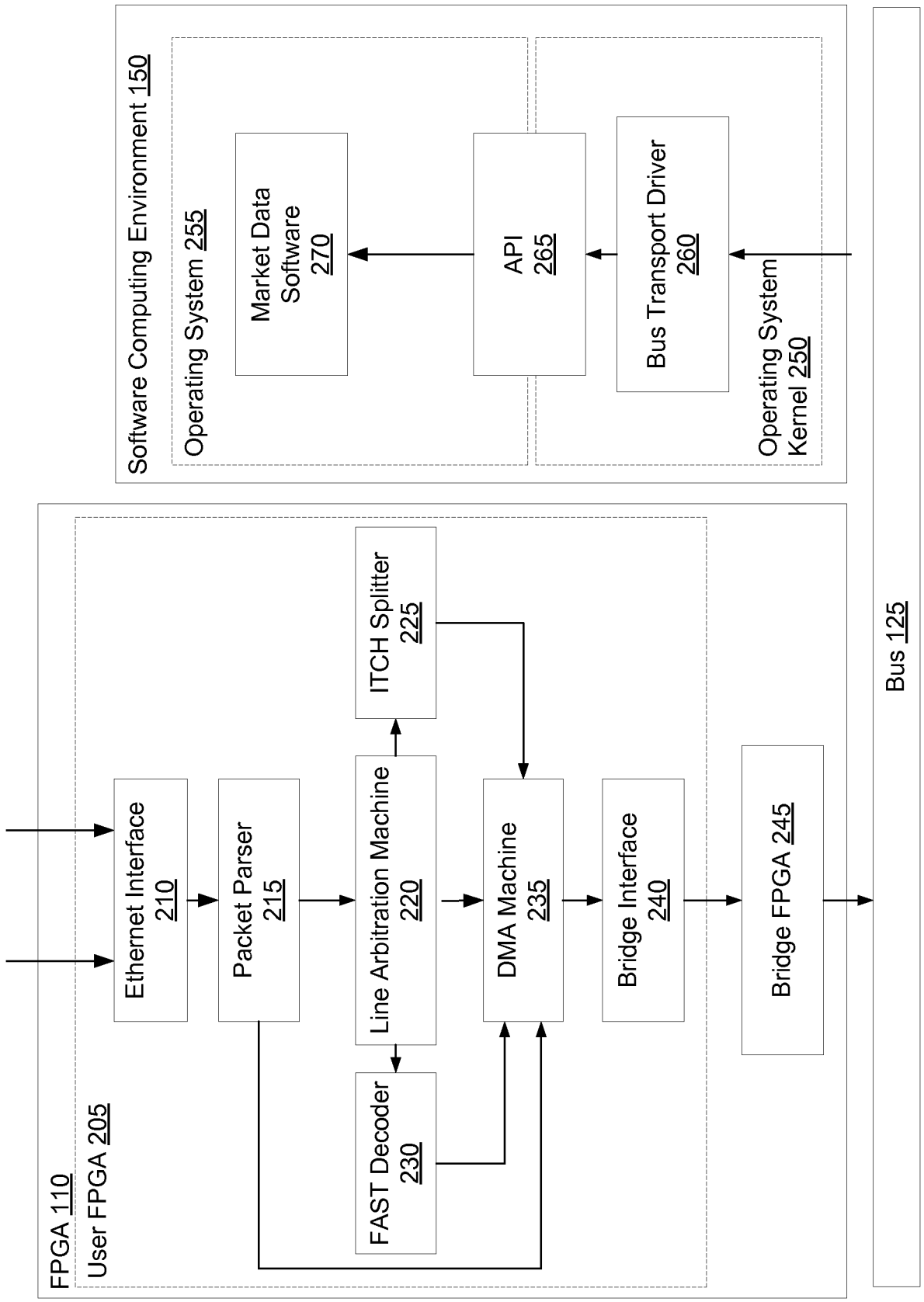

Software Computing Environment 150
Operating System 255
Market Data Software 270
API 265
Bus Transport Driver 260
Operating System Kernel 250
FPGA 110
User FPGA 205
Ethernet Interface 210
Packet Parser 215
Line Arbitration Machine 220
ITCH Splitter 225
FAST Decoder 230
DMA Machine 235
Bridge Interface 240
Bridge FPGA 245
Bus 125

FIG. 2

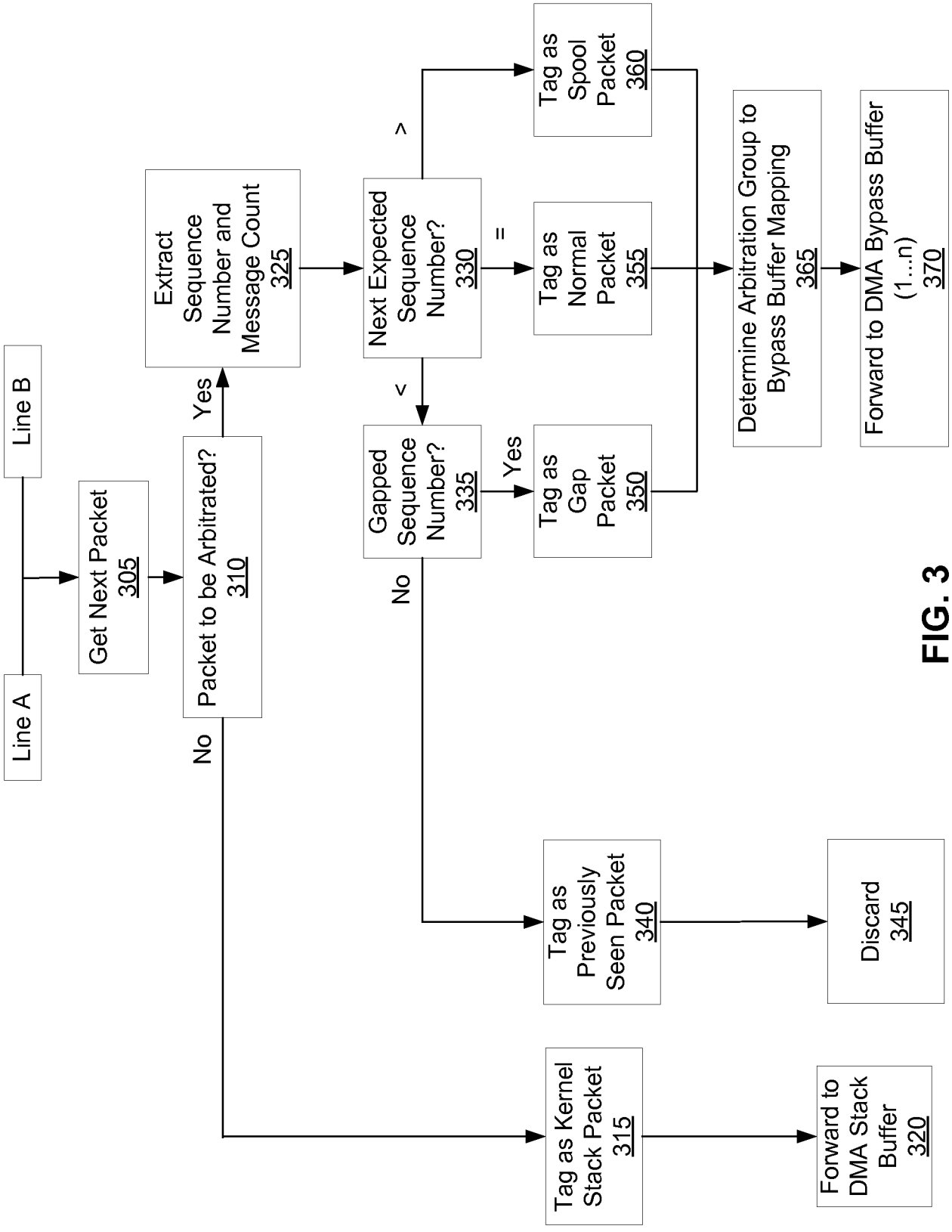

Line A
Line B
Get Next Packet 305
Packet to be Arbitrated? 310
Yes
No
Extract Sequence Number and Message Count 325
Next Expected Sequence Number? 330
>
=
<
Tag as Spool Packet 360
Tag as Normal Packet 355
Gapped Sequence Number? 335
Yes
No
Tag as Gap Packet 350
Determine Arbitration Group to Bypass Buffer Mapping 365
Forward to DMA Bypass Buffer (1...n) 370
Tag as Kernel Stack Packet 315
Forward to DMA Stack Buffer 320
Tag as Previously Seen Packet 340
Discard 345

FIG. 3

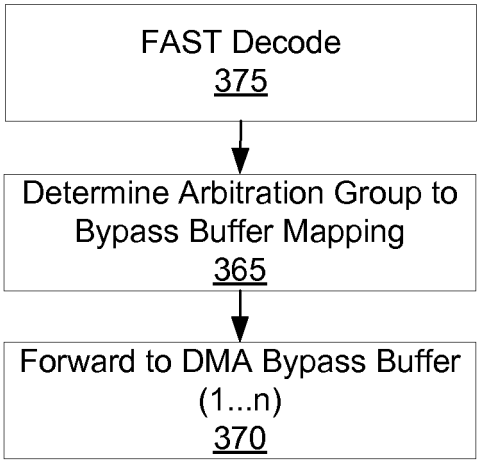

FAST Decode
375
Determine Arbitration Group to Bypass Buffer Mapping
365
Forward to DMA Bypass Buffer (1...n)
370

FIG. 4A

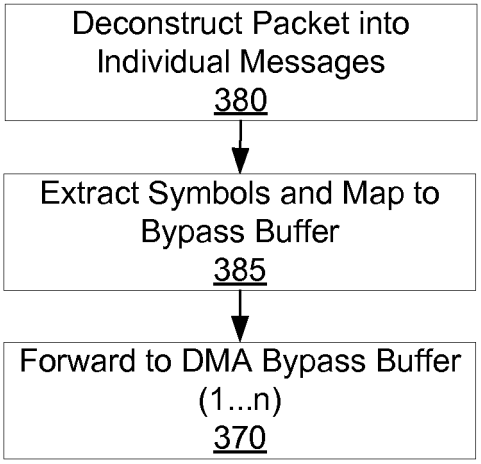

Deconstruct Packet into Individual Messages
380
Extract Symbols and Map to Bypass Buffer
385
Forward to DMA Bypass Buffer (1...n)
370

FIG. 4B

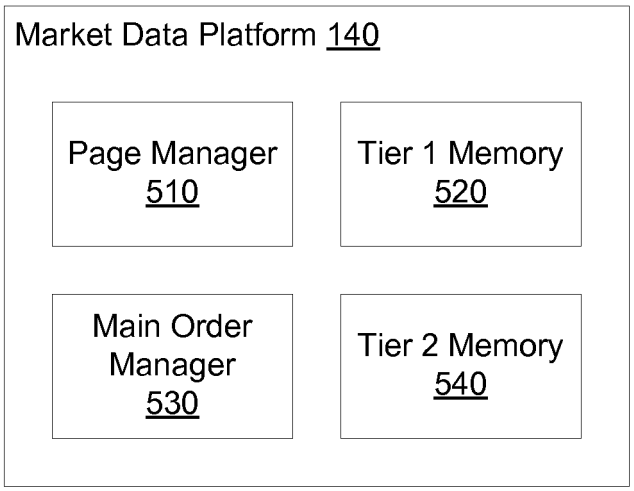

Market Data Platform 140
Page Manager 510
Tier 1 Memory 520
Main Order Manager 530
Tier 2 Memory 540

FIG. 5

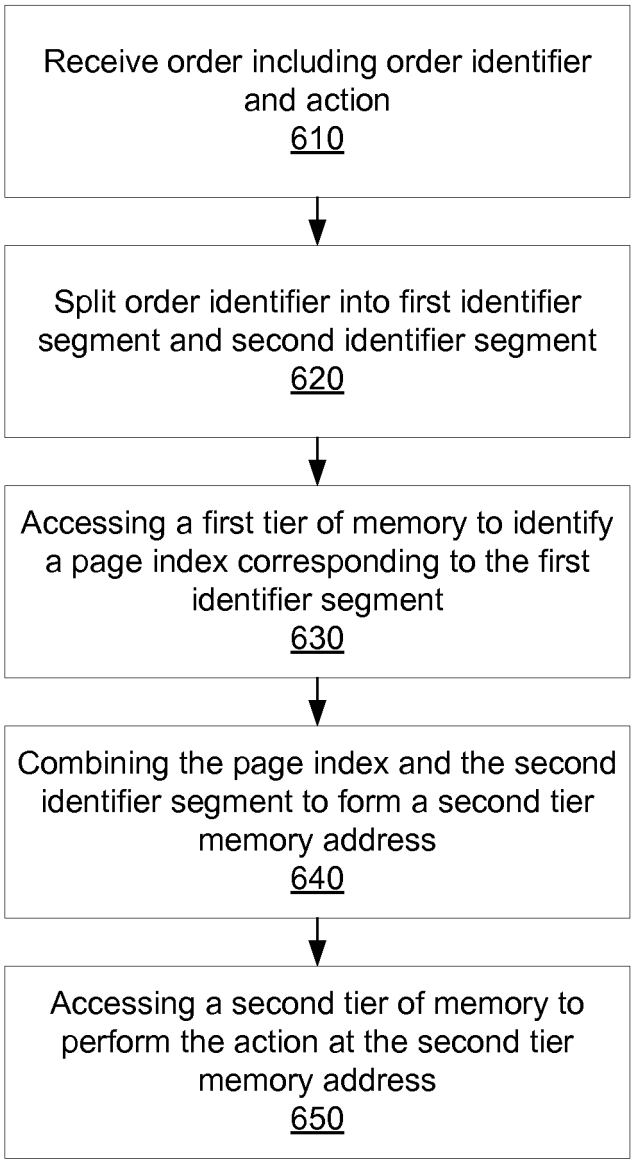

Receive order including order identifier and action
610
Split order identifier into first identifier segment and second identifier segment
620
Accessing a first tier of memory to identify a page index corresponding to the first identifier segment
630
Combining the page index and the second identifier segment to form a second tier memory address
640
Accessing a second tier of memory to perform the action at the second tier memory address
650

FIG. 6

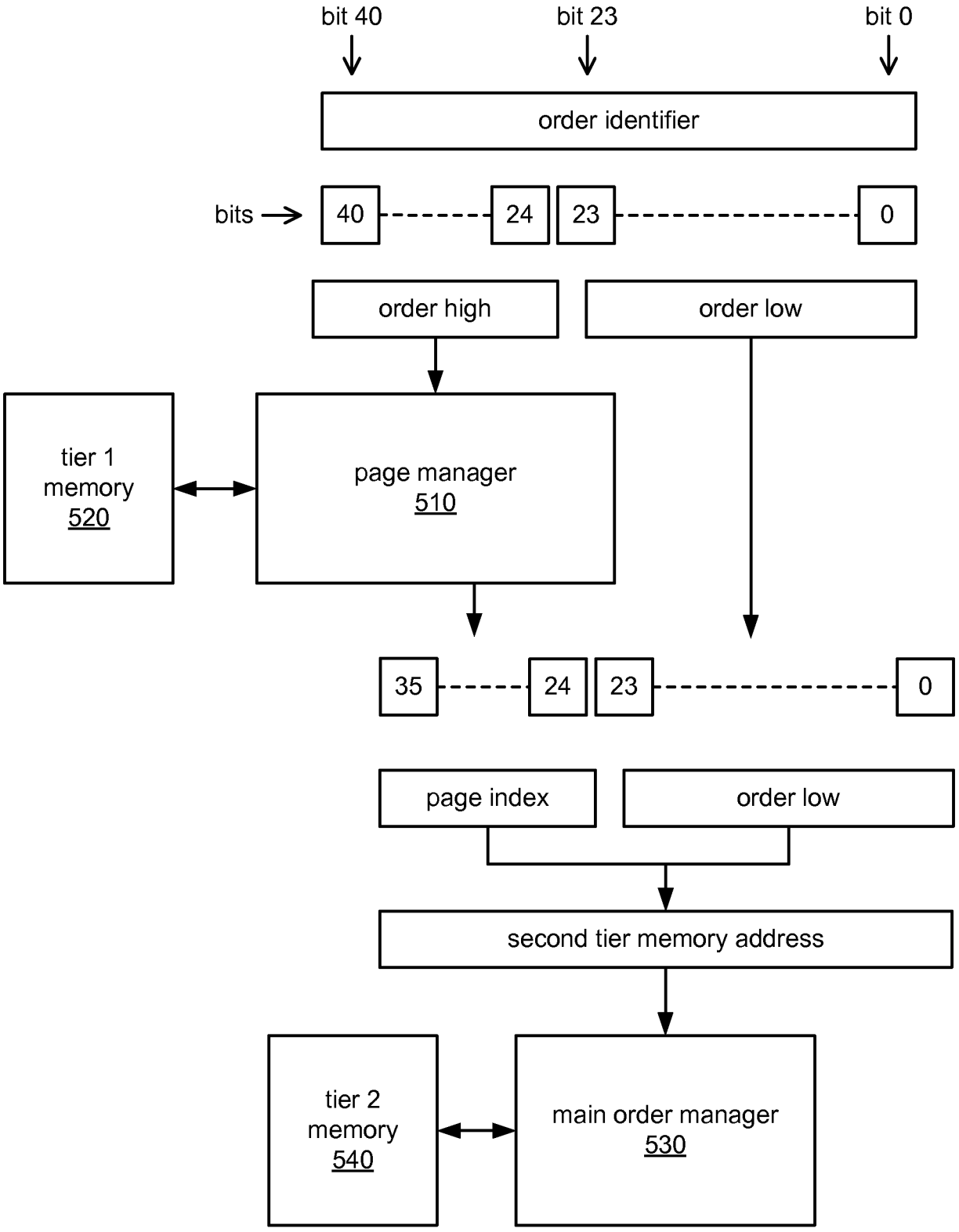

bit 40
bit 23
bit 0
order identifier
bits
40
24
23
0
order high
order low
tier 1
memory
520
page manager
510
35
24
23
0
page index
order low
second tier memory address
tier 2
memory
540
main order manager
530

FIG. 7