

ABSTRACT OF THE DISCLOSURE

A memory device includes a substrate; a stacked structure including a plurality of gate layers and a plurality of interlayer insulating layers that are alternately stacked on the substrate in a vertical direction, the stacked structure including a row of cutouts, each of the cutouts extending in a first horizontal direction and being configured to cut the plurality of gate layers, the cutouts being apart from each other and arranged in a cell region of the stacked structure in the first horizontal direction; and a row of channel structures, the channel structures being arranged in the cell region in the first horizontal direction, each of the channel structures extending in the vertical direction to penetrate the plurality of gate layers.

FIG. 4A