Description

The present invention relates to a method of producing a thin semiconductor layer of substantially uniform thickness upon which semiconductor structures can be subsequently formed.

In the present era of very large scale integration (VLSI), in which the dimensions of transistors and other semiconductor structures are shrinking below one micrometer, a host of new problems must be addressed. In general, greater isolation is required between devices. For CMOS applications, this isolation must prevent latch-up. At the same time, this increased isolation must not be provided at the expense of available chip space.

Silicon-on-insulator technology appears to be a particularly promising method of addressing this problem. A general example of this technology is shown in the article by R. J. Lineback, "Buried Oxide Marks Route to SOI Chips", Electronic-sWeek, October 1, 1984, pp. 11-12. As shown in this article, oxygen ions are implanted into a bulk silicon to form a buried oxide layer therein. The implant is then annealled for two hours so that the portion of the silicon lying above the buried oxide is single-crystal silicon. The various semiconductor devices are then formed on the single-crystal layer. The underlying buried oxide provides isolation between adjacent devices.

More recently, a specific method of forming silicon-on-insulator structures has evolved, in which two silicon substrates are bonded together and one of the substrates is at least partially removed. An example of this method is disclosed in an article by M. Kimura et al, "Epitaxial Film Transfer Technique for Producing Single Crystal Si Film on an Insulating Substrate", Applied Physics Letters, Vol. 43, No. 3, August 1, 1983. As described in this article, a first substrate has a P+ epitaxial layer grown thereon. A second substrate has a layer of oxide grown thereon. Both substrates are then coated with a glass, and the two substrates are bonded together using these glass layers. More specifically, the glass layers of the two substrates are pressed together and are heated to about 930° C. After the substrates are bonded together, the substrate having the epitaxial layer is removed, leaving behind the epitaxial layer on the bonded glass layers. The glass layers provide insulation. See also the article by Brock et al, "Fusing of Silicon Wafers", IBM Technical Disclosure Bulletin, Vol. 19, No. 9, February 1977, pp. 3405-3406, in which it is stated that "wafers may be fused together conveniently by forming a layer of silicon dioxide on each wafer, then placing the layers of silicon dioxide abutting each other, and heating, preferably in a steam atmosphere at a temperature in the order of 1050° C for about one half hour."

U.S. Patent No. 4,142,925 (issued 3/3/79 to King et al) discloses a method of making a structure which includes an epitaxial layer, an insulator layer and a polished silicon layer. As shown in the front figure of the patent, an epitaxial layer is grown on an n+ silicon substrate. An insulator layer of SiO_2 is grown on the epitaxial layer, and the insulator is covered with a polysilicon support layer. The n+ silicon substrate is then removed, leaving the epitaxial layer atop the SiO_2 layer.

It has been found that the step of removing the silicon substrate without removing the underlaying epitaxial layer is facilitated if these two layers have different doping concentrations or are of different conductivity types. For example, if the substrate is p+ and the epitaxial layer is p- or n type, the substrate may be removed by etching in a 1:3:8 solution of hydroflouric, nitric and acetic ("HNA") acid.

A problem with the above process is that the HNA acid will etch to the p+/p- or p+/n junction, which does not occur at the actual physical interface of these two layers. For example, in order to form a final n epitaxial layer of 200nm (nanometers) on a p+ substrate, an epitaxial layer of 1000-1200nm must be deposited. This is because boron will out- diffuse from the substrate into the epitaxial layer, such that the p+/n junction actually occurs at a point approximately 800-1000nm, respectively, above the physical interface between the substrate and the epitaxial layer.

Forming a 1000-1200nm layer of epitaxy leads to another problem. Typically, when working in the nm range, the deposition tools used in the industry can deposit a layer with approximately plus or minus 5 percent error. Thus, if the original epitaxial layer is 1000nm thick, the final epitaxial layer (i.e. after removal of the p+ substrate) will be approximately 250± 50nm thick. When the dopant concentration of the epitaxial layer is sufficiently low, the depletion regions of the channels of FETs subsequently formed on the epitaxial layer will extend to the bottom of the layer. Hence, the threshold voltages of these FETs are at least partially determined by the thickness of the epitaxial layer, such that the above variation in thickness would lead to an unacceptable variation in the threshold voltages of the FETs. Obviously, as the thickness of the epitaxial layer as initially deposited is increased, the resultant thickness variation increases. For example, if the initial epitaxial thickness is 2500 nm, its final thickness would be approximately 250± 150 nm.

U.S.Patent No. 3,976,511 discloses a method for fabricating integrated circuit structures involving the formation of a thin semiconductor layer. Ions are implanted into a silicon substrate to form a buried layer under a thin surface layer, this being

followed by the deposition of a support substrate. Then, the silicon substrate and the buried layer are removed, leaving the surface layer on the support substrate. Although the thickness of this layer is quite uniform, still better thickness control is desired.

It is thus an object of the present invention to provide an improved silicon- on-insulator fabrication process.

It is another object of the invention to provide a silicon-on-insulator process by which the thickness of the final silicon layer is substantially uniform.

It is yet another object of the invention to provide an improved silicon-on-insulator fabrication process in which the etching of the final silicon layer may be more precisely controlled.

These and other objects of the invention are realized in the process of forming a thin semiconductor layer having a substantially uniform thickness defined in claim 1. After a thin epitaxial layer is formed on a silicon substrate, ions are implanted into the epitaxial layer in order to form a thin buried etch-stop layer therein. The buried layer has etching characteristics which differ from those of the epitaxial layer. After bonding the epitaxial layer to a support substrate, the silicon substrate and portions of the epitaxial layer overlaying the buried layer are removed. Subsequently, the remainder of the epi layer above the buried layer is removed in an etchant which does not appreciably attack the buried layer. The buried layer is then removed.

The remaining epitaxial layer has a substantially uniform thickness. This is due to the uniformity of the buried layer, which is in turn due to the uniform concentration of ions achieved during ion implantation.

The foregoing and other structures and teachings of the present invention will become more apparent upon a detailed description of the best mode for carrying out the invention as rendered below. In the description to follow, reference will be made to the accompanying drawing, in which:

Fig. 1 is a cross-sectional view of a silicon substrate having an epitaxial layer and a buried etch stop layer;

Fig. 2 is a cross-sectional view of the substrate of Fig. 1 bonded to a mechanical support utilizing a first bonding technique;

Fig. 3 is a cross-sectional view of the substrate of Fig. 1 bonded to a mechanical support substrate utilizing a second bonding technique;

Fig. 4 is a cross-sectional view of the substrate of Fig. 1 bonded to a mechanical support substrate utilizing a third bonding technique;

Fig. 5 is a cross-sectional view of the mechanical support substrate with the first substrate removed; and

Fig. 6 is a cross-sectional view of the second substrate as shown in Fig. 5 with the overlaying portions of the epitaxial layer and the buried etch stop layer removed.

As shown in Fig. 1, an n- epitaxial layer 12 is formed on a p+ or N+ 0.008 ohm/cm silicon wafer 10. The epitaxial layer 12 is grown using conventional deposition gases such as SiH_2C1_2, SiH_4, $SiC1_4$ or $SiHC1_3$. Preferably, SiH_2C1_2 is used at 1050-1080°C. The resulting epitaxial layer can be relatively thick (e.g. 2500nm). This is because the initial thickness of the epitaxial layer has minimal bearing upon the final thickness of the silicon-on-insulator structure, as will be described in more detail below. Note that the dopant concentration of substrate 10 should be 6 $X10^{18}$ ions/cm^3 or greater, 1 X 10^{19} being a typical choice. Such a concentration is necessary for this substrate to be etched in HNA. When the epitaxial layer 12 is formed on substrate 10, boron will outdiffuse from the substrate such that a p+/n-junction will be established within epitaxial layer 12. The boron atoms penetrate into the epitaxy to form the junction at approximately 400-800nm above the physical epitaxy - substrate interface.

A buried etch-stop layer 14 is then formed within epitaxial layer 12, separating epitaxial layer 12 into a first portion 12A overlaying the etch-stop 14 and a second portion 12B laying beneath the etch-stop 14. In general, buried layer 14 can be comprised of any element which has etch characteristics that are appreciably different from those of the epitaxial layer 12. For example, buried layer 14 can be formed implanting oxygen ions at a dose of 1 x 10^{15} - 1 x 10^{18} 0+ ions/cm^2 at 160 kev into the substrate, with the substrate being heated to approximately 500°C. The substrate is heated during implantation in order to minimize damage in the portion 12A of epitaxial layer 12 overlaying the buried ions. If oxygen ions are implanted, a buried layer of silicon oxide is formed. Note that nitrogen ions could also be used to form a buried layer of silicon nitride. In addition, carbon ions could be implanted to form a buried layer of silicon carbide. The dosage is one factor determining the "effectiveness" of the etch-stop. Specifically, the higher the dosage, the more effective the etch stop and hence the more planar the resulting epitaxial layer upon subsequent etching. This property will be discussed in more detail later. As the dosage increases, a thinner portion of region 12A is left free of defects. Doses of 4 X 10^{15} ions/cm^2 and 1 x 10^{17} ions/cm^2 have produced good results, with the latter being preferred. Finally, the implantation energy also affects the position of the ions within epitaxial layer 12. In general, implantation energies of 80 kev and up (160 kev being preferred) can be used.

Since buried layer 14 is formed by implanta-

tion, it has a thickness which is substantially uniform due to the minimal deviation of the implant energy. In addition, layer 14 is relatively planar (i.e. the upper surface of layer 14 is buried below the exposed surface of the epi layer at the same depth across the entire wafer).

Any one of a number of known bonding techniques can be used to bond substrate 10 to a "mechanical" (i.e. physical support) wafer 100. In a preferred bonding technique as shown in Fig. 2, a layer of silicon dioxide 16A is grown on epitaxial portion 12A. The thickness of this oxide layer 16A can vary in the range of approximately 1-200 nm, with the upper limit being the amount of epitaxial portion 12A consumed during oxide growth. Preferably, SiO_2 16A is 45 nm in thickness, and is grown in an oxygen ambient at approximately 800°C. Alternatively, SiO_2 may be pyrolytically deposited upon epitaxial portion 12A, eliminating silicon consumption. In either case, the oxide layer 16A is then bonded to the mechanical wafer 100 by contact in a steam ambient and heating to a temperature within the range of 700-1200°C (preferably 900°C) for approximately 50 minutes.

In another bonding technique as shown in Fig. 3, an oxide layer 16B of any thickness (e.g. up to 2000 nm) is grown on mechanical substrate 100 prior to bonding. Thus, the oxide layers 16A and 16B bond together, forming a very thick oxide layer. Such a thick oxide may be advantageous in high voltage applications.

In yet another technique as shown in Fig. 4, a reflowable glass such as borosilicate glass (BSG) or boro-phosphosilicate glass (BPSG) layer 18 is used instead of silicon dioxide. When the glass is deposited on epitaxial portion 12A, it is advisable to first deposit a 5-100 nm(typically 20 nm) thick layer of silicon nitride 20. The nitride will prevent out-diffusion of impurities from the glass into epitaxial portion 12A during subsequent high temperature processing. Note that when bonding takes place, the bonding temperature must be above the glass transition temperature. For example, using a 4:4:92 BPSG layer of 0.4μm thickness, bonding is carried out in a steam atmosphere at approximately 900°C. Alternatively, a layer of reflowable glass could also be formed on the mechanical substrate 100.

After any of the above bonding operations, p+ substrate 10 is removed to expose epitaxial portion 12B. The resulting structure is shown in Fig. 5. One removal method is to grind or lap (or otherwise mechanically remove) a substantial portion of substrate 10, mechanically polish the surface in order to remove scratches, and then etch the remaining portions of substrate 10 in a 1:3:8 solution of hydroflouric, nitric and acetic acids (HNA) plus a small amount of hydrogen peroxide. The HNA etchant will remove the remainder of substrate 10, as well as the region of epitaxial portion 12B overlaying the n- epi/p+ substrate junction produced by the out-diffusion of boron from substrate 10 into epitaxial layer 12. It has been found that by ultrasonically agitating the HNA, the by-products of the etch can be removed more efficiently, enhancing the etch selectivity (i.e. etching will cease at the p+/n- junction). With starting thicknesses of 2500 nm for the epitaxial layer 12 and 45 nm for oxide layer 16A, the combined thickness of layers 12A, 12B and 16A is typically 2200± 200 nm after HNA etching. Substrate 10 is initially mechanically removed in order to reduce total processing time. That is, an alternative to the first removal method is to cover the exposed surfaces of both of the substrates with a thermal silicon dioxide layer, and to remove the thermal silicon dioxide layer from substrate 10 using an etchant such as hydroflouric acid. The substrate 10 is then removed using an etch which has a high etch rate ratio of silicon to silicon dioxide. An example of such an etchant is ethylene-diamine-pyrocatechol (EDP). Thus, the oxide layer atop mechanical substrate 100 protects it during EDP etching of substrate 10, thus eliminating the need for the mechanical removing step.

The remainder of epitaxial layer 12B is then removed using an etchant which has a high selectivity of silicon to silicon oxide (or silicon to silicon nitride, in the case where the etch-stop is comprised of silicon nitride). Preferably, this etch is carried out using ethylene-piperidine-pyrocatechol (EPP) at 70°-130°C. The inventors have determined that by using EPP, a 6 μm (micron) etch-stop "effectiveness" can be achieved with a buried oxide layer 14 having a oxygen ion concentration of 1×10^{17} ion/cm^3. The "effectiveness" of the etch-stop can be explained as follows. Assume for the moment that after HNA etching the remaining region of epitaxial portion 12B has a thickness which varies up to 6 microns. When EPP etching is completed, this variation is eliminated, such that a uniform thickness of the etch-stop layer 14 remains. This improvement in planarity is yet another of the advantages of using an implanted etch-stop as in the invention.

Other etchants could be used to remove the epitaxial portion 12B. One such etchant is 3 molar potassium hydroxide (KOH) heated to 35°-50°C. However, tests have shown that when using this etchant, an oxide layer having a concentration of 1×10^{17} oxygen ions/cm^3 achieves an effectiveness of only 1 μm (micron). Therefore, EPP (as well as similar etchants such as ethylene-diamine-pyrocatechol) is preferable to KOH, given the dopant oxygen (or nitrogen) ion concentrations mentioned previously.

Then, etch-stop 14 is removed. Any etchant

which has a high etch rate ratio of silicon oxide to silicon could be used. Alternatively, the layer may be etched in a non-selective etch such as CF_4 + O_2 plasma.

The final structure is shown in Fig. 6. The remaining portion of the epitaxial layer 12 is substantially planar, and thus is of a substantially uniform thickness. As previously noted, this is due to the uniform distribution achieved by the oxygen ions during the implantation to form the buried etch-stop layer 14. If it is desired to reduce the thickness of 12A further, this may be done by oxidation and subsequent etching in BHF. Measurements have shown that the thickness of the remaining portion of epitaxial layer 12 is approximately 350± 4nm, which is quite an improvement over the 250± 150nm achieved with an initial epitaxial thickness of 2500nm and the methods of the prior art as discussed previously. If needed, the remaining epitaxial layer may be oxidized and etched, or directly etched, in order to remove any residual oxide left over from etch-stop 14.

An alternate embodiment of present invention is to form the etch-stop 14 by implanting boron ions into the epitaxy. An n- epitaxial layer is formed on a p+ substrate as in the first embodiment above. Prior to boron implantation, an oxide layer (typically 500 nm thick) is grown on the epi, in order to minimize thermal processing after implantation is done. Then boron ions at a dose of 6 x 10^{14} ions/cm^2 at 2.0 Mev are implanted through the oxide to form a buried boron etch-stop layer. A mechanical substrate is then bonded to the oxide, and the first substrate is removed in ultrasonically agitated HNA, as in the first embodiment. Then the epitaxy is etched in 3 molar KOH at approximately 50°C, to the point where the peak boron concentration in the implanted etch-stop is reached. Finally, the remainder of the etch-stop is removed using HNA. That is, since the peak boron concentration is above that needed to initiate HNA etching (i.e. 4 x 10^{18} ions/cm^3), HNA etching can be initiated. Once initiated, it can be continued to remove the remainder of the etch-stop even though the boron concentration falls below this critical concentration. Note that the distance of this second etch-stop from the thermally grown oxide is formed by ion implantation and hence is substantially uniform.

Both embodiments of the invention as described above result in a thin, uniformly thick silicon layer above an insulator. The final thickness of this layer is independent of the thickness of the epitaxial layer as initially grown.

Claims

1. A method of forming a thin semiconductor layer of substantially uniform thickness upon which semiconductor structures may be subsequently formed, comprising the steps of:
   - growing an epitaxial silicon layer (12) of a second conductivity type upon a silicon substrate (10) of a first conductivity type;
   - implanting ions into said epitaxial layer (12) in order to form a substantially planar buried layer (14) of substantially uniform thickness therein, said buried layer having etch characteristics which appreciably differ from those of said epitaxial layer (12);
   - bonding said epitaxial layer (12) to a support substrate (100);
   - removing said silicon substrate (10) and the adjacent portion of said epitaxial layer in a first etchant which attacks silicon of said first conductivity type while not appreciably attacking silicon of said second conductivity type;
   - etching remaining portions of said epitaxial layer overlaying said buried layer (14) in a second etchant which does not appreciably attack underlaying portions of said buried layer (14); and
   - etching said buried layer (14) in a third etchant which does riot appreciably attack underlaying portions (12A) of said epitaxial layer, said underlaying portions (12A) of said epitaxial layer remaining on said support substrate (100) to form the thin semiconductor layer.

2. The method as recited in claim 1, wherein a portion of said silicon substrate (10) is mechanically removed before the remaining portion thereof is removed in said first etchant.

3. The method as recited in Claim 1, wherein said step of bonding said epitaxial layer (12) to said support substrate (100) comprises the steps of:

   forming a layer of silicon dioxide (16A) on an exposed surface of said epitaxial silicon layer (12);

   bringing said layer of silicon dioxide (16A) and said support substrate (100) into contact; and

   heating said silicon dioxide layer (16A) and said support substrate (100) in order to form a bond therebetween.

4. The method as recited in Claim 3, wherein a second layer of silicon dioxide (16B) is grown on said support substrate (100), such that said silicon dioxide layer (16A) formed on said epitaxial silicon layer (12) contacts said second

which has a high etch rate ratio of silicon oxide to silicon could be used. Alternatively, the layer may be etched in a non-selective etch such as CF_4 + O_2 plasma.

The final structure is shown in Fig. 6. The remaining portion of the epitaxial layer 12 is substantially planar, and thus is of a substantially uniform thickness. As previously noted, this is due to the uniform distribution achieved by the oxygen ions during the implantation to form the buried etch-stop layer 14. If it is desired to reduce the thickness of 12A further, this may be done by oxidation and subsequent etching in BHF. Measurements have shown that the thickness of the remaining portion of epitaxial layer 12 is approximately 350± 4nm, which is quite an improvement over the 250± 150nm achieved with an initial epitaxial thickness of 2500nm and the methods of the prior art as discussed previously. If needed, the remaining epitaxial layer may be oxidized and etched, or directly etched, in order to remove any residual oxide left over from etch-stop 14.

An alternate embodiment of present invention is to form the etch-stop 14 by implanting boron ions into the epitaxy. An n- epitaxial layer is formed on a p+ substrate as in the first embodiment above. Prior to boron implantation, an oxide layer (typically 500 nm thick) is grown on the epi, in order to minimize thermal processing after implantation is done. Then boron ions at a dose of 6 x 10^{14} ions/cm^2 at 2.0 Mev are implanted through the oxide to form a buried boron etch-stop layer. A mechanical substrate is then bonded to the oxide, and the first substrate is removed in ultrasonically agitated HNA, as in the first embodiment. Then the epitaxy is etched in 3 molar KOH at approximately 50°C, to the point where the peak boron concentration in the implanted etch-stop is reached. Finally, the remainder of the etch-stop is removed using HNA. That is, since the peak boron concentration is above that needed to initiate HNA etching (i.e. 4 x 10^{18} ions/cm^3), HNA etching can be initiated. Once initiated, it can be continued to remove the remainder of the etch-stop even though the boron concentration falls below this critical concentration. Note that the distance of this second etch-stop from the thermally grown oxide is formed by ion implantation and hence is substantially uniform.

Both embodiments of the invention as described above result in a thin, uniformly thick silicon layer above an insulator. The final thickness of this layer is independent of the thickness of the epitaxial layer as initially grown.

Claims

1. A method of forming a thin semiconductor layer of substantially uniform thickness upon which semiconductor structures may be subsequently formed, comprising the steps of:
   - growing an epitaxial silicon layer (12) of a second conductivity type upon a silicon substrate (10) of a first conductivity type;
   - implanting ions into said epitaxial layer (12) in order to form a substantially planar buried layer (14) of substantially uniform thickness therein, said buried layer having etch characteristics which appreciably differ from those of said epitaxial layer (12);
   - bonding said epitaxial layer (12) to a support substrate (100);
   - removing said silicon substrate (10) and the adjacent portion of said epitaxial layer in a first etchant which attacks silicon of said first conductivity type while not appreciably attacking silicon of said second conductivity type;
   - etching remaining portions of said epitaxial layer overlaying said buried layer (14) in a second etchant which does not appreciably attack underlaying portions of said buried layer (14); and
   - etching said buried layer (14) in a third etchant which does riot appreciably attack underlaying portions (12A) of said epitaxial layer, said underlaying portions (12A) of said epitaxial layer remaining on said support substrate (100) to form the thin semiconductor layer.

2. The method as recited in claim 1, wherein a portion of said silicon substrate (10) is mechanically removed before the remaining portion thereof is removed in said first etchant.

3. The method as recited in Claim 1, wherein said step of bonding said epitaxial layer (12) to said support substrate (100) comprises the steps of:

   forming a layer of silicon dioxide (16A) on an exposed surface of said epitaxial silicon layer (12);

   bringing said layer of silicon dioxide (16A) and said support substrate (100) into contact; and

   heating said silicon dioxide layer (16A) and said support substrate (100) in order to form a bond therebetween.

4. The method as recited in Claim 3, wherein a second layer of silicon dioxide (16B) is grown on said support substrate (100), such that said silicon dioxide layer (16A) formed on said epitaxial silicon layer (12) contacts said second

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layer (16B) of silicon dioxide during said bonding step.

5. The method as recited in Claim 1, wherein said step of bonding said epitaxial silicon layer (12) to a support substrate (100) comprises the steps of:
forming a layer of silicon nitride (20) on an exposed surface of said epitaxial silicon layer (12);
forming a glass layer (18) on said silicon nitride layer (20);
bringing said glass layer (18) and said support substrate (100) into contact; and
heating said glass layer (18) above its glass transition temperature in order to form a bond to said support substrate (100).

6. The method as recited in Claim 1, wherein said ions comprise oxygen ions which are implanted at a dose within the range of 1×10^{16} - 1×10^{18} ions/cm^2 at an energy of 160 kev, said ions reacting with said epitaxial silicon layer such that said buried layer is comprised of silicon oxide.

7. The method as recited in Claim 1, wherein:
said first etchant comprises a solution of hydroflouric, nitric and acetic acids, and hydrogen peroxide, which is ultrasonically agitated in order to improve selectivity; and
said second etchant comprised a solution selected from the group consisting of ethylenediamine-pyrocatechol acid and ethylenepiperidine-pyrocatechol acid.

Patentansprüche

1. Verfahren zum Ausbilden einer dünnen Halbleiterschicht mit einer im wesentlichen einheitlichen Dicke, auf der nachfolgend Halbleiterstrukturen ausgebildet werden können, welches die folgenden Schritte umfaßt:
Aufwachsen einer epitaktischen Siliziumschicht (12) einer zweiten Leitungsart auf einem Siliziumsubstrat (10) einer ersten Leitungsart,
Implantieren von Ionen in die epitaktische Schicht (12), um darin eine im wesentlichen planare begrabene Schicht (14) mit einer im wesentlichen einheitlichen Dicke auszubilden, wobei die begrabene Schicht Ätzeigenschaften aufweist, die sich von jenen der epitaktischen Schicht (12) beträchtlich unterscheiden,
Bonding der epitaktischen Schicht (12) an ein Trägersubstrat (100),
Entfernen des Siliziumsubstrats (10) und des benachbarten Teils der epitaktischen Schicht in einem ersten Ätzmittel, das Silizium der ersten Leitungsart angreift, wogegen es Silizium der zweiten Leitungsart nicht merklich angreift,
Ätzen verbleibender Teile der, die begrabene Schicht (14) bedeckenden, epitaktischen Schicht in einem zweiten Ätzmittel, das darunterliegende Teile der begrabenen Schicht (14) nicht merklich angreift und,
Ätzen der begrabenen Schicht (14) in einem dritten Ätzmittel, das darunterliegende Teile (12A) der epitaktischen Schicht nicht merklich angreift, wobei die darunterliegenden Teile (12A) der epitaktischen Schicht auf dem Trägersubstrat (100) verbleiben, um die dünne Halbleiterschicht auszubilden.

2. Verfahren nach Anspruch 1, bei welchem ein Teil des Siliziumsubstrats (10) mechanisch entfernt wird, bevor dessen verbleibender Teil in dem ersten Ätzmittel entfernt wird.

3. Verfahren nach Anspruch 1, bei welchem der Schritt des Bondings der epitaktischen Schicht (12) an das Trägersubstrat (100) die folgenden Schritte umfaßt:
Ausbilden einer Schicht aus Siliziumdioxid (16A) auf einer freiliegenden Oberfläche der epitaktischen Siliziumschicht (12),
Bewirken, daß die Schicht (16A) aus Siliziumdioxid und das Trägersubstrat (100) einander berühren und
Erwärmen der Siliziumdioxidschicht (16A) und des Trägersubstrats (100), um eine Bindung zwischen ihnen auszubilden.

4. Verfahren nach Anspruch 3, bei welchem eine zweite Schicht (16B) aus Siliziumdixoid durch Wachstum auf dem Trägersubstrat (100) so gebildet wird, daß die auf der epitaktischen Siliziumschicht (12) gebildete Siliziumdioxidschicht (16A) während des Bonding Schrittes mit der zweiten Schicht (16B) aus Siliziumdioxid in Berührung kommt.

5. Verfahren nach Anspruch 1, bei welchem der Schritt des Bondens der epitaktischen Siliziumschicht (12) an ein Trägersubstrat (100) folgende Schritte umfaßt:
Ausbilden einer Schicht (20) aus Siliziumnitrid auf einer freiliegenden Oberfläche der epitaktischten Siliziumschicht (12),
Ausbilden einer Glasschicht (18) auf der Siliziumnitridschicht (20),
Bewirken, daß die Glasschicht (18) und das Trägersubstrat (100) einander berühren und
Erwärmen der Glasschicht (18) über ihre Glasübergangstemperatur, um eine Bindung an dem Trägersubstrat (100) auszubilden.

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6. Verfahren nach Anspruch 1, bei welchem die Ionen Sauerstoffionen enthalten, die bei einer Dosis innerhalb des Bereichs von 1 x 10^{16} - 1 x 10^{18} Ionen/cm^2 bei einer Energie von 160 keV implantiert werden, wobei die Ionen mit der epitaktischen Siliziumschicht so regieren, daß die begrabene Schicht aus Siliziumoxid besteht.

7. Verfahren nach Anspruch 1, bei welchem:
das erste Ätzmittel eine Lösung von Fluorwasserstoff-, Salpeter- und Essigsäure und Wasserstoffperoxid enthält, die mittels Ultraschalls geschüttelt wird, um die Selektivität zu verbessern und
das zweite Ätzmittel eine Lösung enthält, die aus der Gruppe ausgewählt ist, die aus Ethylen-Diamin-Pyrocatechin-Säure und Ethylen-Piperidin-Pyrocatechin-Säure besteht.

Revendications

1. Procédé pour former une mince couche semi-conductrice d'épaisseur sensiblement uniforme sur laquelle des structures semi-conductrices peuvent être ensuite formées, comprenant les étapes suivantes:
   - développement d'une couche épitaxiale 12 de silicium d'un second type de conductivité sur un substrat de silicium 10 d'un premier type de conductivité;
   - implantations d'ions dans cette couche épitaxiale 12 pour former une couche enfouie 14 pratiquement plane d'épaisseur sensiblement uniforme dans celle-ci, cette couche enfouie ayant des caractéristiques d'attaque qui diffèrent notablement de celles de cette couche épitaxiale 12;
   - liaison de cette couche épitaxiale 12 à un substrat de support 100;
   - élimination de ce substrat de silicium 10 et de la partie adjacente de cette couche épitaxiale dans un premier décapant qui attaque le silicium de ce premier type de conductivité sans attaquer notablement le silicium de ce second type de conductivité;
   - attaque des parties restantes de cette couche épitaxiale recouvrant cette couche enfouie 14 dans un second décapant qui n'attaque pas notablement les parties sous-jacentes de cette couche enfouie 14; et
   - attaque de cette couche enfouie 14 dans un troisième décapant qui n'attaque pas notablement les parties sous-jacentes 12A de cette couche épitaxiale, ces parties sous-jacents 12A de cette couche épitaxiale restant sur ce substrat de support 100 pour former la mince couche semi-conductrice.

2. Procédé suivant la revendication 1, dans lequel une partie de ce substrat de silicium 10 est enlevée mécaniquement avant élimination de la partie restante dans ce premier décapant.

3. Procédé suivant la revendication 1, dans lequel ladite étape de liaison de ladite couche épitaxiale 12 audit substrat de support 100 comprend les étapes suivantes:
   formation d'une couche de dioxyde de silicium 16A sur une surface exposée de cette couche épitaxiale de silicium 12;
   mise en contact de cette couche de dioxyde de silicium 16A et de ce substrat de support 100; et
   chauffage de cette couche de dioxyde de silicium 16A et de ce substrat de support 100 pour former une liaison entre eux.

4. Procédé suivant la revendication 3, dans lequel une seconde couche de dioxyde de silicium 16B est développée sur ce substrat de support 100, de telle sorte que cette couche de dioxyde de silicium 16A formée sur cette couche épitaxiale de silicium 12 soit en contact avec cette seconde couche 16B de dioxyde de silicium pendant cette étape de liaison.

5. Procédé suivant la revendication 1, caractérisé en ce que cette étape de liaison de cette couche épitaxiale de silicium 12 à un substrat de support 100 comprend les étapes suivantes :
   formation d'une couche de nitrure de silicium 20 sur une surface exposée de cette couche épitaxiale de silicium 12;
   formation d'une couche de verre 13 sur cette couche de nitrure de silicium 20;
   mise en contact de cette couche de verre 18 et de ce substrat de support 100; et
   chauffage de cette couche de verre 20 au-delà de sa température de transition vitreuse pour former une liaison avec ce substrat de support 100.

6. Procédé suivant la revendication 1, caractérisé en ce que ces ions comprennent des ions oxygène qui sont implantés à une dose de l'ordre de 1x10^{16} à 1x10^{18} ions/cm^2 à une énergie de 160 kev, ces ions réagissant avec cette couche épitaxiale de silicium si bien que cette couche enfouie est composée d'oxyde de silicium.

* C L M S *

7. Procédé suivant la revendication 1, caractérisé en ce que :

ce premier décapant comprend une solution d'acides fluorhydrique, nitrique et acétique et du peroxyde d'hydrogène, qui est agitée par ultrasons pour améliorer la sélectivité; et que

ce second décapant comprend une solution choisie dans le groupe comprenant l'éthylène-diamine-pyrocatéchol et l'éthylène-pipéridine-pyrocatéchol.

* C L M S *