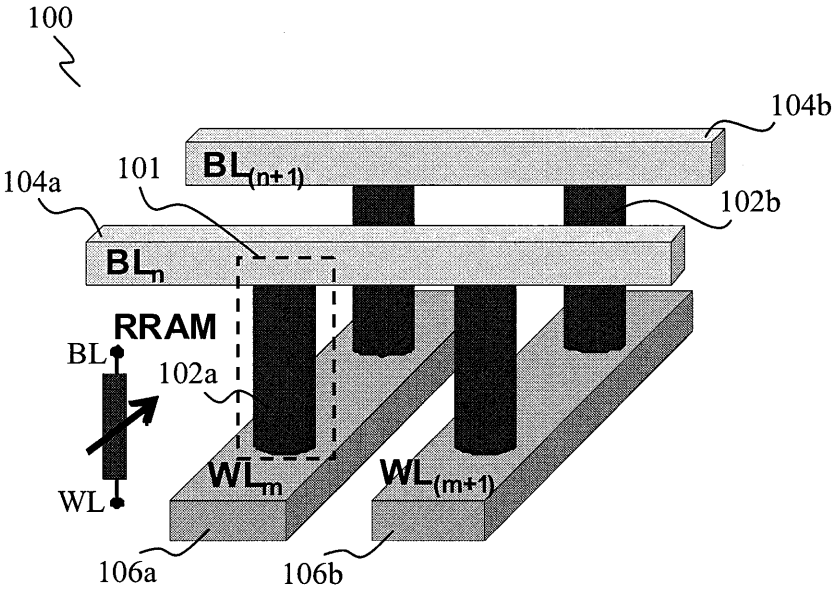

100
104b
101
$BL_{(n+1)}$
104a
102b
BL_n
RRAM
BL
102a
WL
WL_m
$WL_{(m+1)}$
106a
106b

FIG. 1A

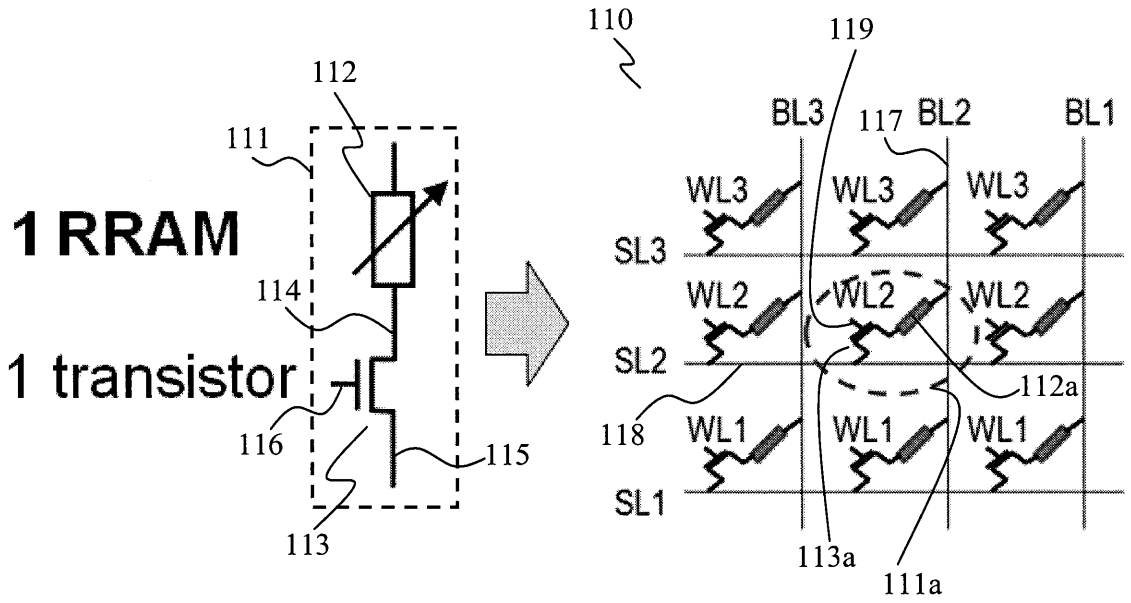

1 RRAM
1 transistor
112
111
114
116
115
113
110
119
BL3
117
BL2
BL1
WL3
WL2
WL1
SL3
SL2
SL1
118
112a
113a
111a

FIG. 1B

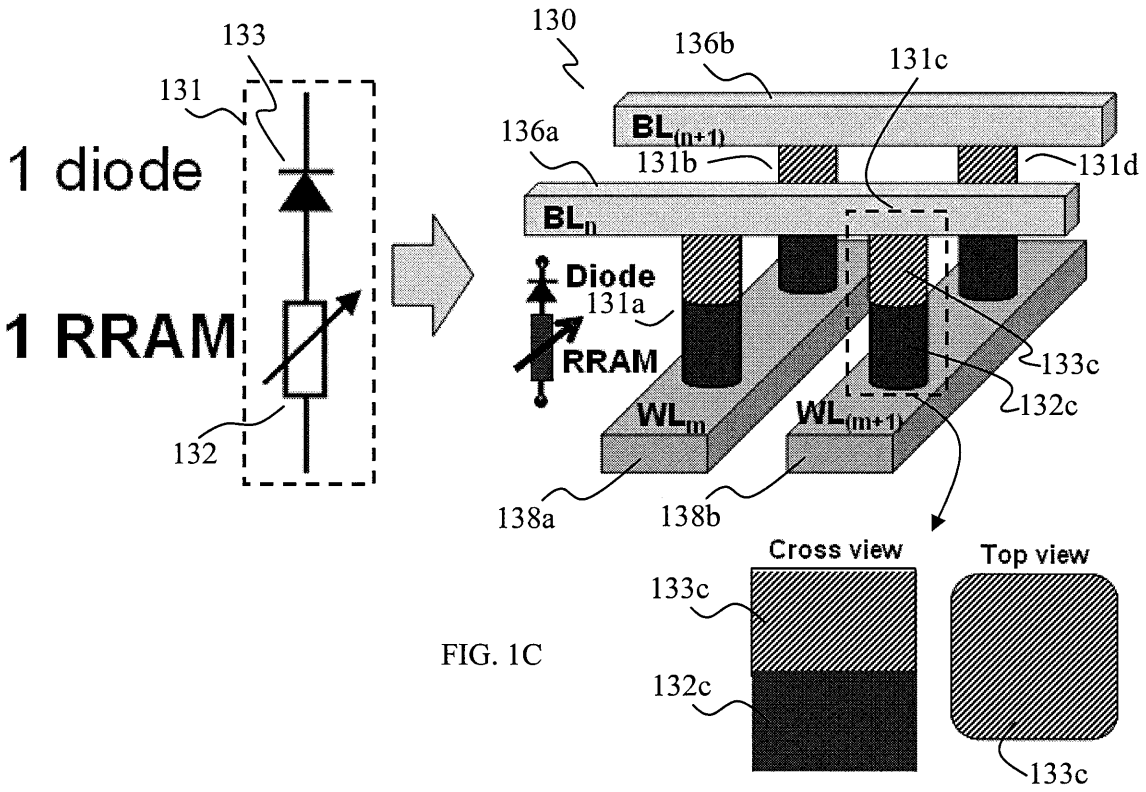


FIG. 1C

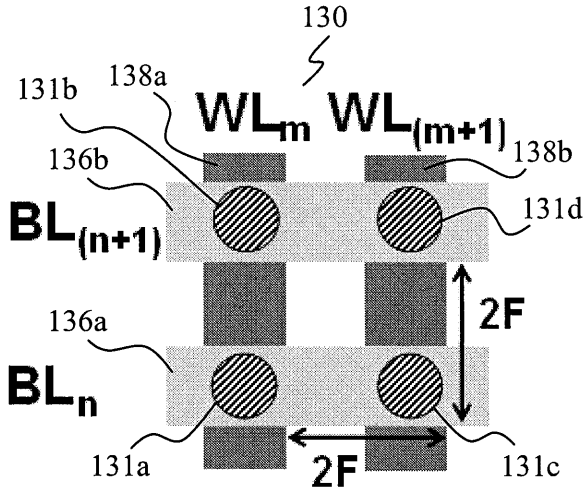


FIG. 1D

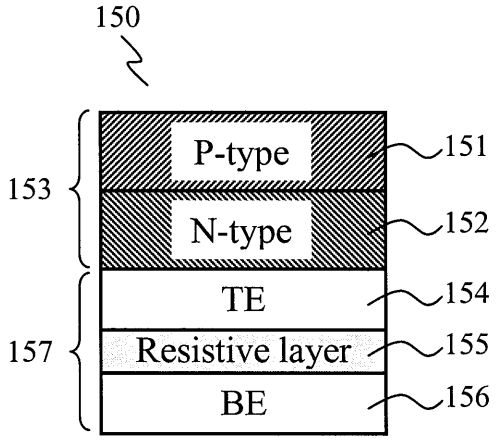


FIG. 1E

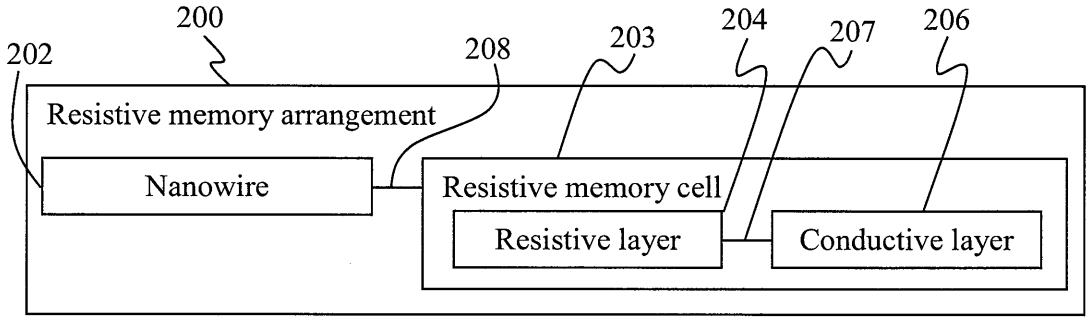


FIG. 2A

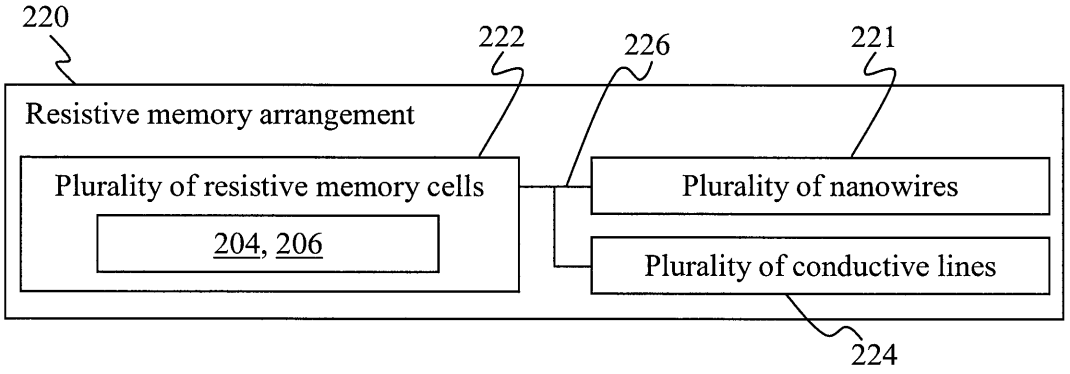


FIG. 2B

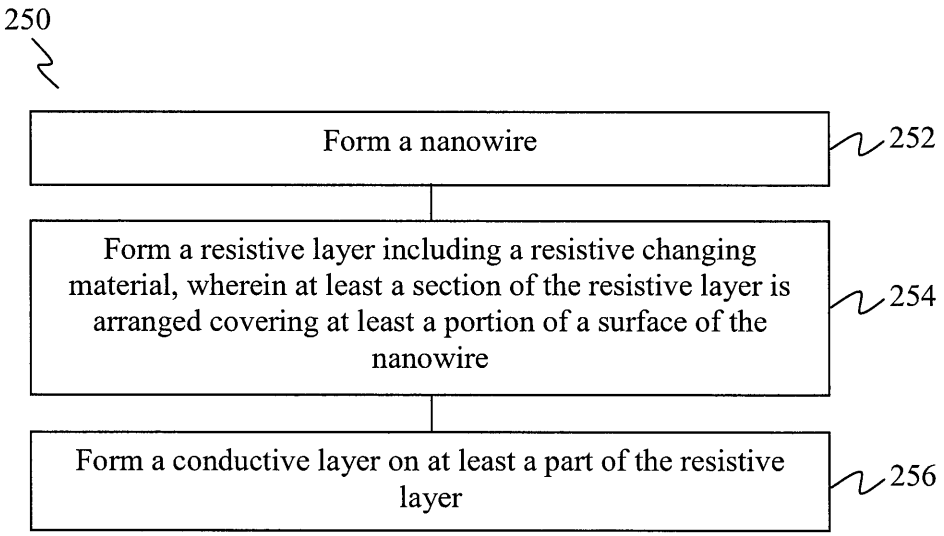


FIG. 2C

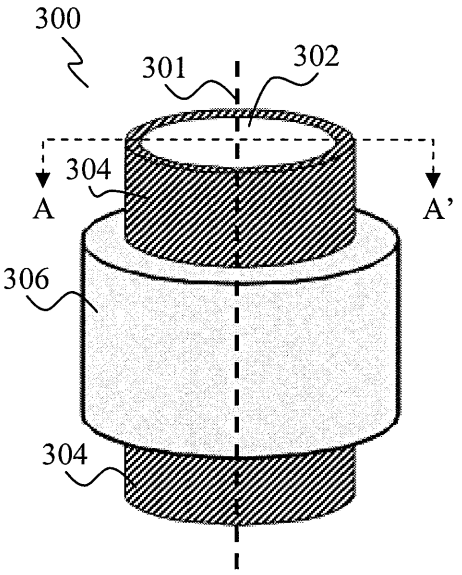


FIG. 3A

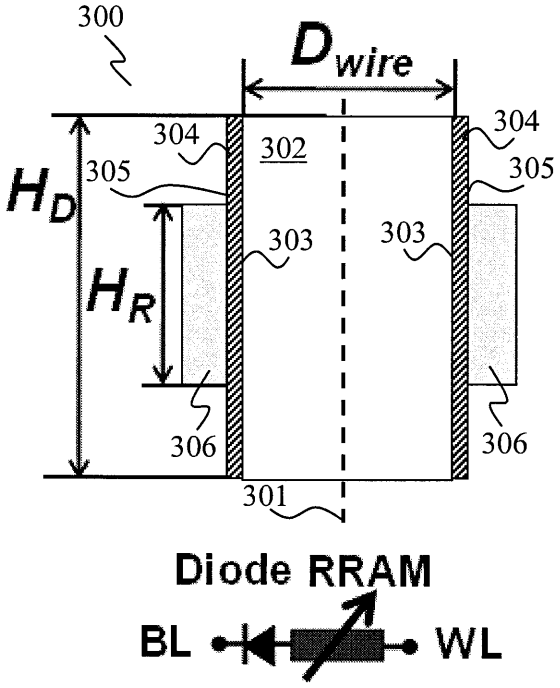


FIG. 3B

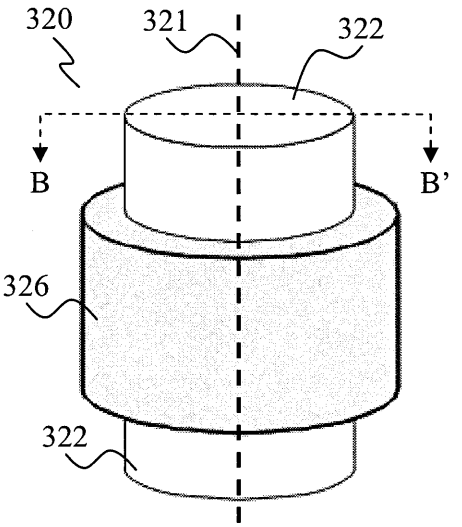


FIG. 3C

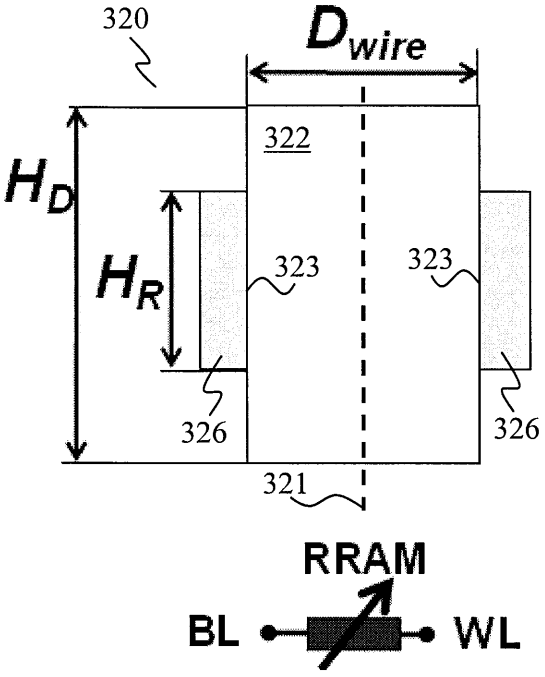


FIG. 3D

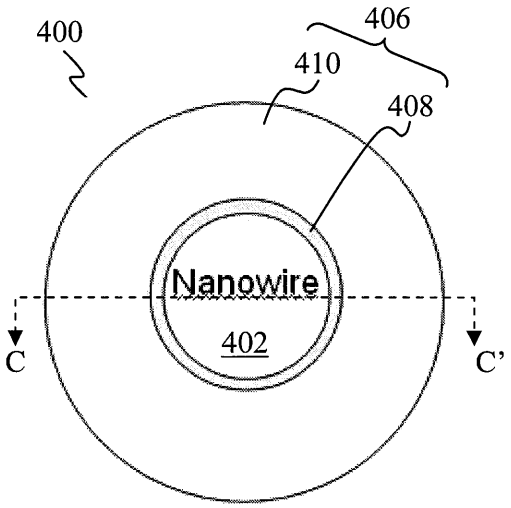


FIG. 4A

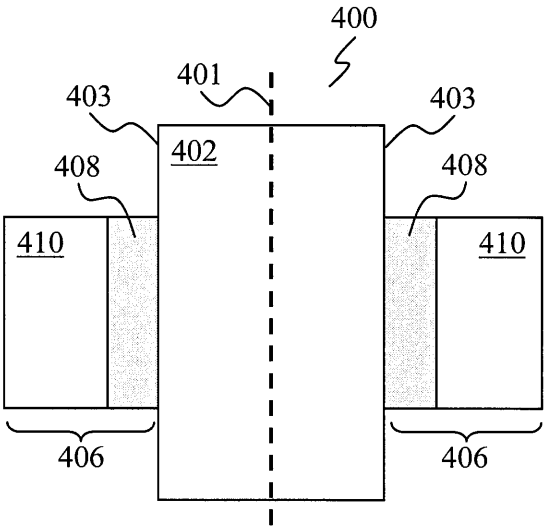


FIG. 4B

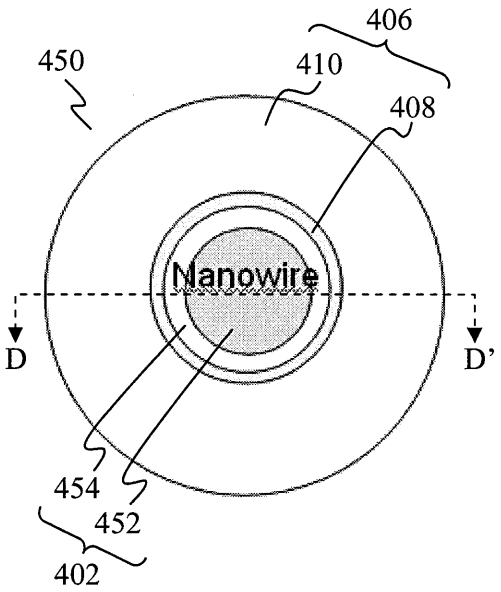


FIG. 4C

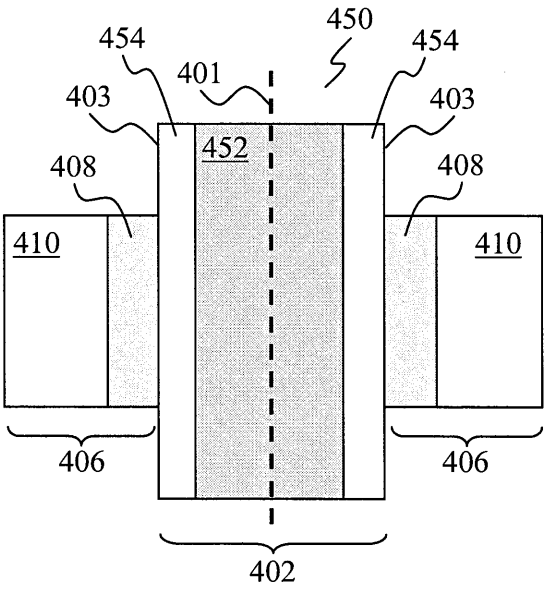


FIG. 4D

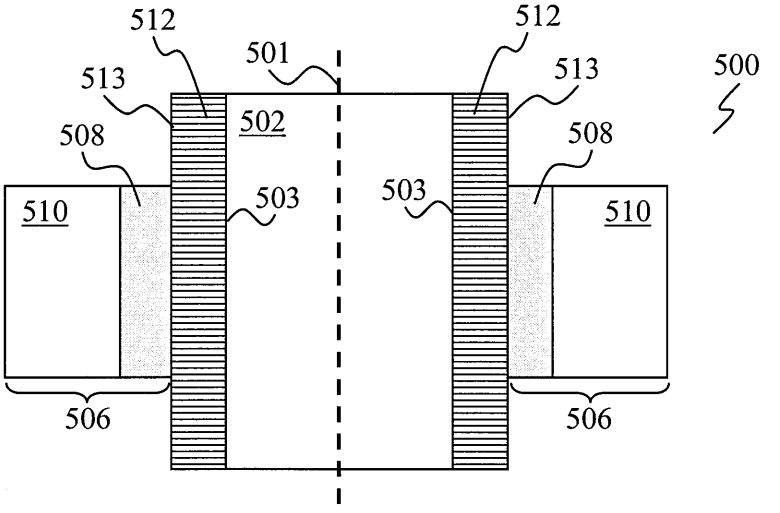


FIG. 5A

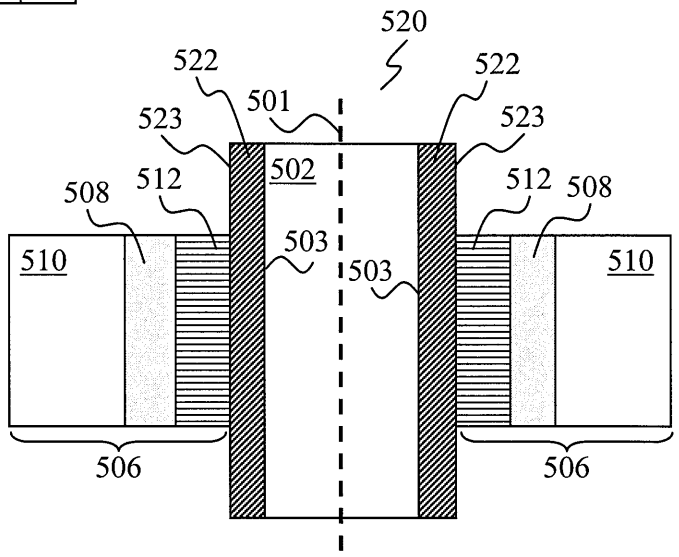


FIG. 5B

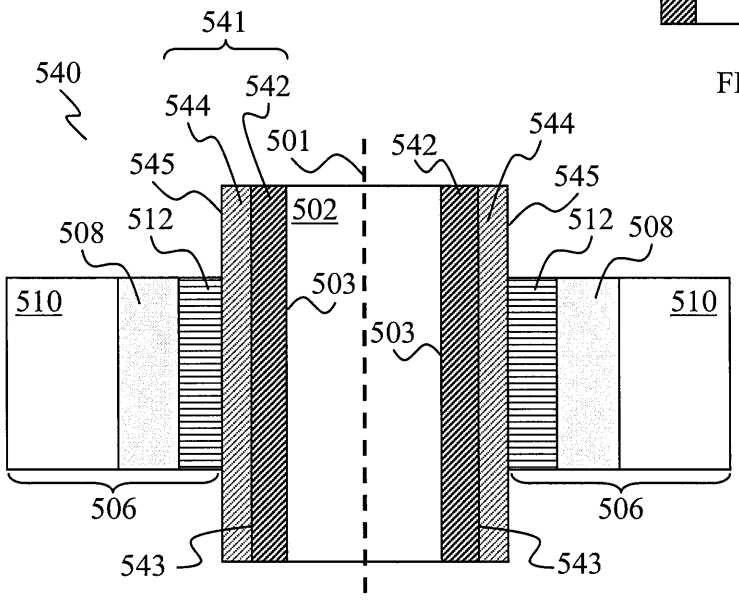


FIG. 5C

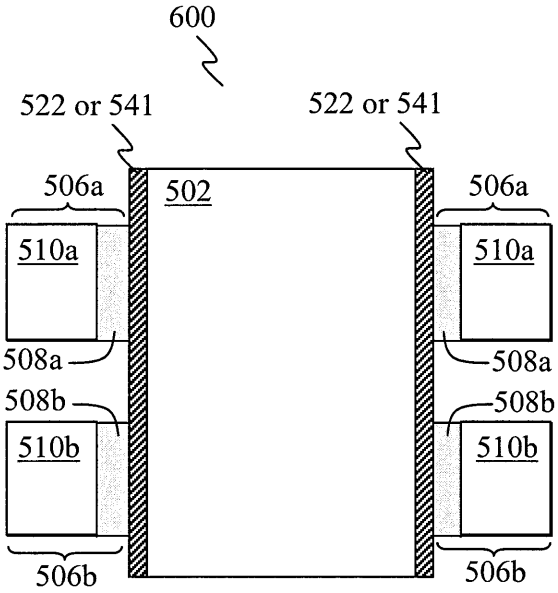


FIG. 6A

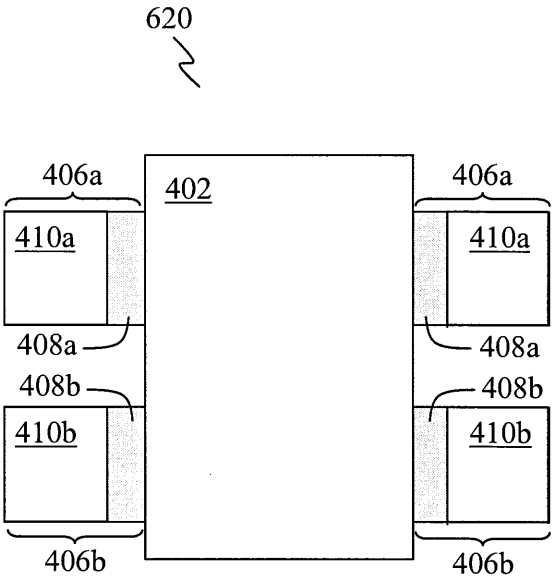
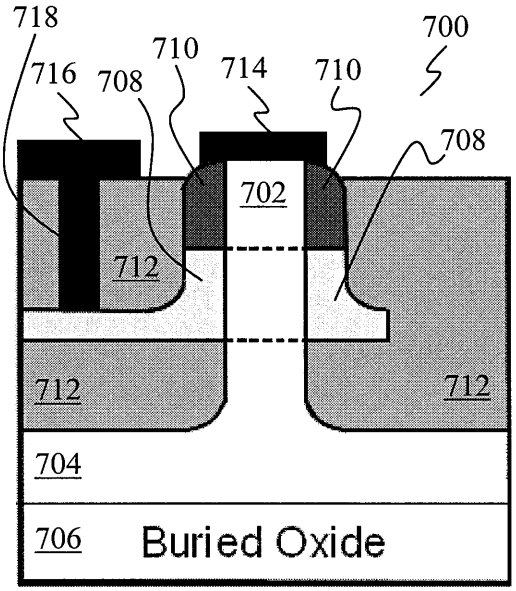
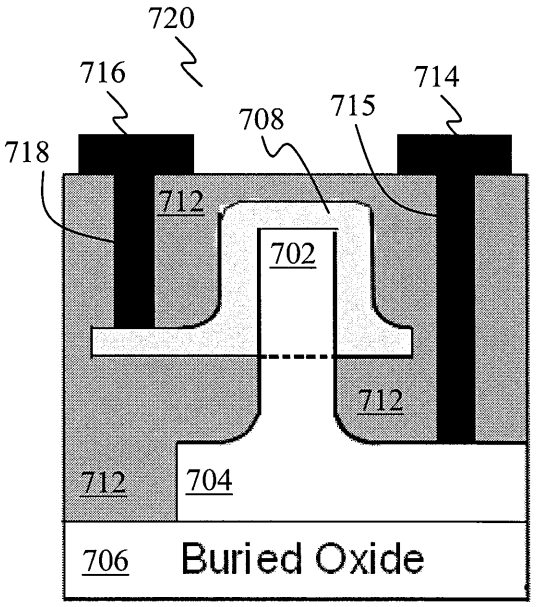


FIG. 6B



from top

FIG. 7A



from bottom

FIG. 7B

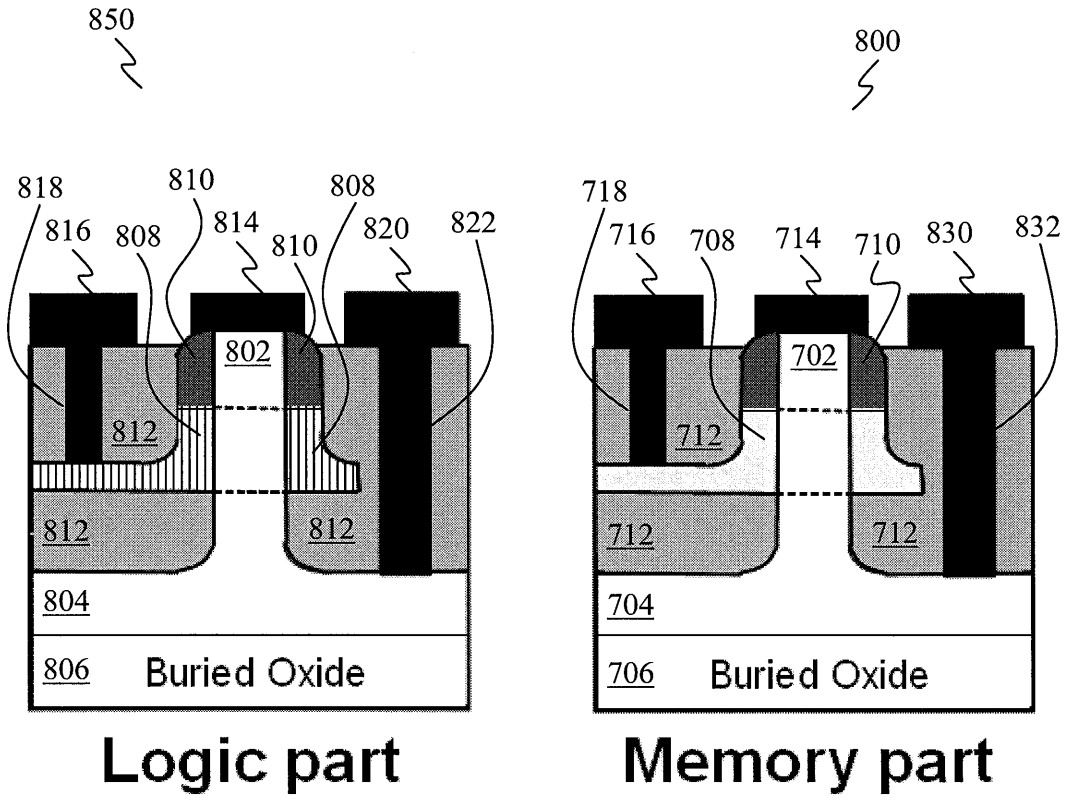

850
800
818
816
808
810
814
808
810
820
822
802
812
812
812
804
806
Buried Oxide
Logic part
718
716
708
714
710
830
832
702
712
712
712
704
706
Buried Oxide
Memory part

FIG. 8

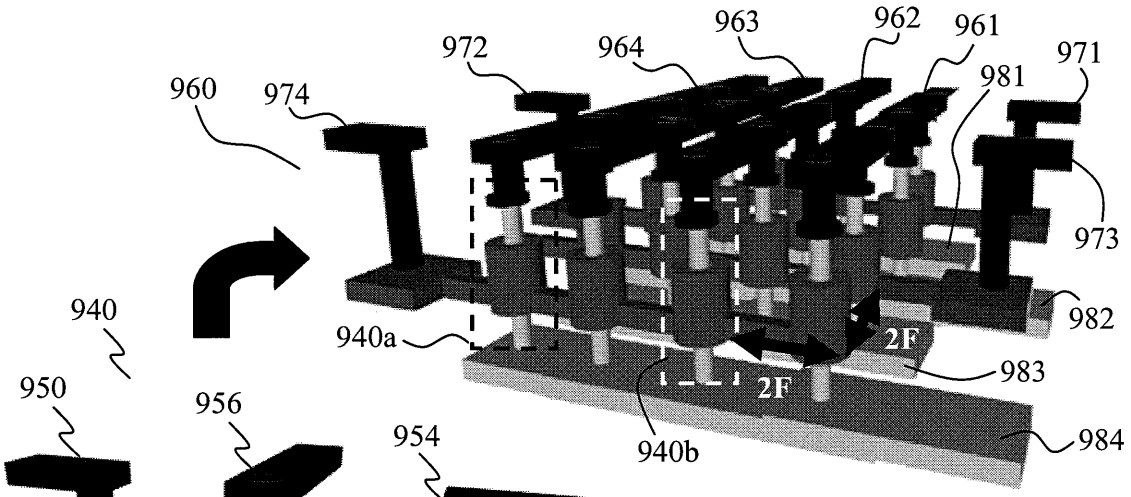


FIG. 9B

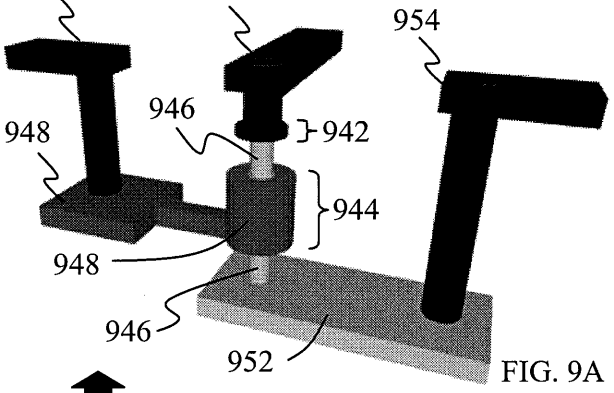


FIG. 9A

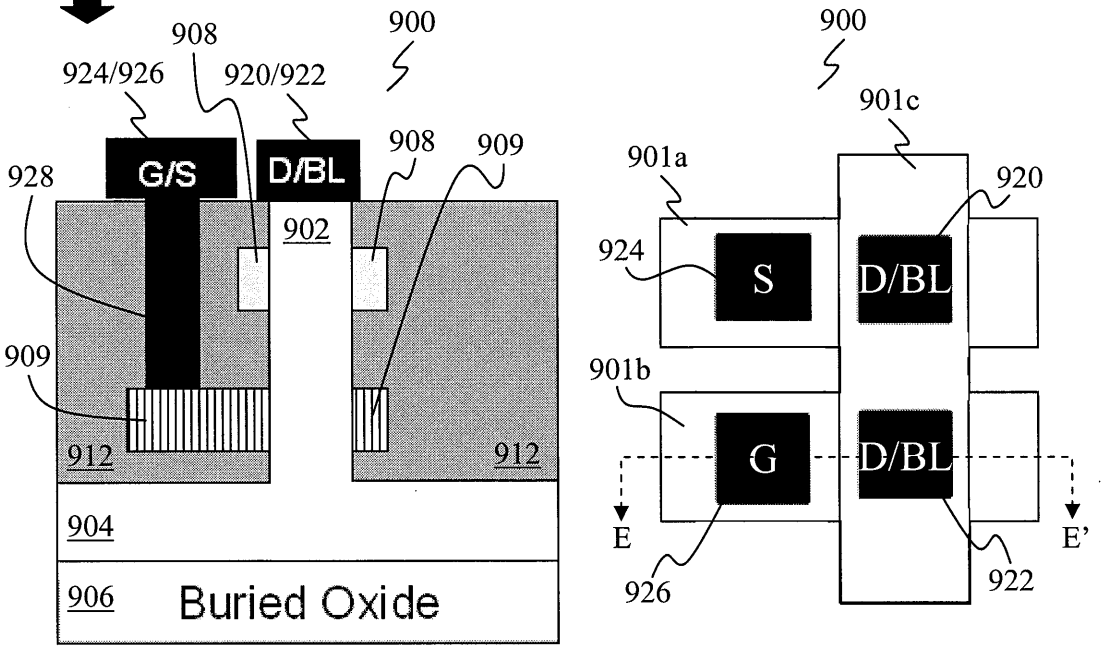


FIG. 9C

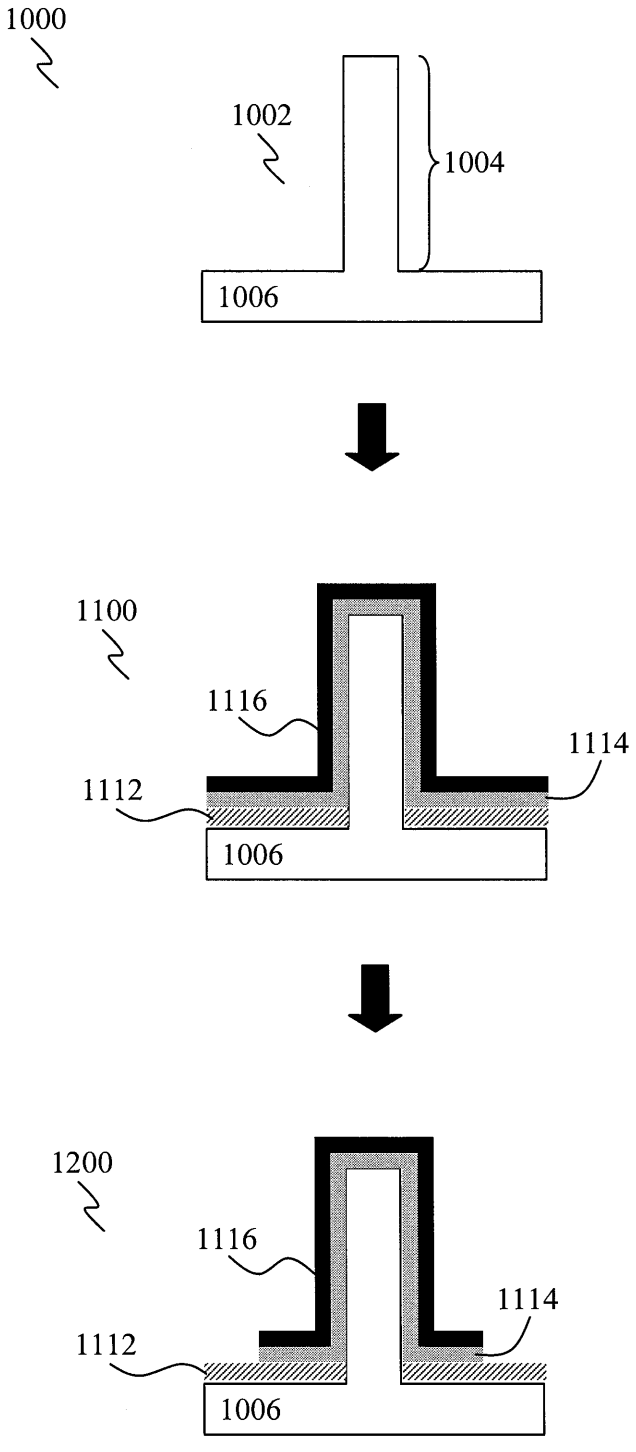

1000
1002
1004
1006
1100
1116
1114
1112
1006
1200
1116
1114
1112
1006

FIG. 10