WHAT IS CLAIMED IS:

1. A semiconductor device comprising:

a core circuit; and

a first IO cell and a second IO cell arranged on a periphery of the core circuit;

wherein each of the first IO cell and the second IO cell comprises:

a power supply terminal to which a power supply voltage is applied;

a ground terminal connected to ground;

an RC delay circuit comprising series connected element of~~including~~ a resistor ~~having one terminal connected to one of the power supply terminal and the ground terminal~~ and a capacitor ~~having one terminal connected to the other terminal of the resistor and the other terminal connected to the other of the power supply terminal and the ground terminal~~;

a P-type transistor; and

an N-type transistor,

in at least one of the first IO cell and the second IO cell, the RC delay circuit is connected between the power supply terminal and the ground terminal, and a connection terminal between the resistor and the capacitor is connected to a gate of at least one transistor of the P-type transistor and the N-type transistor,

when the at least one transistor is the P-type transistor, a source of the P-type transistor is connected to the first power supply terminal, and a drain is connected to the ground terminal, and

when the at least one transistor is the N-type transistor, the drain of the N-type transistor is connected

to the first power supply terminal, and the source is connected to the ground terminal.

2. The device of claim 1, wherein each of the first IO cell and the second IO cell further comprises:

a first buffer having an output terminal connected to the gate of the P-type transistor; and

a second buffer having the output terminal connected to the gate of the N-type transistor,

when the at least one transistor is the P-type transistor, the gate of the P-type transistor is connected to the connection terminal via the first buffer, and

when the at least one transistor is the N-type transistor, the gate of the N-type transistor is connected to the connection terminal via the second buffer.

3. The device of claim 2, wherein each of the first buffer and the second buffer includes an inverter chain including inverters.

4. The device of claim 2, further comprising a level shifter circuit arranged between the core circuit and the first buffer and between the core circuit and the second buffer and configured to shift a signal potential.

5. The device of claim 1, wherein

when the at least one transistor is the P-type transistor, the N-type transistor is a dummy element not being involved in circuit operation, and

when the at least one transistor is the N-type transistor, the P-type transistor is a dummy element not being involved in circuit operation.

6. The device of claim 1, wherein one terminal of the resistor is connected to the first power supply terminal, and the other terminal of the capacitor is connected to the ground terminal.

7. The device of claim 1, wherein the other terminal of the capacitor is connected to the first power supply terminal, and one terminal of the resistor is connected to the ground terminal.

8. A semiconductor device comprising:

a core circuit; and

a first IO cell and a second IO cell arranged on a periphery of the core circuit;

wherein each of the first IO cell and the second IO cell comprises:

a power supply terminal to which a power supply voltage is applied;

a ground terminal connected to ground;

an RC delay circuit comprising series connected element of~~including~~ a resistor ~~having one terminal connected to one of the power supply terminal and the ground terminal~~ and a capacitor~~ having one terminal connected to the other terminal of the resistor and the other terminal connected to the other of the power supply terminal and the ground terminal~~;

a high withstand voltage P-type transistor;

a high withstand voltage N-type transistor;

a low withstand voltage P-type transistor having a lower withstand voltage than the high withstand voltage P-type transistor; and

a low withstand voltage N-type transistor having a lower withstand voltage than the high withstand voltage N-type transistor,

when ~~at least one of~~ the first IO cell and the second IO cell are~~is~~ used as ~~a~~ high withstand voltage types, in at least one of the first IO cell and the second IO cell, the RC delay circuit is connected between the power supply terminal and the ground terminal, and a connection terminal between the resistor and the capacitor is connected to a gate of at least one transistor out of the high withstand voltage P-type transistor and the high withstand voltage N-type transistor,

when ~~at least one of~~ the first IO cell and the second IO cell are~~is~~ used as ~~the~~ high withstand voltage types, and the at least one transistor is the high withstand voltage P-type transistor, a source of the high withstand voltage P-type transistor is connected to the power supply terminal, and a drain is connected to the ground terminal,

when ~~at least one of~~ the first IO cell and the second IO cell are~~is~~ used as ~~the~~ high withstand voltage types, and the at least one transistor is the high withstand voltage N-type transistor, the drain of the high withstand voltage N-type transistor is connected to the power supply terminal, and the source is connected to the ground terminal,

when ~~at least one of~~ the first IO cell and the second IO cell are~~is~~ used as ~~a~~ low withstand voltage types, in at least one of the first IO cell and the second IO cell, the RC delay circuit is connected between the power supply terminal and the ground terminal, and the connection terminal between the resistor and the capacitor is connected to the gate of at least one transistor out of the

low withstand voltage P-type transistor and the low withstand voltage N-type transistor,

when ~~at least one of~~ the first IO cell and the second IO cell are~~is~~ used as ~~the~~ low withstand voltage types, and the at least one transistor is the low withstand voltage P-type transistor, the source of the low withstand voltage P-type transistor is connected to the power supply terminal, and the drain is connected to the ground terminal, and

when ~~at least one of~~ the first IO cell and the second IO cell are~~is~~ used as ~~the~~ low withstand voltage types, and the at least one transistor is the low withstand voltage N-type transistor, the drain of the low withstand voltage N-type transistor is connected to the power supply terminal, and the source is connected to the ground terminal.

9. The device of claim 8, wherein each of the first IO cell and the second IO cell further comprises:

a first buffer having an output terminal connected to the gate of the high withstand voltage P-type transistor;

a second buffer having the output terminal connected to the gate of the high withstand voltage N-type transistor,

a third buffer having the output terminal connected to the gate of the low withstand voltage P-type transistor; and

a fourth buffer having the output terminal connected to the gate of the low withstand voltage N-type transistor,

when at least one of the first IO cell and the second IO cell is used as the high withstand voltage type, and the at least one transistor is the high withstand voltage P-type transistor, the gate of the high withstand P-type transistor is connected to the connection terminal via the first buffer,

when at least one of the first IO cell and the second IO cell is used as the high withstand voltage type, and the at least one transistor is the high withstand voltage N-type transistor, the gate of the high withstand N-type transistor is connected to the connection terminal via the second buffer,

when at least one of the first IO cell and the second IO cell is used as the low withstand voltage type, and the at least one transistor is the low withstand voltage P-type transistor, the gate of the low withstand P-type transistor is connected to the connection terminal via the third buffer, and

when at least one of the first IO cell and the second IO cell is used as the low withstand voltage type, and the at least one transistor is the low withstand voltage N-type transistor, the gate of the low withstand N-type transistor is connected to the connection terminal via the fourth buffer.

10. The device of claim 9, wherein each of the first buffer, the second buffer, the third buffer, and the fourth buffer includes an inverter chain including inverters.

11. The device of claim 9, further comprising a level shifter circuit arranged between the core circuit and the first buffer, between the core circuit and the second buffer, between the core circuit and the third buffer and between the core circuit and the forth buffer and configured to shift a signal potential.

12. The device of claim 8, wherein

when at least one of the first IO cell and the second IO cell is used as the high withstand voltage type, and the

at least one transistor is the high withstand voltage P-type transistor, the high withstand voltage N-type transistor, the low withstand voltage P-type transistor, and the low withstand voltage N-type transistor are dummy elements not being involved in circuit operation,

when at least one of the first IO cell and the second IO cell is used as the high withstand voltage type, and the at least one transistor is the high withstand voltage N-type transistor, the high withstand voltage P-type transistor, the low withstand voltage P-type transistor, and the low withstand voltage N-type transistor are dummy elements not being involved in circuit operation,

when at least one of the first IO cell and the second IO cell is used as the low withstand voltage type, and the at least one transistor is the low withstand voltage P-type transistor, the low withstand voltage N-type transistor, the high withstand voltage P-type transistor, and the high withstand voltage N-type transistor are dummy elements not being involved in circuit operation, and

when at least one of the first IO cell and the second IO cell is used as the low withstand voltage type, and the at least one transistor is the low withstand voltage N-type transistor, the low withstand voltage P-type transistor, the high withstand voltage P-type transistor, and the high withstand voltage N-type transistor are dummy elements not being involved in circuit operation.

13. The device of claim 8, wherein one terminal of the resistor is connected to the power supply terminal, and the other terminal of the capacitor is connected to the ground terminal.

14. The device of claim 8, wherein the other terminal of the capacitor is connected to the power supply terminal, and one terminal of the resistor is connected to the ground terminal.

15. A semiconductor device comprising:

a core circuit; and

a first IO cell, ~~and~~ a second IO cell and a third IO cell arranged on a periphery of the core circuit;

wherein each of the first IO cell, ~~and~~ the second IO cell and the third IO cell comprises:

a first power supply terminal to which a power supply voltage is applied;

a second power supply terminal to which a power supply voltage different from that of the first power supply terminal is applied;

a ground terminal connected to ground;

an RC delay circuit comprising series connected element of~~including a first terminal, second terminal,~~ a resistor ~~having one terminal connected to one of the first terminal and the second terminal~~ and a capacitor ~~having one terminal connected to the other terminal of the resistor and the other terminal connected to the other of the first terminal and the second terminal~~;

a P-type transistor; and

an N-type transistor,

~~one of the first terminal and the second terminal is connected to one of the first power supply terminal and the second power supply terminal and the other of the first terminal and the second terminal is connected to the ground terminal,~~

in at least one of the first IO cell, the second IO cell and the third IO cell, the RC delay circuit~~one of the~~

~~first terminal and the second terminal~~ is connected between~~to~~ the ~~first~~ power supply terminal and the ground terminal, and a connection terminal between the resistor and the capacitor is connected to a gate of at least one transistor of the P-type transistor and the N-type transistor via the wiring layer,

in the first IO cell, when the at least one transistor is the P-type transistor, a source of the P-type transistor is connected to the first power supply terminal, and a drain is connected to the ground terminal,

in the first IO cell, when the at least one transistor is the N-type transistor, the drain of the N-type transistor is connected to the first power supply terminal, and the source is connected to the ground terminal.

in at least one of the first IO cell, the second IO cell and the third IO cell, the RC delay circuit~~one of the first terminal and the second terminal~~ is connected between~~to~~ the ~~second~~ power supply terminal and the ground terminal, and the connection terminal between the resistor and the capacitor is connected to the gate of at least one transistor of the P-type transistor and the N-type transistor via the wiring layer,

in the second IO cell, when the at least one transistor is the P-type transistor, the source of the P-type transistor is connected to the second power supply terminal, and the drain is connected to the ground terminal,

in the second IO cell, when the at least one transistor is the N-type transistor, the drain of the N-type transistor is connected to the second power supply terminal, and the source is connected to the ground terminal.

16. The device of claim 15, wherein each of the first IO cell and the second IO cell further comprises:

a first buffer having an output terminal connected to the gate of the P-type transistor; and

a second buffer having the output terminal connected to the gate of the N-type transistor,

in the first IO cell and the second IO cell, when the at least one transistor is the P-type transistor, the gate of the P-type transistor is connected to the connection terminal via the first buffer, and

in the first IO cell and the second IO cell, when the at least one transistor is the N-type transistor, the gate of the N-type transistor is connected to the connection terminal via the second buffer.

17. The device of claim 16, wherein each of the first buffer and the second buffer includes an inverter chain including inverters.

18. The device of claim 16, further comprising a level shifter circuit arranged between the core circuit the first buffer and between the core circuit and the second buffer and configured to shift a signal potential.

19. The device of claim 15, wherein

in the first IO cell and the second IO cell, when the at least one transistor is the P-type transistor, the N-type transistor is a dummy element not being involved in circuit operation, and

in the first IO cell and the second IO cell, when the at least one transistor is the N-type transistor, the P-type transistor is a dummy element not being involved in circuit operation.