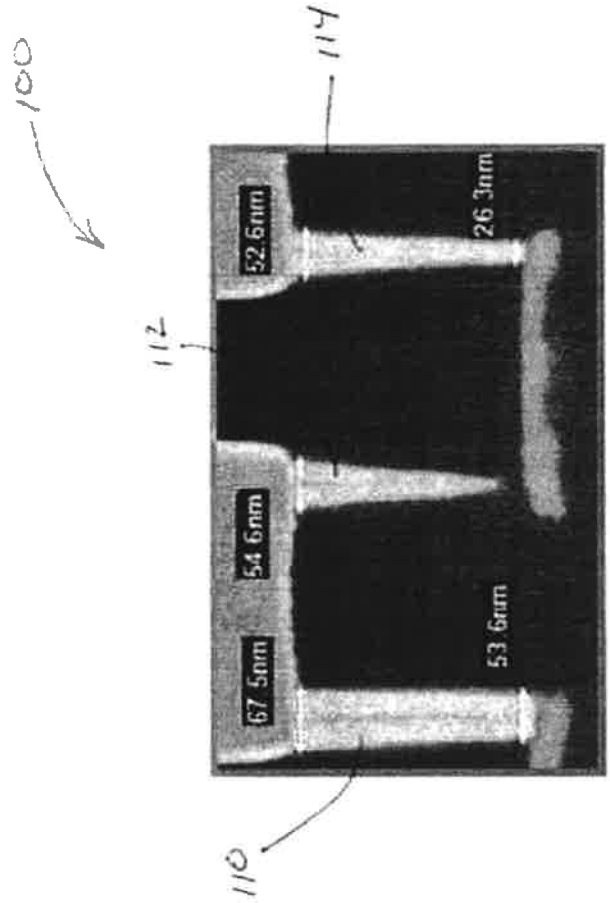

Figure 1

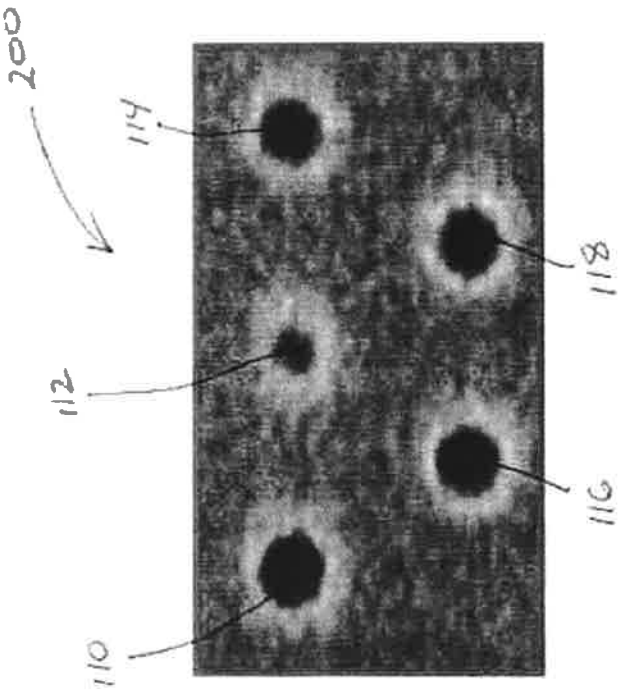

Figure 2

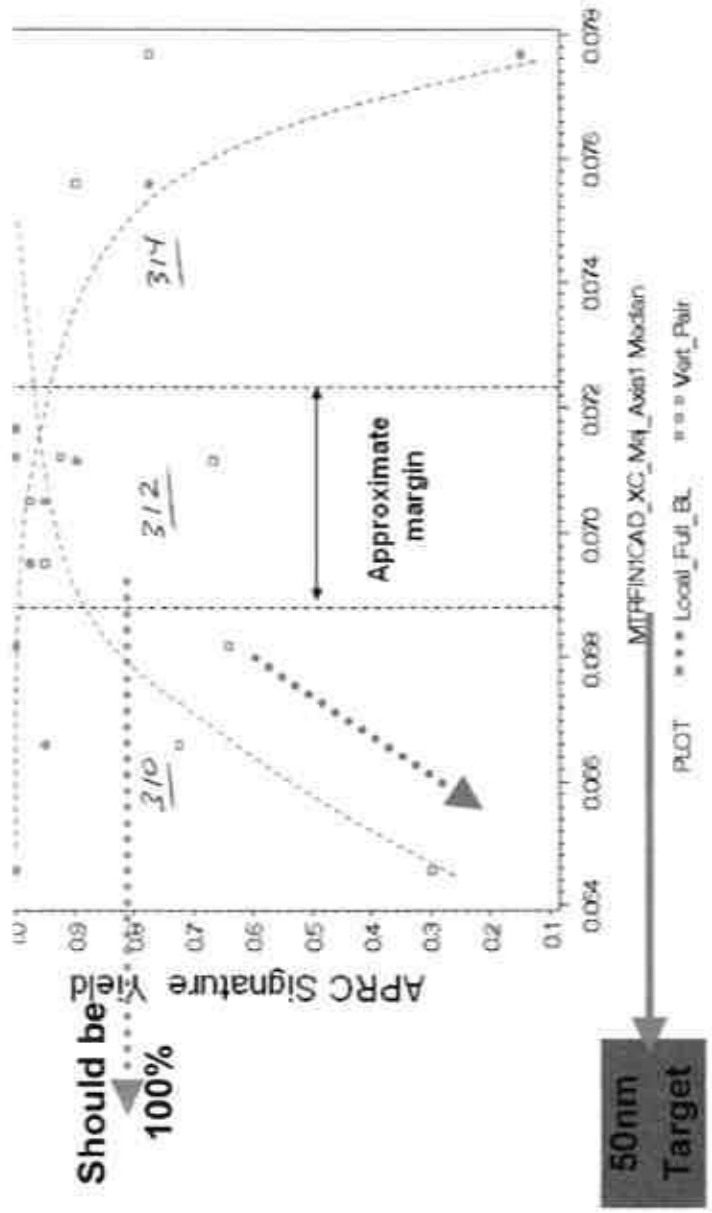
300
310
312
314
Approximate margin
Should be 100%
APRC Signature Yield
1.0
0.9
0.8
0.7
0.6
0.5
0.4
0.3
0.2
0.1
0.064
0.066
0.068
0.070
0.072
0.074
0.076
0.078
MRFINVCAD_XC_Mq_Axis1 Median
PLOT *** Local_Full_BL *** Vert_Pair
50nm Target

Figure 3

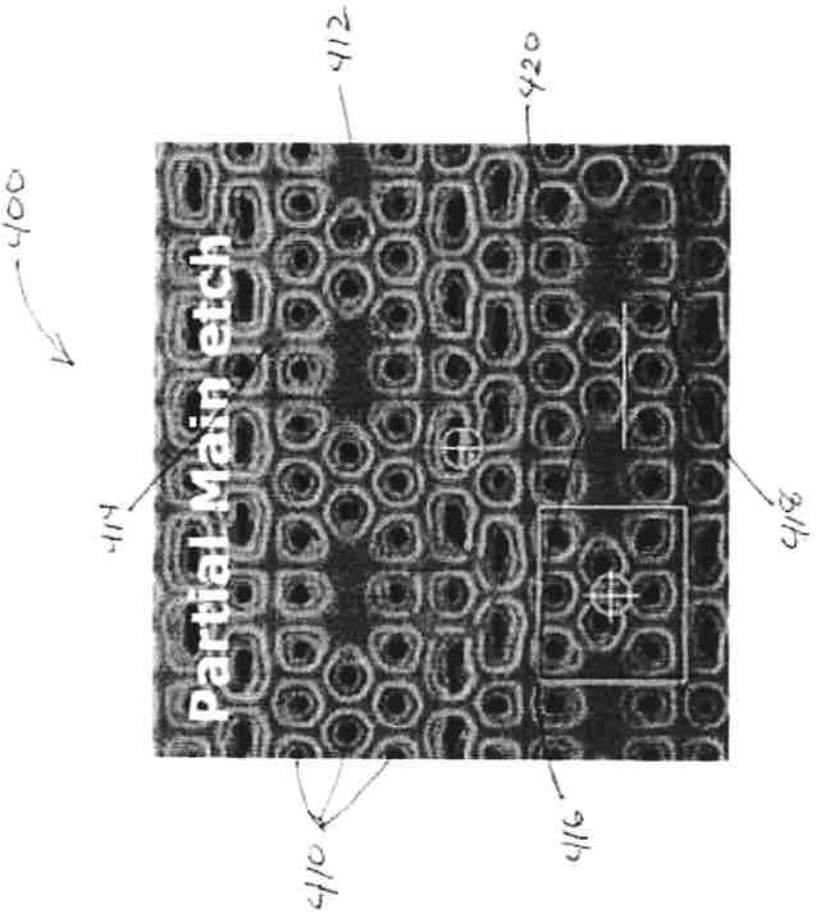

Figure 4

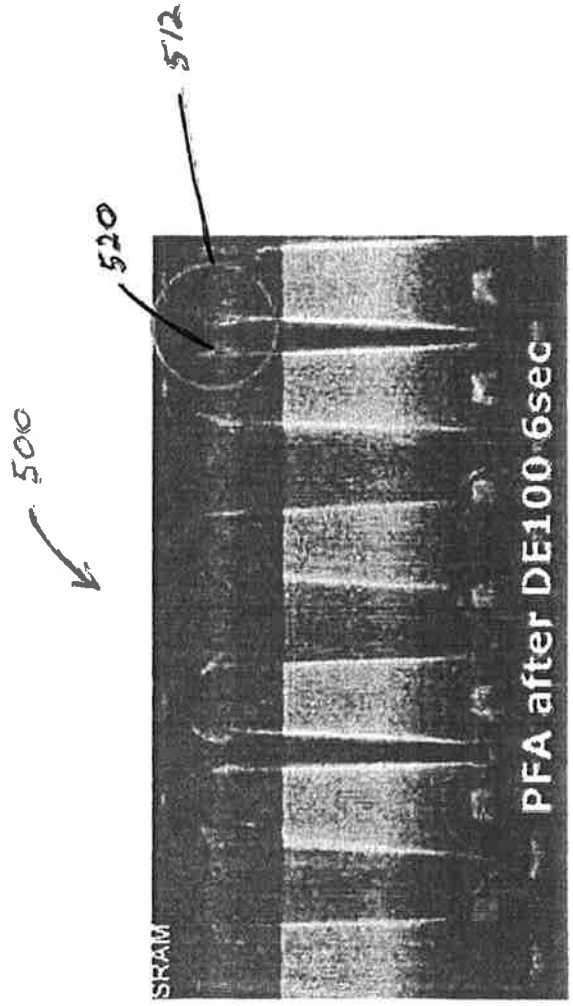

Figure 5

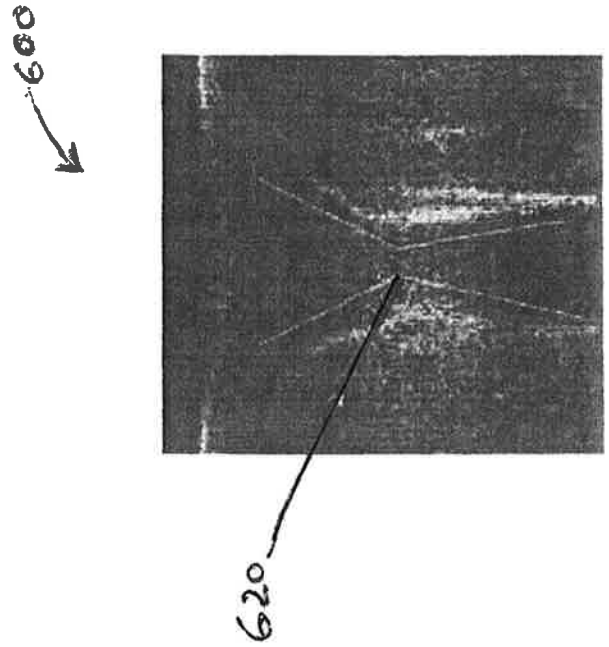

Figure 6

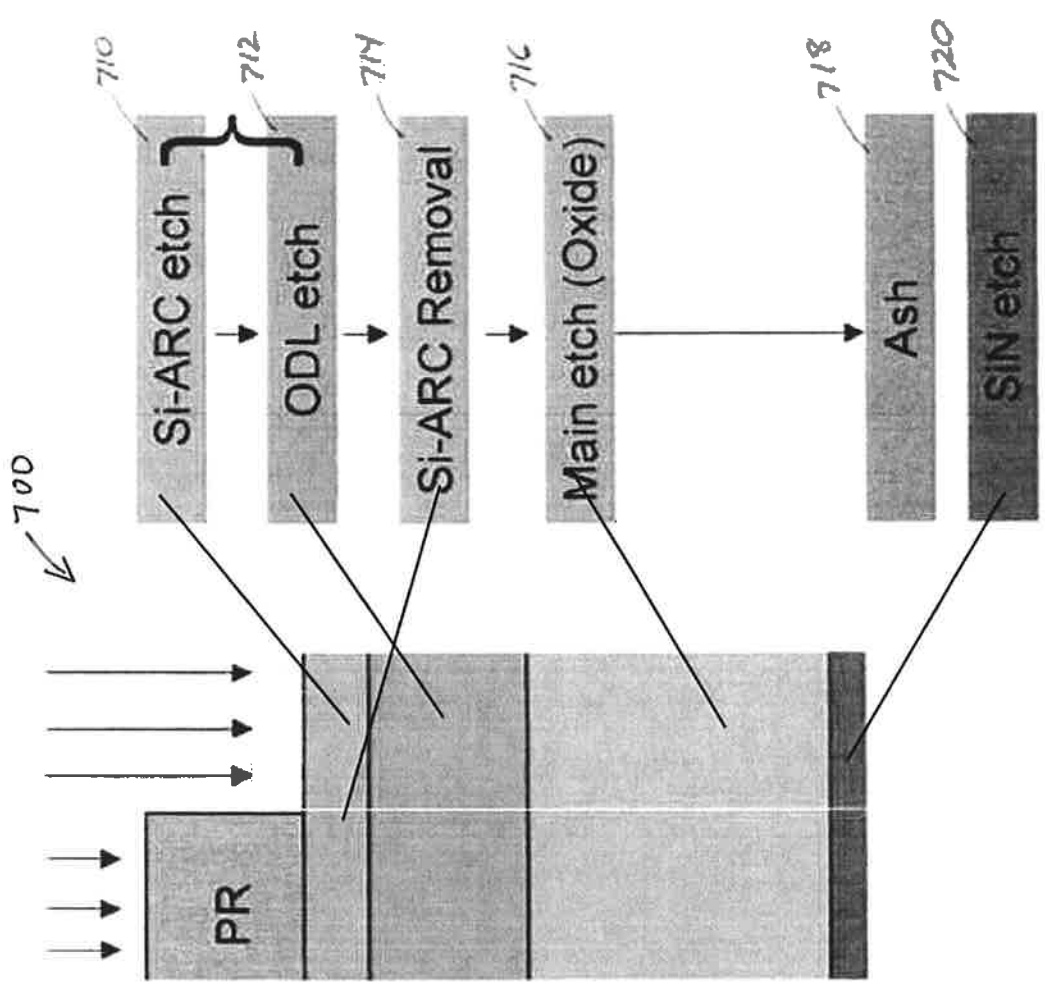
700
710
712
714
716
718
720
Si-ARC etch
ODL etch
Si-ARC Removal
Main etch (Oxide)
Ash
SIN etch
PR

Figure 7

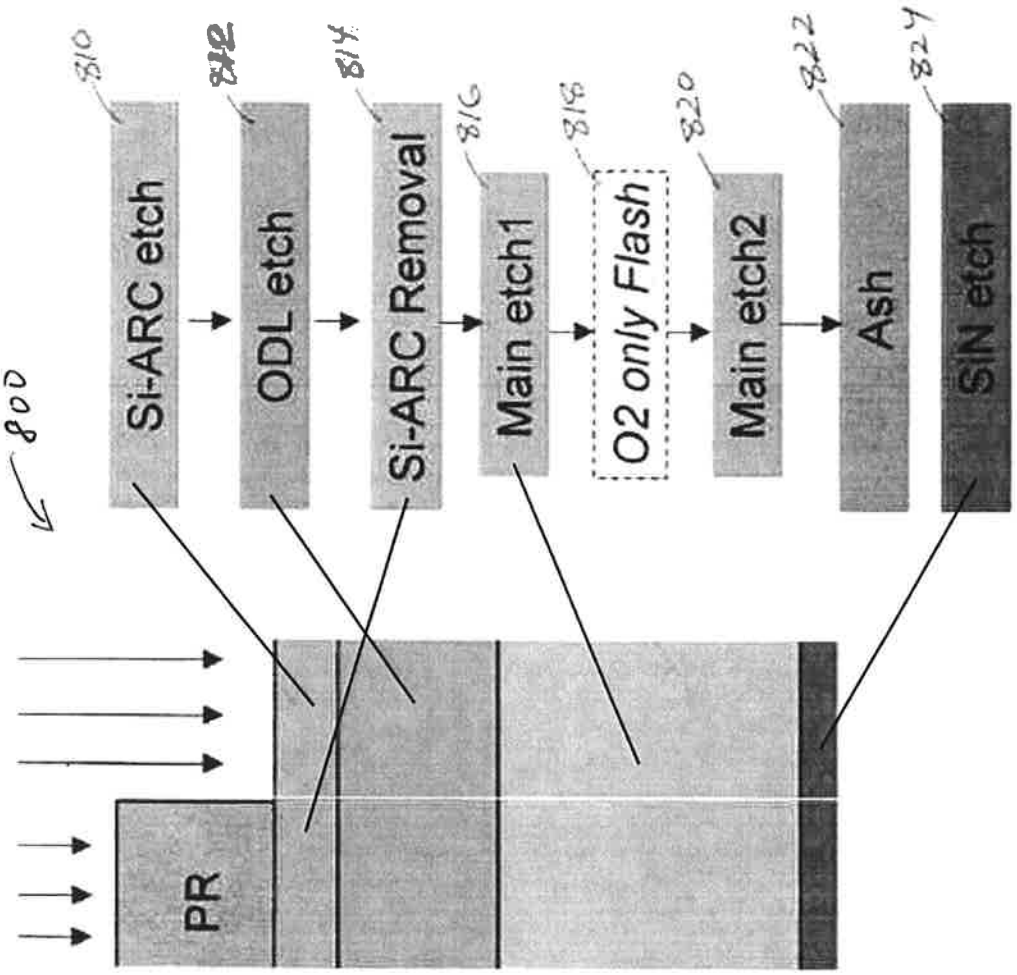
800
PR
Si-ARC etch
ODL etch
Si-ARC Removal
Main etch1
O2 only Flash
Main etch2
Ash
SiN etch
810
812
814
816
818
820
822
824

Figure 8

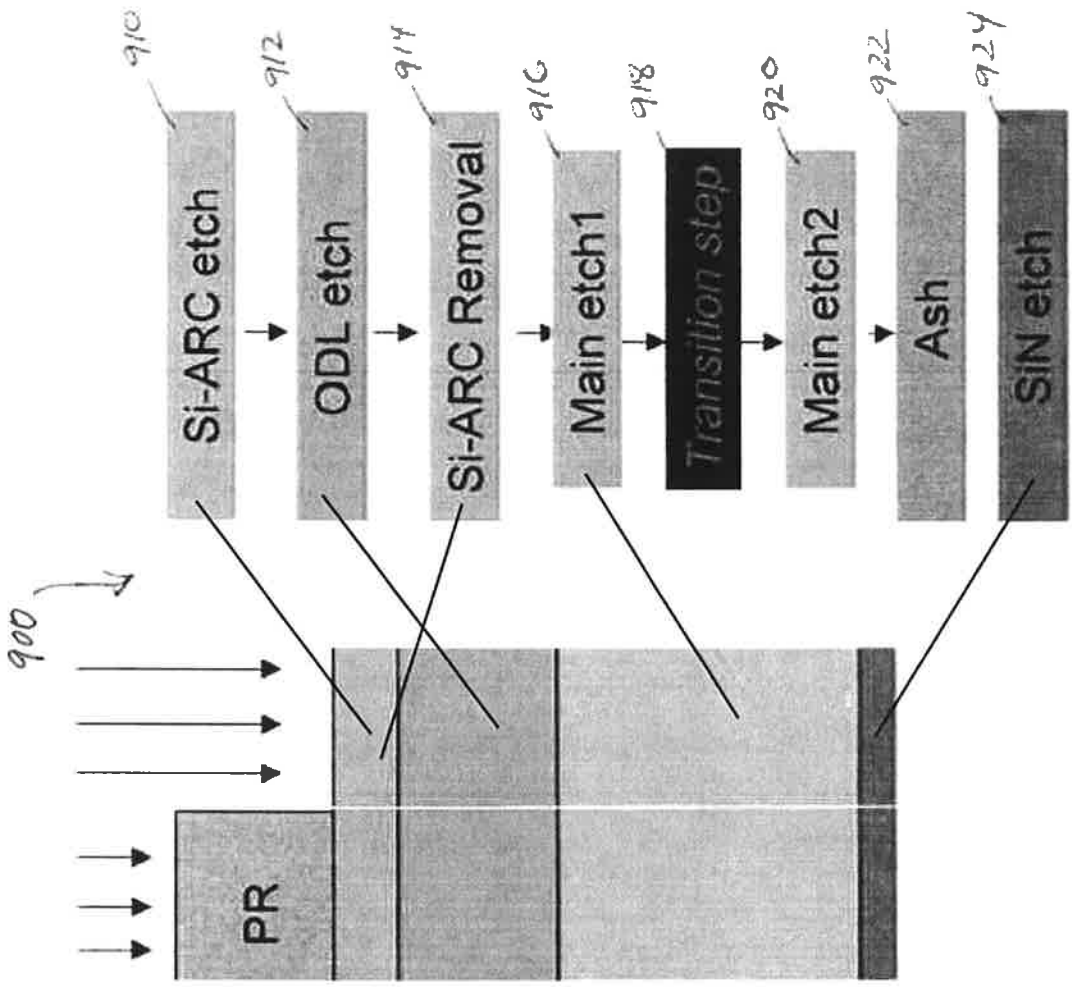
900
PR
910
Si-ARC etch
912
ODL etch
914
Si-ARC Removal
916
Main etch1
918
Transition step
920
Main etch2
922
Ash
924
SiN etch

Figure 9

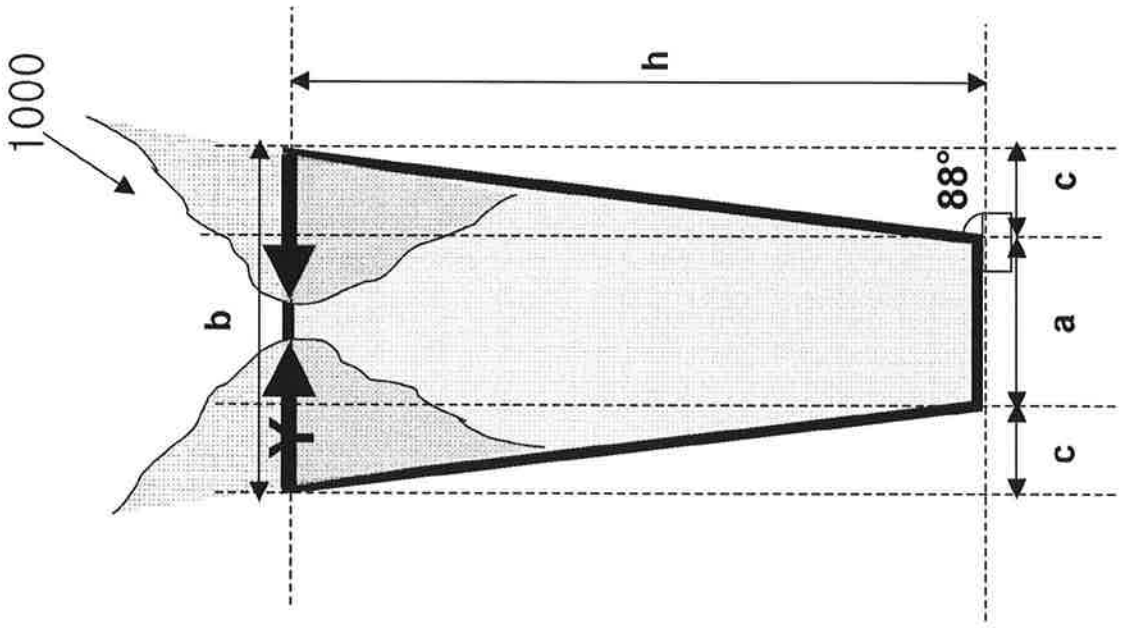

Figure 10

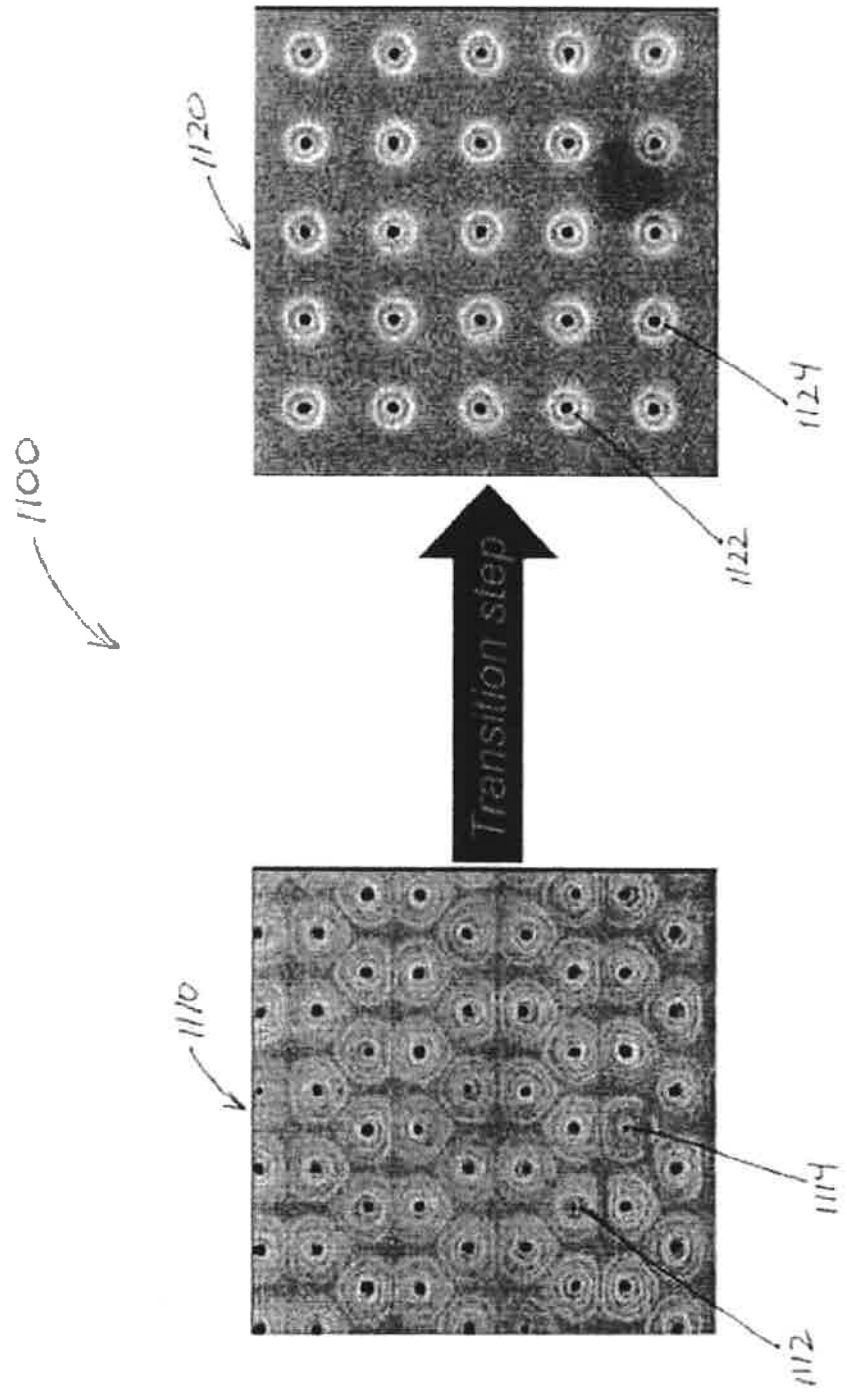

Figure 11

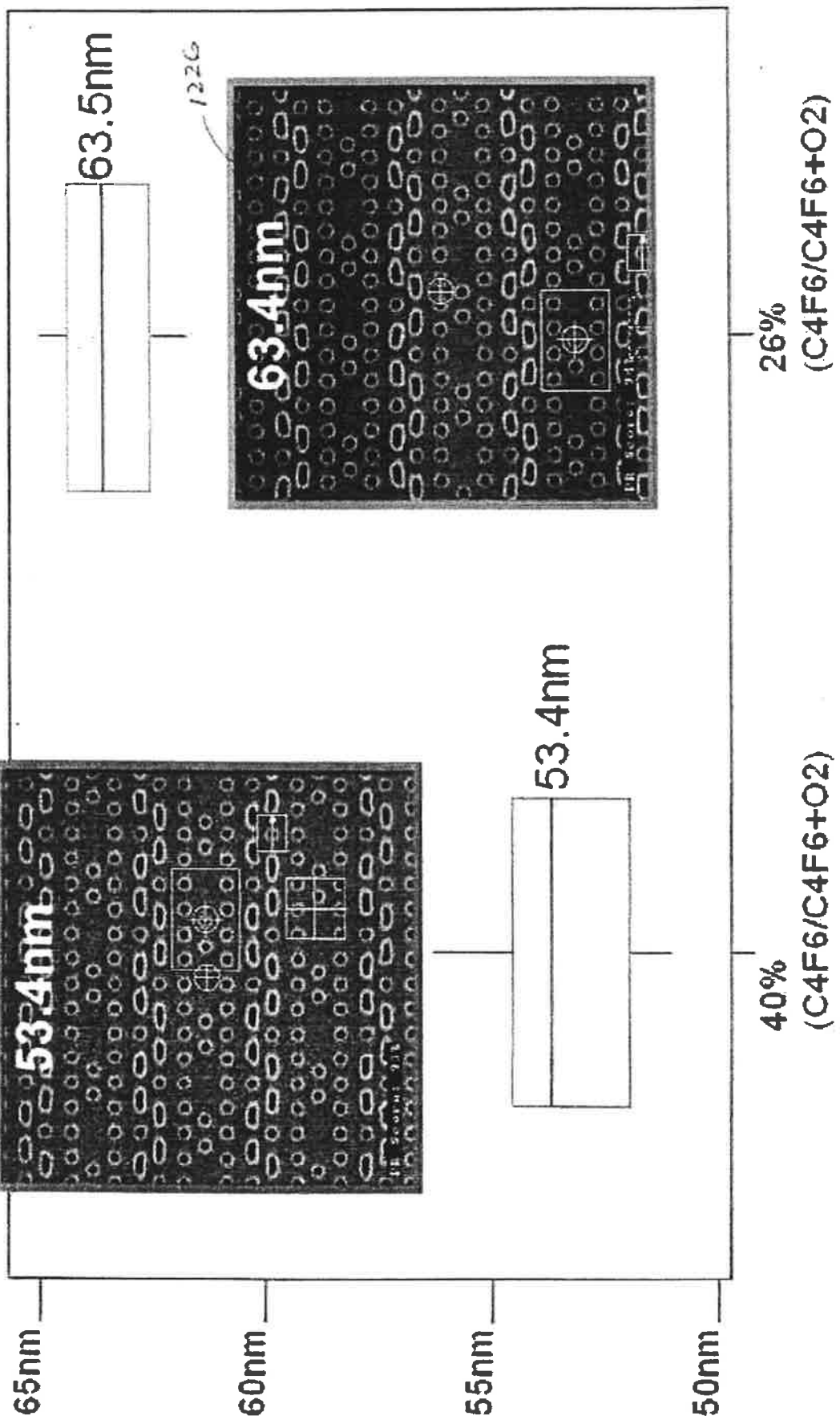
1200
1226
63.5nm
63.4nm
26%
(C4F6/C4F6+O2)
1240
53.4nm
53.4nm
40%
(C4F6/C4F6+O2)
65nm
60nm
55nm
50nm

Figure 12

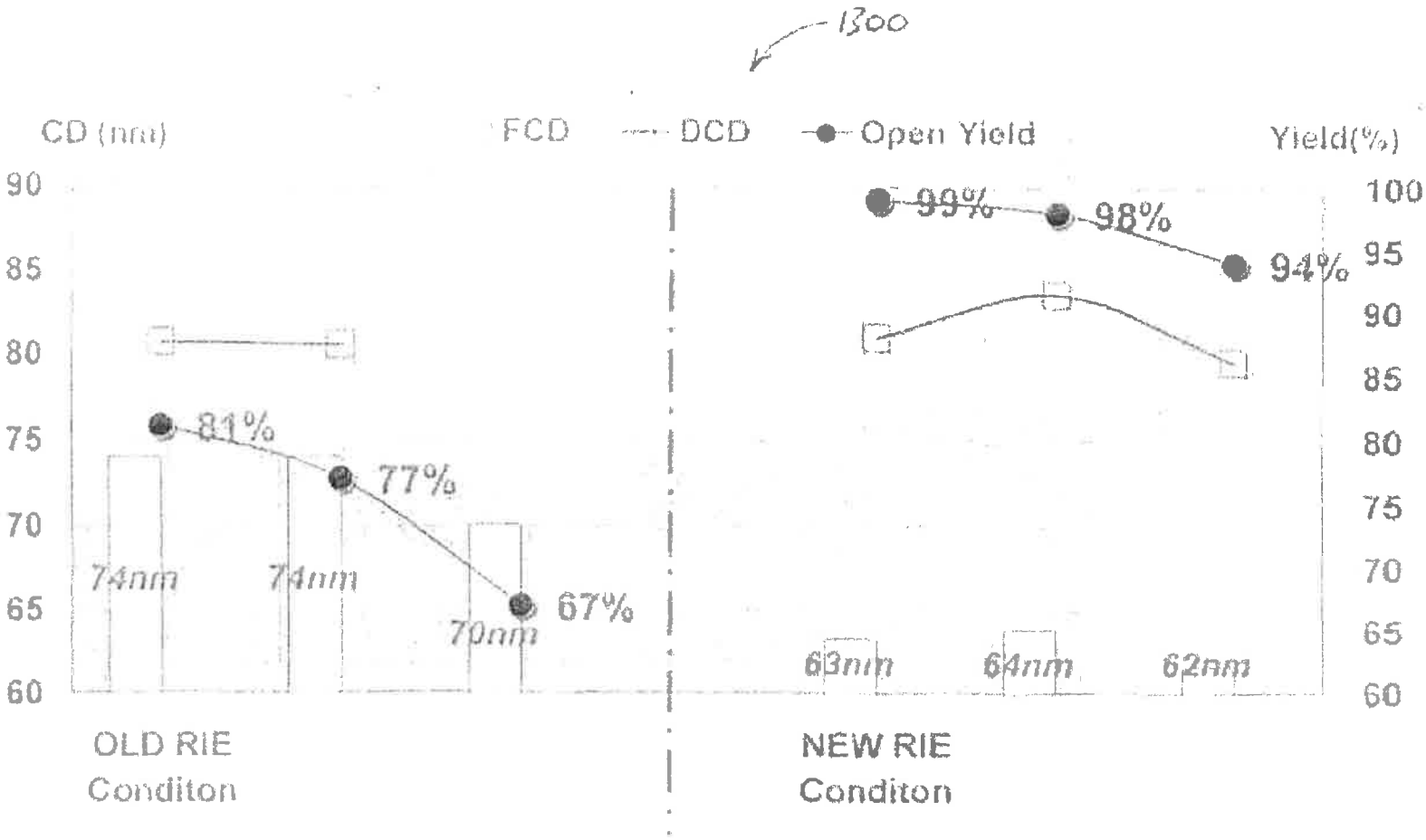
1300
CD (nm)
FCD
DCD
Open Yield
Yield(%)
90
85
80
75
70
65
60
100
95
90
85
80
75
70
65
60
99%
98%
94%
81%
77%
67%
74nm
74nm
70nm
63nm
64nm
62nm
OLD RIE
Conditon
NEW RIE
Conditon

Figure 13