

Electronic Assembly Comprising Substrate with Embedded Capacitors and Methods of Manufacture

Related Invention

The present invention is related to the following invention which is assigned to the same assignee as the present invention and which was filed on even date herewith:

Serial No. 09/628705, entitled "Electronic Assembly Comprising Interposer with Embedded Capacitors and Methods of Manufacture".

Technical Field of the Invention

The present invention relates generally to electronics packaging. More particularly, the present invention relates to an electronic assembly that includes a substrate having one or more embedded capacitors to reduce switching noise in a high speed integrated circuit, and to manufacturing methods related thereto.

Background of the Invention

Integrated circuits (ICs) are typically assembled into packages by physically and electrically coupling them to a substrate made of organic or ceramic material. One or more such IC packages can be physically and electrically coupled to a printed circuit board (PCB) or card to form an "electronic assembly". The "electronic assembly" can be part of an "electronic system". An "electronic system" is broadly defined herein as any product comprising an "electronic assembly". Examples of electronic systems include computers (e.g., desktop, laptop, hand-held, server, etc.), wireless communications devices (e.g., cellular phones, cordless phones, pagers, etc.), computer-related peripherals (e.g., printers, scanners, monitors, etc.), entertainment devices (e.g., televisions, radios, stereos, tape and compact disc players, video cassette recorders, MP3 (Motion Picture Experts Group, Audio Layer 3) players, etc.), and the like.

In the field of electronic systems there is an incessant competitive pressure among manufacturers to drive the performance of their equipment up while driving down production costs. This is particularly true regarding the packaging of ICs on substrates, where each new generation of packaging must provide increased performance while generally being smaller or more compact in size.

An IC substrate may comprise a number of insulated metal layers selectively patterned to provide metal interconnect lines (referred to herein as "traces"), and one or more electronic components mounted on one or more surfaces of the substrate. The electronic component or components are functionally connected to other elements of an electronic system through a hierarchy of conductive paths that includes the substrate traces. The substrate traces typically carry signals that are transmitted between the electronic components, such as ICs, of the system. Some ICs have a relatively large

number of input/output (I/O) terminals, as well as a large number of power and ground terminals. The large number of I/O, power, and ground terminals requires that the substrate contain a relatively large number of traces. Some substrates require multiple layers of traces to accommodate all of the system interconnections.

Traces located within different layers are typically connected electrically by vias (also called "plated through-holes") formed in the board. A via can be made by making a hole through some or all layers of a substrate and then plating the interior hole surface or filling the hole with an electrically conductive material, such as copper or tungsten.

One of the conventional methods for mounting an IC on a substrate is called "controlled collapse chip connect" (C4). In fabricating a C4 package, the electrically conductive terminations or lands (generally referred to as "electrical contacts") of an IC component are soldered directly to corresponding lands on the surface of the substrate using reflowable solder bumps or balls. The C4 process is widely used because of its robustness and simplicity.

As the internal circuitry of ICs, such as processors, operates at higher and higher clock frequencies, and as ICs operate at higher and higher power levels, switching noise can increase to unacceptable levels.

For the reasons stated above, and for other reasons stated below which will become apparent to those skilled in the art upon reading and understanding the present specification, there is a significant need in the art for a method and apparatus for packaging an IC on a substrate that minimizes problems, such as switching noise, associated with high clock frequencies and high power delivery.

Brief Description of the Drawings

FIG. 1 is a block diagram of an electronic system incorporating at least one electronic assembly with embedded capacitors in accordance with one embodiment of the invention;

FIG. 2 shows a cross-sectional representation of a multilayer substrate with embedded capacitors in accordance with one embodiment of the invention;

FIG. 3 shows a cross-sectional representation of a multilayer substrate with embedded capacitors in accordance with another embodiment of the invention;

FIG. 4 shows a cross-sectional representation of a multilayer substrate with embedded discrete capacitors in accordance with an alternate embodiment of the invention;

FIG. 5 shows a graphical representation of capacitance versus area for various dielectric materials that can be used in a substrate with an embedded capacitor in accordance with one embodiment of the invention;

5 FIG. 6 is a flow diagram of a method of fabricating a substrate comprising an embedded capacitor, in accordance with one embodiment of the invention; and

FIG. 7 is a flow diagram of a method of fabricating an electronic assembly having a substrate comprising an embedded capacitor, in accordance with one embodiment of the invention.

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Detailed Description of Embodiments of the Invention

In the following detailed description of embodiments of the invention, reference is made to the accompanying drawings which form a part hereof, and in which is shown by way of illustration specific preferred embodiments
15 in which the inventions may be practiced. These embodiments are described in sufficient detail to enable those skilled in the art to practice the invention, and it is to be understood that other embodiments may be utilized and that logical, mechanical and electrical changes may be made without departing from the spirit and scope of the present inventions. The following detailed
20 description is, therefore, not to be taken in a limiting sense, and the scope of the present invention is defined only by the appended claims.

The present invention provides a solution to power delivery problems that are associated with prior art packaging of integrated circuits that operate at high clock speeds and high power levels by embedding one or more
25 decoupling capacitors in a multilayer substrate. Various embodiments are illustrated and described herein. In one embodiment, the IC die is directly mounted to the multilayer substrate, which contains embedded capacitors. The embedded capacitors can be discrete capacitors, or they can be one or more layers of capacitive material.

30 FIG. 1 is a block diagram of an electronic system 1 incorporating at least one electronic assembly 4 with embedded capacitors in accordance with one embodiment of the invention. Electronic system 1 is merely one example of an electronic system in which the present invention can be used. In this example, electronic system 1 comprises a data processing system that
35 includes a system bus 2 to couple the various components of the system. System bus 2 provides communications links among the various components of the electronic system 1 and can be implemented as a single bus, as a combination of busses, or in any other suitable manner.

Electronic assembly 4 is coupled to system bus 2. Electronic assembly 4 can include any circuit or combination of circuits. In one embodiment, electronic assembly 4 includes a processor 6 which can be of any type. As used herein, "processor" means any type of computational circuit, such as but not limited to a microprocessor, a microcontroller, a complex instruction set computing (CISC) microprocessor, a reduced instruction set computing (RISC) microprocessor, a very long instruction word (VLIW) microprocessor, a graphics processor, a digital signal processor (DSP), or any other type of processor or processing circuit.

Other types of circuits that can be included in electronic assembly 4 are a custom circuit, an application-specific integrated circuit (ASIC), or the like, such as, for example, one or more circuits (such as a communications circuit 7) for use in wireless devices like cellular telephones, pagers, portable computers, two-way radios, and similar electronic systems. The IC can perform any other type of function.

Electronic system 1 can also include an external memory 10, which in turn can include one or more memory elements suitable to the particular application, such as a main memory 12 in the form of random access memory (RAM), one or more hard drives 14, and/or one or more drives that handle removable media 16 such as floppy diskettes, compact disks (CDs), digital video disk (DVD), and the like.

Electronic system 1 can also include a display device 8, a loudspeaker 9, and a keyboard and/or controller 20, which can include a mouse, trackball, game controller, voice-recognition device, or any other device that permits a system user to input information into and/or receive information from electronic system 1.

FIG. 2 shows a cross-sectional representation of a multilayer substrate 210 with embedded capacitors in accordance with one embodiment of the invention. Substrate 210 has a plurality of lands 211-213 on one surface thereof that can be coupled to leads or conductive areas 201-203, respectively, on IC die 200 via solder balls or bumps 208. Leads 201 are coupled to signal lines of IC die 200, lead 202 is coupled to Vcc, and lead 203 is coupled to Vss. It will be understood that, although identical reference numbers have been used for the two conductive paths carrying signal levels, i.e. the paths comprising the structure identified by reference numbers 201, 208, 211, and 221-223, these signals can be different. Signal path structure

can include various signal conductors illustrated as conductive layers within ceramic substrate 210, such as signal conductors 235-237.

Signal leads or bumps, such as signal bumps 201, are typically arranged at the periphery of the die in an arrangement that is, for example, several rows deep (only one row being shown on each side of die 200 for the sake of simplicity).

Substrate 210 can include multiple Vcc, Vss, and signal conductors, only a few of which are illustrated for the sake of simplicity.

Substrate 210 comprises a pair of embedded capacitors. Each capacitor 230 comprises a pair of capacitive plates 226 and 229, with high permittivity (Dk) layers 228 between the capacitive plates 226 and 229, and between capacitors 230. One capacitive plate 226 of each capacitor 230 can be coupled to a Vss terminal 203 on die 200 via conductor 215, land 213, and solder ball 208. Another capacitive plate 229 of each capacitor 230 can be coupled to a Vcc terminal 202 on die 200 via conductor 227, land 212, and solder ball 208.

The expression "high permittivity layer" as used herein means a layer of high permittivity material such as a high permittivity ceramic ply such as titanate particles; a high permittivity dielectric film such as a titanate film that is deposited, for example, by Sol-Gel or metal-organic chemical vapor deposition (MOCVD) techniques; or a layer of any other type of high permittivity material.

Substrate 210 can be provided with one or more embedded capacitors 230.

Die 200 and substrate 210 can be of any type. In one embodiment, die 200 is a processor, and substrate 210 is a multilayer ceramic substrate.

In the embodiment shown in FIG. 2, metallized power vias 215 and 227, situated in the central or core region of substrate 210, can connect the Vss and Vcc capacitive plates 226 and 229, respectively, of capacitor 210 to the corresponding regions of the die, which can comprise a relatively large number of Vss and Vcc die bumps 203 and 202, respectively, distributed in the core region of the die 200. This large parallel connectivity ensures very low inductance (e.g. < 1 pico-Henry) and enhances the current carrying ability of the overall IC packaging structure.

The invention is equally applicable to embodiments where signal traces occur other than at the periphery of the die, and to embodiments where Vcc and Vss traces are provided anywhere on the die.

It will be understood that while the pitch of power vias 215 and 227 in FIG. 2 is shown to be the same as the die bump pitch, the pitch of power vias 215 and 227 could be different from that of the die bump pitch. Likewise, while the pitch of signal vias 223 is shown to be wider than that of the die bump pitch, it could be the same in another embodiment. The geometry of the vias, including via pitch, can be varied in any suitable manner in accordance with design parameters known to those skilled in the art.

Various embodiments can be implemented using ceramic substrate technology.

One important purpose of the substrate with embedded capacitor(s) is to provide relatively high capacitance relatively close to the die in order to reduce the effect of reactive inductive coupling when the IC is operating, particularly at high clock speeds.

FIG. 3 shows a cross-sectional representation of a substrate 310 with embedded capacitors in accordance with another embodiment of the invention. In the embodiment illustrated in FIG. 3, substrate 310 can be coupled to a further substrate 320. Substrate 320 can be similar to substrate 310, optionally having an IC die (not shown) on the opposite surface thereof, or it can be a printed circuit board (PCB) or other type of substrate. Leads or conductive areas 334, 339, and 319 of substrate 320 can be coupled to corresponding lands 331, 332, and 317 of substrate 310 via solder balls 338.

The internal structure of substrate 310 can be similar to that described above regarding substrate 210 (FIG. 2). Thus, substrate 310 has a plurality of lands 311-313 on one surface thereof that can be coupled to leads or conductive areas 301-303, respectively, on IC die 300 via solder balls 308. Leads 301 are coupled to signal lines of IC die 300, lead 302 is coupled to Vcc, and lead 303 is coupled to Vss. It will be understood that, although identical reference numbers have been used for the two conductive paths carrying signal levels, i.e. the paths comprising the structure identified by reference numbers 301, 308, 311, and 321-323, these signals can be different. Signal path structure can include various signal conductors illustrated as conductive layers within substrate 310, such as signal conductors 335-337.

Substrate 310 can include multiple Vcc, Vss, and signal conductors, only a few of which are illustrated for the sake of simplicity.

Substrate 310 can comprise a pair of embedded capacitors 330, each comprising a pair of capacitive plates 326 and 329, with high Dk layers 340

between the capacitive plates 326 and 329, and between capacitors 330. One capacitive plate 326 of each capacitor 330 can be coupled to a Vss terminal 303 on die 300 through via segment 315, land 313, and solder ball 308. Plate 326 can also be coupled to a Vss terminal 319 on substrate 320 by means of via segment 316, land 317, and solder ball 338. Another capacitive plate 329 of each capacitor 330 can be coupled to a Vcc terminal 302 on die 300 through via segment 327, land 312, and solder ball 308. Plate 329 can also be coupled to a Vcc terminal 339 on substrate 320 by means of via segment 328, land 332, and solder ball 338.

Substrate 310 can be provided with one or more embedded capacitors 330.

Die 300 and substrates 310 and 320 can be of any type. In one embodiment, die 300 is a processor, substrate 310 is a multilayer ceramic substrate, and substrate 320 is a PCB. In another embodiment, substrate 320 is a ceramic substrate.

In the embodiment shown in FIG. 3, metallized power vias 315, 316 (it should be noted that various via segments illustrated in FIGS. 2 and 3, such as via segments 315, 316 and 327, 328, can be either separate vias or one continuous via) and 327, 328, situated in the central or core region of substrate 310, can connect the Vss and Vcc capacitive plates 326 and 329, respectively, of capacitor 310 to the corresponding regions of the die, which can comprise a relatively large number of Vss and Vcc die bumps 303 and 302, respectively, distributed at the core regions of the die 300. This large parallel connectivity ensures very low inductance (e.g. < 1 pico-Henry).

Various embodiments of substrates 310 and 320 can be implemented using ceramic substrate technology. The structure, including types of materials used, dimensions, number of layers, layout of power and signal conductors, and so forth, of substrates 310 and 320 can be similar or different, depending upon the requirements of the electronic assembly of which they form a part.

It will be understood that the land/bump pitch of the top of substrate 310 needs to match the bump pitch of die 300, and that the land/bump pitch of the bottom of substrate 310 needs to match the pad pitch of substrate 320. While in the embodiment shown in FIG. 3 the pitch of the power vias 315 and 327 is the same on the top and bottom of substrate 320, and the pitch of the signal vias 323 is wider on the bottom of substrate 320 than on the top of

substrate 320, the pitch relationship could be altered in any suitable fashion to satisfy design constraints and objectives.

FIG. 4 shows a cross-sectional representation of a multilayer substrate 410 with two embedded discrete capacitors 430 and 440 in accordance with an alternate embodiment of the invention. Substrate 410, which can include multiple layers of Vcc, Vss, and signal conductors, is intended to be used to mount a die 400 thereon. Lands 402 of substrate 410 are intended to be at Vcc potential and can be coupled via certain ones of solder balls 401 to corresponding conductive areas (not shown) on IC die 400. Likewise, lands 403 are intended to be at Vss potential and can be coupled via other solder balls 401 to corresponding areas (not shown) on IC die 400.

Discrete capacitors 430 and 440 can be of any suitable type. In one embodiment, each discrete capacitor 430 and 440 comprises a pair of upper terminals 426 and 428 and a pair of lower terminals 423 and 425. However, discrete capacitors with more or fewer terminals and/or with terminals coupled only to the upper portions of substrate 410 may also be used. For example, in the Related Invention mentioned above, in one embodiment a single discrete capacitor embedded within an interposer has two terminals that are coupled only to the upper part of the interposer. A similar capacitive structure could likewise be employed in an embodiment of the present invention, i.e. having terminals that are coupled only to the upper part of substrate 410.

Lands 402 are coupled to upper terminal 426 of embedded capacitor 430 by a route that includes power vias 404, conductive layer 406, and power via 412. Lands 403 are coupled to the other upper terminal 428 of embedded capacitor 430 by a route that includes power vias 405, conductive layer 407, and power via 413.

Lands 431 are coupled to lower terminal 423 of embedded capacitor 430 by a route that includes power vias 418, conductive layer 416, and power via 422. Lands 432 are coupled to the other lower terminal 425 of embedded capacitor 430 by a route that includes power vias 419, conductive layer 417, and power via 424.

As illustrated in FIG. 4, similar Vcc and Vss connections can be made to the terminals of capacitor 440 as were described with respect to capacitor 430.

As illustrated in FIG. 4, the power vias, including power vias 404, 405, 412, 413, 418, 419, 422, and 424, are located in a core region of substrate 410 (the left-hand portion of IC die 400 and substrate 410 are not illustrated for simplicity), which substantially underlies the core region of IC die 400.

Various signal routing (not illustrated for the sake of simplicity, but comprising

signal areas of IC die 400, certain solder balls 401, appropriate lands on substrate 410 such as lands 408 and 434, and signal planes and signal vias within substrate 410 such as signal via 409) can also be provided within substrate 410, as will be understood by those of ordinary skill.

As illustrated in FIG. 4, the signal vias, including signal via 409, are located in a peripheral region of substrate 410 (the left-hand portion of IC die 400 and substrate 410 are not illustrated for simplicity), which substantially underlies the periphery of IC die 400.

Embedded capacitors 430 and 440 can be of any suitable construction. In one embodiment, they are ceramic chip capacitors that are fabricated using conventional ceramic chip capacitor technology. While two capacitors 430 and 440 are illustrated, for the sake of simplicity of illustration and description, a different number of capacitors could be used in the embodiment illustrated in FIG. 4, including only one capacitor.

FIGS. 2-4 are merely representational and are not drawn to scale. Certain proportions thereof may be exaggerated, while others may be minimized. FIGS. 2-4 are intended to illustrate various implementations of the invention, which can be understood and appropriately carried out by those of ordinary skill in the art.

Fabrication

Multilayer ceramic substrates can be fabricated by conventional techniques, such as but not limited to high temperature co-fired ceramic (HTCC) technology, high thermal coefficient of expansion (HITCE) technology, or glass ceramic technology.

Although it is known in ceramic technology to embed low Dk capacitors in ceramic substrates, by sandwiching thin (e.g. 2 mils) films of conventional ceramic such as Al_2O_3 between metal planes, in the present invention multilayer stacks of high Dk ply are used in one embodiment. High Dk ply is commercially available for fabricating ceramic chip capacitors, for example. Suitable high Dk materials, such as titanate particles, can be inserted into the conventional ceramic matrix. Multilayer stacks of high Dk ply, such as $BaTiO_3$, in the present invention can provide capacitances as high as 10 $\mu F/sq. cm.$, compared to capacitances in the range of only nano-Farads/sq. cm. for low Dk ply.

In an alternative embodiment, a high Dk layer, such as a titanate film, e.g. $(Ba_xSr_{1-x})TiO_3$ (BST) or $PbZrTiO_3$ (PZT) or Ta_2O_5 or $SrTiO_3$, can be formed in the ceramic substrate by known techniques such as a metal-organic chemical vapor deposition (MOCVD) process, or a Sol-Gel process, in which a sol, which is a colloidal suspension of solid particles in a liquid, transforms into a gel due to growth and interconnection of the solid particles.

In either case, high Dk material can be embedded at temperature ranges that are compatible with ceramic technology (e.g. 600-1000 degrees Centigrade).

Regarding the embodiment illustrated in FIG. 4, wherein discrete capacitors 430 and 440 are embedded in the substrate 410, access to capacitors 430 and 440 can be made by any conventional technique, such as punching or laser ablation, and the Vcc and Vss conductors of substrate 410 can be coupled to the terminals of capacitors 430 and 440 by any appropriate metallization technique that is consistent with the temperature requirements of the process.

Estimation of Capacitance

Capacitance values for the embodiment shown in FIG. 3 can be estimated via Equation 1.

$$\text{Equation (1) } C = A * \epsilon_r * \epsilon_0 / d$$

where: A = capacitor size (square meters)

ϵ_r = permittivity constant 8.854×10^{-12} Farads/meter

ϵ_0 = dielectric constant of insulator

d = dielectric layer thickness (meters)

FIG. 5 shows a graphical representation of capacitance (in nano-Farads) versus a side dimension of the capacitor (in microns) for various dielectric materials that can be used in a substrate with an embedded capacitor in accordance with one embodiment of the invention. Shown in FIG. 5 are plots for the following dielectric materials: line 501 for PZT (Dk=2000), line 502 for BaTiO₃ (Dk= 1000), line 503 for BST (Dk=500), line 504 for SrTiO_x (Dk=200), and line 505 for TaO_x (Dk=25).

FIG. 5 summarizes the approximate range of capacitance available with the various titanates and oxide materials indicated. When using high permittivity ceramic ply (such as ceramic ply impregnated with BaTiO₃), the indicated values correspond to the maximum capacitance generally achievable with a 10 micron thick ply between Vcc and Vss layers in a stack containing 40 such layers.

In the case of dielectric formed by Sol-Gel or MOCVD embodiments (e.g., PZT, BST, SrTiO₃ or Ta₂O₅), the computed values correspond to a

0.25 micron film of the indicated dielectric.

To satisfy the capacitance requirements of any given embodiment, multiple layers of capacitors could be stacked as necessary.

5 FIG. 6 is a flow diagram of a method of fabricating a substrate comprising an embedded capacitor, in accordance with one embodiment of the invention. The method begins at 601.

10 In 603, at least one capacitor having first and second terminals is formed within a substrate structure. In one embodiment, the structure is a multilayer ceramic structure, although in other embodiments the structure could be formed of a material other than a ceramic material. The capacitor comprises (1) at least one high permittivity layer sandwiched between conductive layers; alternatively, the capacitor is (2) a discrete capacitor.

15 In 605, first and second power supply nodes are formed in the substrate structure. As used herein, the term "power supply node" refers to either a ground node (e.g. Vss) or to a power node at a potential different from ground (e.g. Vcc).

20 In 607, a plurality of lands are formed on a surface of the substrate structure, including a first land coupled to the first terminal(s) of the capacitor(s) and to the first power supply node, and a second land coupled to the second terminal(s) of the capacitor(s) and to the second power supply node. The first and second lands are positioned to be coupled to first and second power supply nodes of a die (e.g. IC die 200, FIG. 2) that is to be juxtaposed to a surface of the substrate structure and physically affixed thereto. The method ends at 609.

25 FIG. 7 is a flow diagram of a method of fabricating an electronic assembly having a substrate comprising an embedded capacitor, in accordance with one embodiment of the invention. The method begins at 701.

In 703, a die is provided that has first and second power supply nodes.

30 In 705, a substrate is provided that has third and fourth power supply nodes. The substrate comprises at least one capacitor having first and second terminals. The capacitor comprises (1) at least one high permittivity layer sandwiched between conductive layers; alternatively, the capacitor is a discrete capacitor. The substrate further comprises a plurality of lands on a surface thereof, including a first land coupled to the first terminal(s) of the capacitor(s) and to the third power supply node, and a second land coupled to the second terminal(s) of the capacitor(s) and to the fourth power supply

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node.

In 707, the first and second lands are coupled to the first and second power supply nodes, respectively, of the die. The method ends at 709.

5 The operations described above with respect to the methods illustrated in FIGS. 6 and 7 can be performed in a different order from those described herein.

Conclusion

10 The present invention provides for an electronic assembly and methods of manufacture thereof that minimize problems, such as switching noise, associated with high clock frequencies and high power delivery. The present invention provides scalable high capacitance (e.g. >10 mF/square centimeter) by employing embedded decoupling capacitors having low inductance which can satisfy the power delivery requirements of, for example, high
15 performance processors. An electronic system that incorporates the present invention can operate at higher clock frequencies and is therefore more commercially attractive.

As shown herein, the present invention can be implemented in a number of different embodiments, including a substrate, an electronic
20 assembly, an electronic system, a data processing system, a method for making a substrate, and a method for making an electronic assembly. Other embodiments will be readily apparent to those of ordinary skill in the art. The capacitive elements, choice of materials, geometries, and capacitances can all be varied to suit particular packaging requirements. The particular geometry
25 of the embedded capacitors is very flexible in terms of their orientation, size, number, location, and composition of their constituent elements.

While embodiments have been shown in which signal traces are provided around the periphery, and in which Vcc and Vss traces are provided at the die core, the invention is equally applicable to embodiments where the
30 signal traces occur other than at the periphery, and to embodiments where Vcc and Vss are provided anywhere on the die.

Further, the present invention is not to be construed as limited to use in C4 packages, and it can be used with any other type of IC package where the herein-described features of the present invention provide an advantage.

35 Although specific embodiments have been illustrated and described herein, it will be appreciated by those of ordinary skill in the art that any arrangement which is calculated to achieve the same purpose may be substituted for the

specific embodiment shown. This application is intended to cover any adaptations or variations of the present invention. Therefore, it is manifestly intended that this invention be limited only by the claims and the equivalents thereof.

Claims:

1. A substrate for mounting a die, the substrate comprising:
an embedded capacitor having first and second terminals,
a first surface having a first core including a first plurality of power lands coupled to the first terminal and a first plurality of ground lands coupled to the second terminal,
a second surface having a second core including a second plurality of power lands coupled to the first terminal and a second plurality of ground lands coupled to the second terminal,
wherein the first plurality of power lands and the first plurality of ground lands are positioned to be coupled to corresponding power and ground nodes of the die.
2. The substrate recited in claim 1, wherein the substrate is a multilayer ceramic substrate.
3. The substrate recited in claim 1 or 2, wherein the second plurality of power lands and the second plurality of ground lands are positioned to be coupled to corresponding power and ground nodes of an additional substrate subjacent to the substrate.
4. The substrate recited in any one of claims 1 to 3, wherein the first surface has a first periphery including a first plurality of signal lands, the second surface has a second periphery including a second plurality of signal lands, and the signal lands of the first plurality of signal lands are positioned to be coupled to corresponding signal nodes of the die.
5. The substrate recited in claim 4, wherein the signal lands of the second plurality of signal lands are positioned to be coupled to corresponding signal nodes of an additional substrate subjacent to the substrate.
6. The substrate recited in any one of claims 1 to 5, wherein the embedded capacitor includes at least one high permittivity layer.
7. The substrate recited in any one of claims 1 to 5, wherein the embedded capacitor includes a plurality of high permittivity layers.

8. The substrate recited in claim 7, wherein the embedded capacitor includes a plurality of conductive layers interleaved with the high permittivity layers, such that alternating conductive layers are coupled to the first and second terminals respectively.

9. The substrate recited in any one of claims 1 to 5, wherein the embedded capacitor includes at least one embedded discrete capacitor.

10. The substrate recited in any one of claims 1 to 9, wherein at least one power land of the first plurality of power lands is coupled to the first terminal through a via that does not go entirely through the substrate.

11. The substrate recited in any one of claims 1 to 10, wherein at least one ground land of the second plurality of ground lands is coupled to the second terminal through a via that does not go entirely through the substrate.

12. An electronic assembly comprising:
a die including power and ground nodes, and
the substrate recited in any one of claims 1 to 11,
wherein the first plurality of power lands and the first plurality of ground lands are respectively coupled to the power and ground nodes of the die.

13. An electronic system comprising the electronic assembly recited in claim 12, wherein the first and second terminals of the embedded capacitor are respectively coupled to the power and ground nodes of the die.

14. A data processing system comprising:
a bus coupling components in the data processing system;
a display coupled to the bus;
an external memory coupled to the bus; and
a processor coupled to the bus,
wherein the processor comprises the electronic assembly recited in claim 12.

15. A method for making a substrate to package a die, the method comprising:
forming in the substrate at least one capacitor having first and second terminals;
forming in the substrate first and second power supply nodes; and
forming a plurality of lands on a surface of the substrate, including a first land coupled to the first terminal and to the first power supply node, and a second land coupled to the second terminal and to the second power supply node, wherein the first and second lands are located at a first core of the surface, and are positioned to be coupled to first and second power supply nodes of the die.
16. The method recited in claim 15 wherein, the substrate is a multilayer ceramic substrate.
17. The method recited in claim 15 or 16, wherein the at least one capacitor is formed of a plurality of high permittivity layers.
18. The method recited in claim 17, wherein the at least one capacitor is formed of a plurality of conductive layers interleaved with the high permittivity layers, such that alternating conductive layers are coupled to the first and second lands, respectively.
19. The method recited in claim 15 wherein the at least one capacitor is formed of at least one embedded discrete capacitor.
20. A method of making an electronic assembly comprising:
providing a substrate by the method recited in any one of claims 15 to 19, and
providing the die with power and ground nodes;
wherein the power and ground nodes are respectively the first and second power supply nodes of the die.
21. A substrate to package a die, the substrate comprising:
a plurality of power and ground vias in a core region of the substrate;
an embedded capacitor having first and second terminals; and
a plurality of power lands coupled to the first terminal through the plurality of power vias, and a plurality of ground lands coupled to the second terminal through the plurality of ground vias;

wherein the plurality of power lands and the plurality of ground lands are positioned to be coupled to corresponding power and ground nodes of the die.

22. The substrate recited in claim 21, wherein the substrate is a multilayer ceramic substrate.

23. The substrate recited in claim 21 or 22, wherein the plurality of power lands are substantially equal in number to the plurality of ground lands.

24. The substrate recited in claim 21, 22 or 23, wherein at least one of the power vias does not go entirely through the substrate.

25. The substrate recited in any one of claims 21 to 24, wherein at least one of the ground vias does not go entirely through the substrate.

26. The substrate recited in any one of claims 21 to 25, further comprising
a plurality of signal vias in a peripheral region of the substrate; and
a surface having the plurality of power lands, the plurality of ground lands, and a plurality of signal lands;

wherein the plurality of signal lands are coupled to the plurality of signal vias, and the plurality of signal lands are positioned to be coupled to corresponding signal nodes of the die.

27. A substrate to package a die comprising:
a plurality of power and ground vias in a core region of the substrate;
an embedded capacitor having first and second terminals;
a first surface including a first plurality of power lands coupled to the first terminal through first ones of the plurality of power vias, and a first plurality of ground lands coupled to the second terminal through first ones of the plurality of ground vias; and
a second surface including a second plurality of power lands coupled to the first terminal through second ones of the plurality of power vias, and a second plurality of ground lands coupled to the second terminal through second ones of the plurality of ground vias;

wherein the first plurality of power lands and the first plurality of ground lands are positioned to be coupled to corresponding power and ground nodes of the die.

28. The substrate recited in claim 27, wherein the substrate is a multilayer ceramic substrate.

29. The substrate recited in claim 27 or 28, wherein the first plurality of power lands are substantially equal in number to the first plurality of ground lands.

30. The substrate recited in claim 27, 28 or 29, wherein the second plurality of power lands are substantially equal in number to the second plurality of ground lands.

31. The substrate recited in any one of claims 27 to 30, wherein at least one of the power vias does not go entirely through the substrate.

32. The substrate recited in any one of claims 27 to 31, wherein at least one of the ground vias does not go entirely through the substrate.

33. A substrate to package a die, the substrate comprising:
 a plurality of power and ground vias in a core region of the substrate;
 a plurality of signal vias;
 an embedded capacitor having first and second terminals;
 a first surface including a first plurality of power lands coupled to the first terminal through first ones of the plurality of power vias, a first plurality of ground lands coupled to the second terminal through first ones of the plurality of ground vias, and a first plurality of signal lands coupled to the plurality of signal vias; and
 a second surface including a second plurality of power lands coupled to the first terminal through second ones of the plurality of power vias, a second plurality of ground lands coupled to the second terminal through second ones of the plurality of ground vias, and a second plurality of signal lands coupled to the plurality of signal vias;
 wherein the first plurality of power lands, the first plurality of ground lands, and the first plurality of signal lands are positioned to be coupled to corresponding power, ground, and signal nodes of the die.

34. The substrate recited in claim 33, wherein the substrate is a multilayer ceramic substrate.

35. The substrate recited in claim 33 or 34, wherein the first plurality of power lands are substantially equal in number to the first plurality of ground lands.

36. The substrate recited in claim 33, 34 or 35, wherein the second plurality of power lands are substantially equal in number to the second plurality of ground lands.

37. The substrate recited in any one of claims 33 to 36, wherein at least one of the power vias does not go entirely through the substrate.

38. The substrate recited in any one of claims 33 to 37, wherein at least one of the ground vias does not go entirely through the substrate.

39. The substrate recited in any one of claims 33 to 38, wherein the plurality of signal vias are in a peripheral region of the substrate.