

TITLE OF THE INVENTION
REDUNDANT STABILIZED POWER SUPPLY

BACKGROUND OF THE INVENTION

Field of the Invention

This invention relates to a redundant stabilized power supply applicable to a computer device or the like. Specifically, the present invention relates to a redundant stabilized power supply of a type wherein the detection of both an overvoltage state at a load end and changes in output currents flowing in a pair of parallel-driven stabilized power supply circuits makes it possible to accurately determine which one of the pair of stabilized power supply circuits would be in an overvoltage state.

Description of the Related Art

Even when an a.c. source supplied to an audio video server (AV server), a computer device or the like is cut off instantaneously, stabilized power supply circuits driven in parallel have recently been used therein so that a device driving voltage is maintained at a voltage greater than or equal to a specified value during a cut-off period.

Fig. 5 is a prior art showing one example thereof. The power supply circuits that perform a parallel operation, are

normally called "redundant stabilized power supply circuits".

Referring to Fig. 5, a pair of regulated or stabilized power supply circuits 10A and 10B are respectively electrically connected to a load (such as an IC circuit or the like) 12 through diodes Da and Db which serve as reverse-current preventive elements. As the condition for driving the pair of stabilized power supply circuits 10A and 10B in parallel, the difference between source voltages (output voltages) of these is normally less than or equal to 50mV. If the potential difference exceeding 50mV is produced, then the power supply circuit low in voltage is cut off. This is because the diode Da or Db electrically connected to the other power supply circuit is cut off by the power supply circuit whose terminal voltage is high and the voltage on the cut-off power supply circuit side is not applied across the load 12.

Thus, when the second stabilized power supply circuit 10B is cut off and the load 12 is driven by the first stabilized power supply circuit 10A alone, for example, output currents are respectively represented as $I_b = 0$ and $I_a = I_L$ (I_L : load current) as shown in Fig. 6. When the difference between output voltages V_a and V_b is reversed, $I_a = 0$ and $I_b = I_L$ so that the relationship of cut-off between the stabilized power supply circuits 10A and 10B is reversed. When $I_a = I_b (= I_L)$,

the stabilized power supply circuits 10A and 10B are kept in balance. Thus, the load 12 is driven (operated or driven in parallel) by both the pair of stabilized power supply circuits 10A and 10B.

When the stabilized power supply circuits are in the parallel-driven state, i.e., when the output voltage V_a of one stabilized power supply circuit 10A is brought into an overvoltage state (a time t_1) due to some reason when $I_a = I_b$, the following operations are taken if an overvoltage detection system does not exist.

When the stabilized power supply circuits are in the parallel-driven state, $V_a = V_b$. However, once the power supply circuits are brought into unbalance, $V_a > V_b$ as shown in Fig. 7. Thus, the second stabilized power supply circuit 10B is cut off so that $I_b = 0$. Since the overvoltage state remains unchanged even if $I_b = 0$, the output voltage V_a continues to rise and exceeds a voltage V_{max} giving warrant to the load 12 in a short time. If done so, there may be cases in which components for the load 12 are destroyed. It is therefore necessary to provide some overvoltage detecting means.

As means for detecting the overvoltage produced in the aforementioned redundant power supply, the detection of voltages at points a, b and c shown in Fig. 5 has been considered.

When the output voltage at the point a or b is selected

as an overvoltage detection point, an advantage is brought about in that the overvoltage states of the stabilized power supply circuits 10A and 10B can be separately detected. On the other hand, since voltage drops developed by line impedances from the detection points a and b to the load 12 differ from each other according to the output currents I_a and I_b , the overvoltage states cannot be detected with accuracy.

On the other hand, since the power supply circuits 10A and 10B are driven in parallel when the point c corresponding to a load end is selected as the overvoltage detection point, it is not possible to determine which power supply circuit would be placed in the overvoltage state. Thus, a suitable subsequent process cannot be carried out.

SUMMARY OF THE INVENTION

Therefore, the present invention has been provided to solve the prior art problems. The present invention proposes a redundant stabilized power supply capable of accurately determining which power supply circuit would be in an overvoltage state and carrying out a suitable subsequent process.

In order to solve the above problems, there is provided a redundant stabilized power supply suitable for a parallel operation, according to the present invention, for supplying

two stabilized power supply circuits to a load in parallel and simultaneously driving the load, each power supply circuit referred to above including:

 overvoltage detecting means for detecting an overvoltage applied to a load end;

 current detecting means for detecting a current flowing in a power supply line; and

 power supply control means, and

 wherein when a state of the overvoltage applied across the load is detected and a current detection output at that time remains unchanged, the power supply control means is controlled so as to cut off the supply of power from the stabilized power supply circuit which serves as the overvoltage side.

 In the present invention, the overvoltage state is detected from the voltage applied to the load end (point c). This simple detection fails to specify which power supply circuit would be in the overvoltage state. On the other hand, when the power supply circuits are out of balance and the load is driven by the single power supply circuit in an impracticable state of their parallel operation as described above, the output currents I_a and I_b are also simultaneously brought into unbalance, so that the output current on the cut-off power supply circuit side does not flow, whereas the output current

on the other power supply circuit side continues to increase.

Noting the state of the unbalance between the output currents, which occurs upon the overvoltage state as described above, a voltage drop developed between a sense end with respect to the load and the power supply line through which the output current flows, is detected. When an output voltage becomes high, a voltage drop produced by a line impedance from the load end to an overcurrent detection end further increases correspondingly.

When the output current on the cut-off side reaches zero and the output current results in zero, the voltage drop is also brought to zero. The overvoltage state of the power supply circuit is determined by ANDing both a change in voltage drop, which is produced due to the difference between the output currents and an output at the time that the overvoltage has been detected.

This intends to specify the stabilized power supply circuit being in the overvoltage state, utilizing that when the voltage drop occurs, the AND output is inverted to a high level, whereas when no voltage drop occurs, the AND output remains at a low level.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a fragmentary systematic diagram showing one

embodiment of a redundant stabilized power supply according to the present invention;

Fig. 2 is a diagram illustrating a configuration of a shunt regulator;

Fig. 3 is a diagram depicting a symbol mark;

Figs. 4A ~4G are diagram for describing the operation of the stabilized power supply according to the present invention at the time of an overvoltage;

Fig. 5 is a systematic diagram illustrating a conventional example of a redundant stabilized power supply;

Fig. 6 is an operation explanatory diagram of a parallel operation; and

Fig. 7 is an explanatory diagram at the time of an overvoltage operation.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

One embodiment of a redundant regulated or stabilized power supply according to the present invention will hereinafter be described in detail with reference to the accompanying drawings.

In a redundant stabilized power supply 10 shown in Fig. 1, according to the present invention, first and second stabilized power supply circuits 10A and 10B electrically connected in parallel to a load 12 has d.c. voltage sources

or power supplies 14a and 14b respectively. As these d.c. power supplies 14a and 14b, ones of such types that alternating currents are separately rectified and smoothed, are used. Since a pair of stabilized power supply circuits 10A and 10B are identical in configuration to each other, only one configuration will be illustrated as an example and the other configuration will be omitted.

A series regulator will be illustrated as the stabilized power supply circuit 10A. However, it may be a switching regulator. Therefore, a series regulator 16 is provided between power supply line La and La' constituting the stabilized power supply circuit 10A. In the present embodiment, a high-accuracy series regulator constructed by combining a series regulator with a shunt regulator will be illustrated as the series regulator 16. Therefore, a series transistor Q is electrically connected to the power supply line La and controlled by a shunt regulator 20.

As shown in Fig. 2, the shunt regulator 20 has a voltage comparator 22 having an inversion terminal to which a voltage reference source 24 is electrically connected and a non-inversion terminal to which a reference voltage REF is supplied from a terminal 26.

As a result of control on a transistor 28 by an output produced from the voltage comparator 22, its collector current

varies so that the value of a current flowing between a plus side power supply terminal (cathode K) and a minus side power supply terminal (anode A) is controlled by the reference voltage REF. With an increase in the reference voltage REF, a shunt current (anode-to-cathode current) is controlled so as to increase. As a symbol mark of the shunt regulator 20, a symbol shown in Fig. 3 is used.

Such a shunt regulator 20 is electrically series-connected to a resistor 21 so that the cathode K thereof is set as the plus power side. Further, the cathode K thereof is electrically connected to the base of the series transistor Q. As a result, the high-accuracy series regulator 16 can be constructed as a whole.

The series transistor Q is electrically connected to a pulse side power supply terminal 17a through a diode Da. The power supply terminal 17a is electrically connected to the load 12 through the pulse side power supply line La. The minus side power supply line La' electrically connected to the load 12 is electrically connected to the minus side of the d.c. power supply 14a through a power supply terminal 17b.

Further, sense (SENSE) terminals 18a and 18b are drawn from both ends of the load 12 to sense a voltage applied across the load 12. Therefore, a voltage obtained between the sense terminals 18a and 18b is first fractioned or divided by a

voltage detecting means 19 composed of three resistors 19a through 19c to make a reference voltage REFa of a predetermined value. This reference voltage REFa is supplied to a reference terminal of the shunt regulator 20.

When a driving voltage applied to the load 12 varies, a voltage corresponding to its variation is sensed and the reference voltage REFa is also changed. Correspondingly, negative feedback is provided so that the voltage across the load is held constant, whereby the driving voltage is stabilized.

Further, the load voltage obtained between the sense terminals 18a and 18b is supplied to an overvoltage detecting means 30. The overvoltage detecting means 30 is constructed by electrically series-connecting a resistor 31 and a shunt regulator 32 as shown in the drawing. In this case, the shunt regulator 32 is also identical to that shown in Fig. 2 but functions as a voltage comparator in this case. A current (shunt current) flows between the cathode and anode only after a voltage REFb applied across a reference terminal has become higher than an internally-provided reference voltage Vref.

Therefore, the load voltage applied between the sense terminals 18a and 18b is supplied to the reference terminal as its reference voltage REFb through a voltage-divider circuit 33 composed of a pair of resistors 33a and 33b. Further, a

detected voltage Cv' obtained at a connection middle point p is inverted by an inverter 34 and the so-inverted detected voltage Cv is used as an overvoltage detection output. When the load voltage results in overvoltage, the shunt regulator 32 is activated to bring the connection middle point p substantially to a ground potential. Therefore, the detected output Cv produced from the inverter 34 is brought to a high level only after the ground potential has been reached.

The value of an excessive voltage or overvoltage to be detected can be selected in the following manner. As guaranteed voltages for normally operating an IC circuit used as the load 12, a voltage of 4.75V, a voltage of 5.25V and a voltage of 5V are respectively supplied on the reduced voltage side thereof, the overvoltage side thereof and the normal side as driving voltages in most cases. When such an IC circuit is used as the load 12, the voltage increased by 0.25V (250mV) from the voltage of 5V is selected as an overvoltage detection voltage.

Thus, when the reference voltage $REFb$ is increased by 250mV from the internal reference voltage V_{ref} , the overvoltage detecting means 30 is activated to obtain an overvoltage detection output Cv . Incidentally, since the difference between output voltages Va and Vb exceeds 50mV in detection timing of the overvoltage detecting means 30, the second

stabilized power supply circuit 10B is in a cut-off state.

In the present invention, an overcurrent detecting means 40 is further provided. The present example utilizes the unbalance achieved even between output currents I_a and I_b by switching a parallel operation to a single operation after an overvoltage has been reached. The activation of a power supply control means with respect to the power supply circuit on the overvoltage side and the deactivation of the power supply control means with respect to the power supply circuit on cut-off side will result in the detection of an overcurrent incident to the overvoltage.

The overcurrent forming means 40 has a voltage comparator 41. A reference voltage generating means 42 comprises a pair of resistors 42a and 42b electrically connected to a minus battery or power supply -B. A minus voltage $-V_r$ obtained by the reference voltage generating means 42 is supplied to a non-inversion terminal of the voltage comparator 41 as a reference voltage. An inversion terminal attached to the voltage comparator 41 is electrically connected to a suitable position (corresponding to a point d in the drawing) of a power supply line, or the minus power supply line La' in the present example.

Here, the power supply line La' has a line impedance (which ranges from about a few $10m\Omega$ to a few $100m\Omega$) between

its load end c' and the detection point d although it is small. During a period in which the output current I_a flows in the power supply line La' , a voltage drop (corresponding to a minus voltage $-V_d$ as viewed from the load end c') is developed by the line impedance. However, when the output voltage is out of balance and one stabilized power supply circuit is cut off, no output current flows in the stabilized power supply circuit.

Therefore, the minus voltage $-V_r$ is selected as $-V_r > -V_d$ so that a high-level comparison output (current detection output) C_i is always obtained from the voltage comparator 41 when the output current I_a flows. Thus, when the output current I_a results in zero, the potential at the inversion terminal becomes high and hence the current detection output C_i is inverted to a low level.

The overvoltage detection output C_v and the overcurrent detection output C_i are ANDed by an AND circuit 45. The resultant AND output is supplied to a switching element constituting the power supply control means, i.e., a trigger terminal of an SCR 50 in the present example as an overvoltage control signal. The SCR 50 is electrically connected to the resistor 21 and triggered by the overvoltage control signal so as to fall into an on state.

Constituent means respectively identical to the aforementioned overvoltage detecting means 30 and overcurrent

detecting means 40, AND circuit 45 and power supply control means 50 are provided even within the other stabilized power supply circuit 10B. Thus, power supply lines Lb and Lb' connect between power supply terminals 17c and 17d and the load 12. A load voltage is introduced between sense terminals 18c and 18d.

An overvoltage detecting operation of the redundant stabilized power supply 10 constructed in this way will now be described with reference to Fig. 4.

When the redundant stabilized power supply 10 works normally, the overvoltage detecting means 30 indicates $V_a = V_b (= V_L)$ and $I_a = I_b (= I_L)$ as described above. Thus, the redundant stabilized power supply 10 is in a parallel operating state.

Now consider that the output voltage V_a of the first stabilized power supply circuit 10A starts to abnormally rise or increase from a time T_1 due to some reason as shown in Fig. 4A. When the difference in potential between the two reaches 50mV or higher, the second stabilized power supply circuit 10B is brought into a state identical to the cut-off state. Thus, the output current I_a continues to rise but the other output current I_b starts to drop by degrees. Since the voltage relative to the voltage comparator 41 is not inverted even if the output current I_a rises in an overvoltage state, the current

detection output C_i (first detection output) corresponding to the output of the voltage comparator 41 still holds a high-level state (see Fig. 4B).

When the output voltage V_a rises to a voltage V_x defined as an overvoltage (time T_3), the shunt regulator 32 is activated by a reference voltage REF_b at that time so that the overvoltage detection output C_v is inverted to a high level (see Fig. 4C). As a result, a power control signal (first power control signal) T_a is brought to a high level firstly at the time T_3 (see Fig. 4D). Thus, the SCR 50 is triggered so that it is turned on.

Since the d.c. power supply 14a is shunted through the resistor 21 when the SCR 50 is turned on, the output voltage V_a becomes zero and correspondingly the output current I_a also reaches zero.

On the other hand, the same detecting operation as described above is simultaneously carried out even by the second stabilized power supply circuit 10B. Since an overvoltage state is detected by the overvoltage detecting means 30 provided within the stabilized power supply circuit 10B although not shown in the drawing, an overvoltage detection output C_v similar to that shown in Fig. 4C is obtained.

In contrast to this, the overcurrent detecting means 40 provided within the same stabilized power supply circuit 10B performs the following operation.

When the output current I_b starts to drop as shown in Fig. 4A and a voltage drop $-V_d$ at that time reaches a time T_2 at which it exceeds the reference voltage $-V_r$, the output of the voltage comparator 41 is inverted. Namely, a second current detection output C_i is inverted to a low level as shown in Fig. 4E. Its inversion timing is antecedent to overvoltage detection timing (time T_3). Since the relationship of timing between the detection outputs C_v and C_i inputted to the AND circuit 45 is represented as shown in Figs. 4C and 4E, a second power control signal T_b (see Fig. 4F) indicative of the AND output holds a low level identical to that at the time of the normal operation mode. As a result, the SCR 50 in the other stabilized power supply circuit 10B is not triggered.

When the first stabilized power supply circuit 10A is shunted by the turning on of the SCR 50, an output voltage V_a thereof starts to drop from the time T_3 according to the time constant determined by the load 12 and a decoupling capacitor (not shown) electrically connected between both ends of the load 12. Next, the load 12 is entirely driven by the second stabilized power supply circuit 10B alone at a time T_4 where $V_b > V_a$. Thus, the output voltage supplied to the load 12 is represented as shown in Fig. 4G. As is also apparent from Fig. 4A, the operating voltage V_L is continuously supplied to the load 12, so that the instantaneous cutting off of the power

supply is not developed.

During a period between the times T3 and T4, the load 12 is supplied with a driving voltage owing to a current discharged from the decoupling capacitor.

Thus, when the first stabilized power supply circuit 10A is brought into an overvoltage state, its overvoltage state is cut off and the load 12 can be activated by the normal second stabilized power supply circuit 10B alone. Even when an overvoltage takes place on the second stabilized power supply circuit 10B side, it can be easily understood that the same operation as described above is achieved.

In order to notify to which power supply circuit the stabilized power supply circuit whose power supply is in a cut-off state in the overvoltage state, corresponds, to an operator when the overvoltage stage is detected, a warning lamp or buzzer (both not shown) may be provided and driven.

In Fig. 1, the overvoltage is eventually detected by detecting the currents that flow on the minus power supply lines La' and Lb'. However, the overvoltage can be detected even in the case where the currents that flows on the plus power supply lines La and Lb, are detected. The overvoltage detecting means 30 may be provided in a dual-purpose configuration.

In the present invention as has been described above,

each of redundant stabilized power supply circuits that carry out a parallel operation, is provided with an overvoltage detecting means for detecting an overvoltage applied to a load end and a current detecting means for detecting a current flowing in a power supply line. When the state of the overvoltage applied across the load is detected and a current detection output at that time remains unchanged, a power supply control means is controlled so as to cut off the supply of power from the stabilized power supply circuit that functions as the overvoltage side.

According to this, even if the stabilized power supply circuit is brought into the overvoltage state, the automatic switching between the power supply circuits can be implemented while a voltage giving warrant to the load is being maintained. Further, since the stabilized power supply circuit placed in the overvoltage state can be accurately specified, the subsequent treatment for it becomes also perfect.

Thus, the present invention is extremely suitable for use in a power supply or the like that must maintain the voltage warranted against the load even if power applied to an AV server, a computer device or the like is instantaneously cut off.



WHAT IS CLAIMED IS:

1. A redundant stabilized power supply suitable for a parallel operation, for supplying two stabilized power supply circuits to a load in parallel and simultaneously driving the load, said each power supply circuit including:

 overvoltage detecting means for detecting an overvoltage applied to a load end;

 current detecting means for detecting a current flowing in a power supply line; and

 power supply control means, and

 wherein when a state of the overvoltage applied across the load is detected and a current detection output at that time remains unchanged, said power supply control means is controlled so as to cut off the supply of power from the stabilized power supply circuit which serves as the overvoltage side.

2. A redundant stabilized power supply according to claim 1, wherein when said one stabilized power supply circuit is cut off, the load is driven by the other stabilized power supply circuit alone.

3. A redundant stabilized power supply wherein said overvoltage detecting means is constructed such that a shunt



regulator is electrically connected to a power supply line through a resistor and a voltage at a middle point between the shunt regulator and the resistor is supplied to an inverter and

said voltage at the middle point is utilized as an overvoltage detection voltage.

4. A redundant stabilized power supply according to claim 1, wherein said overcurrent detecting means includes a voltage comparator provided so as to detect an output current as a voltage change and

said overcurrent detecting means is constructed such that a reference voltage is applied to one portion of the voltage comparator and a voltage drop incident to a line impedance between a sense end of the load and a current detection end of a signal line is supplied to the other portion thereof.

5. A redundant stabilized power supply according to claim 1, wherein the other stabilized power supply circuit is cut off by the voltage outputted from the stabilized power supply circuit serving as the overvoltage side and

said overcurrent detecting means provided within the other stabilized power supply circuit is constructed such that



a comparison output of the voltage comparator provided within said overcurrent detecting means is inverted by an output current at the time of the cutting off of the other stabilized power supply circuit to prevent a power supply control signal from being outputted to said power supply control means provided within the other stabilized power supply circuit.

6. A redundant stabilized power supply according to claim 1, wherein when the AND of an output detected by said overvoltage detecting means and an output detected by said overcurrent detecting means is obtained as an output, said power supply control means is controlled so that the supply of the power is cut off.

7. A redundant stabilized power supply according to claim 1, wherein said power supply control means uses a switching element such as an SCR or the like.

REDUNDANT STABILIZED POWER SUPPLY**ABSTRACT OF DISCLOSURE**

To permit a reliable distinction of a power supply circuit on the overvoltage side.

An overvoltage state is detected from a voltage at a load end (point c). Noting the state of an unbalance between output currents I_a and I_b , which is produced upon the overvoltage state, a voltage drop developed between a sense end c with respect to a load 12 and a power supply line I_a' through which the output current flows, is detected. When an output voltage becomes high, a voltage drop produced by a line impedance from the load end to an overcurrent detection end further increases correspondingly. When the output current on the cut-off side reaches zero and the output current becomes zero, the voltage drop is also brought to zero. A distinction as to which power supply circuit would be in the overvoltage state, is done by ANDing a current detection output C_i produced due to the difference between the output currents and an output C_v at the time that the overvoltage has been detected.

Figure 1

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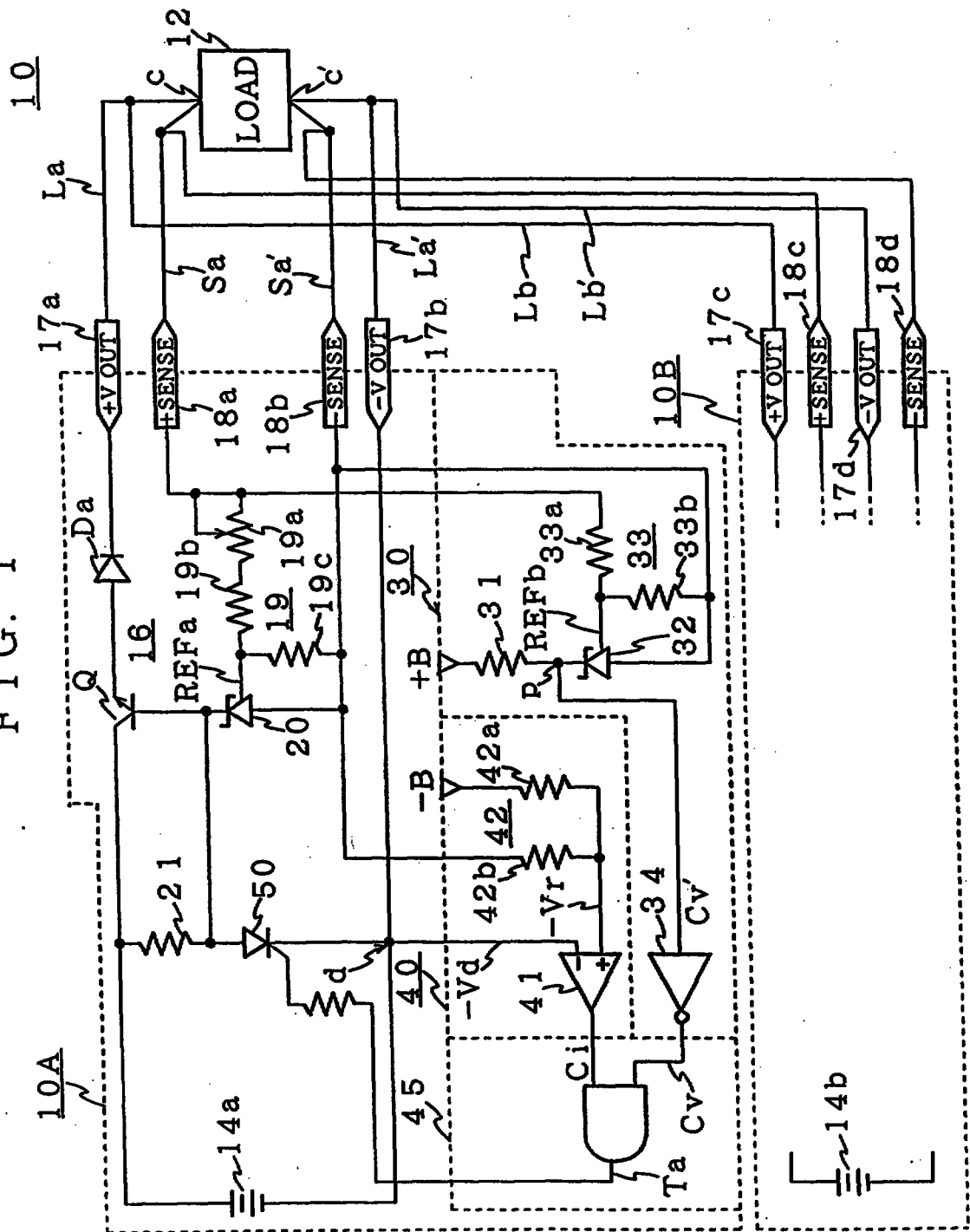


FIG. 2

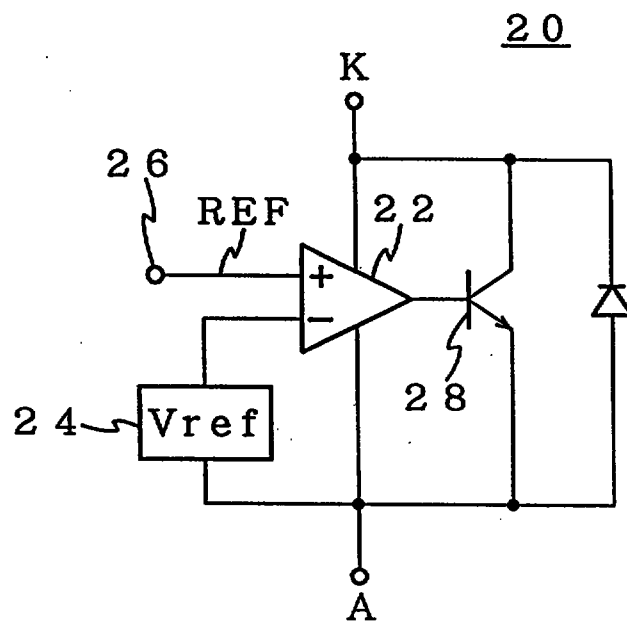


FIG. 3

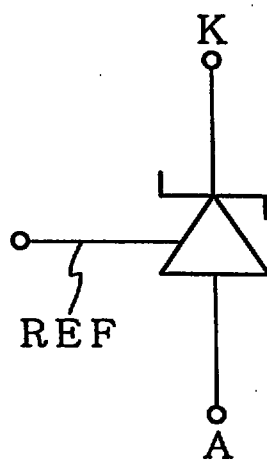


FIG. 4A
VOLTAGE/
CURRENT
WAVEFORM

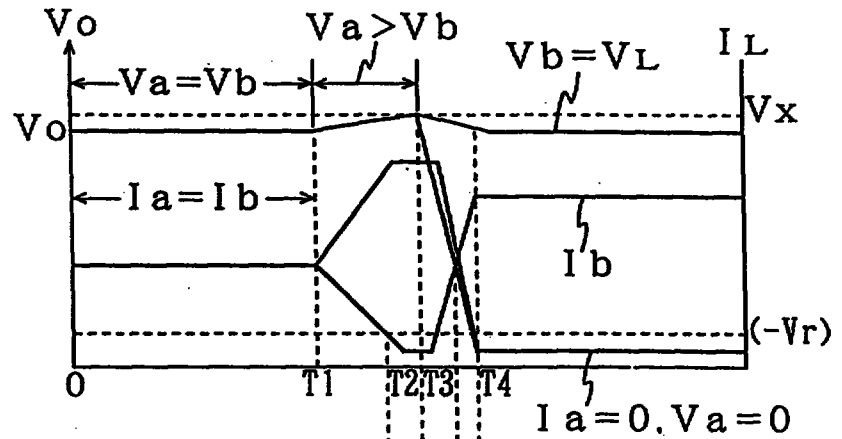


FIG. 4B
FIRST CURRENT
DETECTION
OUTPUT C_i

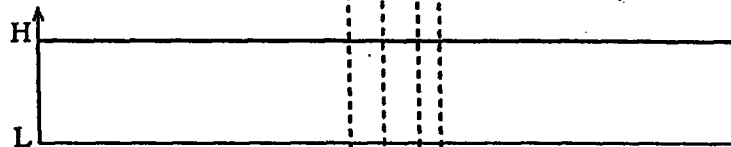


FIG. 4C
OVERVOLTAGE
DETECTION
OUTPUT C_v

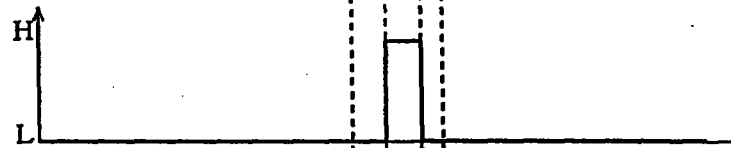


FIG. 4D
FIRST POWER
CONTROL SIGNAL
 T_a

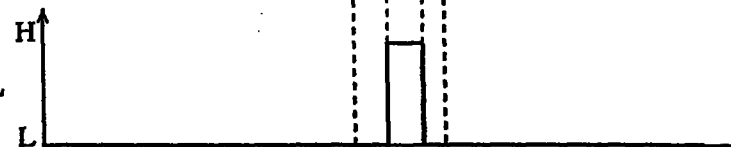


FIG. 4E
SECOND CURRENT
DETECTION
OUTPUT C_i

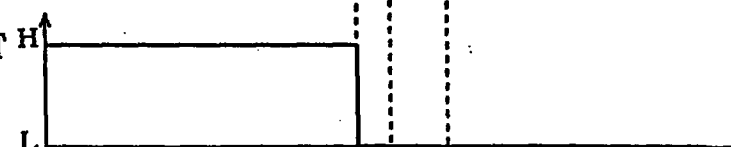


FIG. 4F
SECOND POWER
CONTROL SIGNAL
 T_b

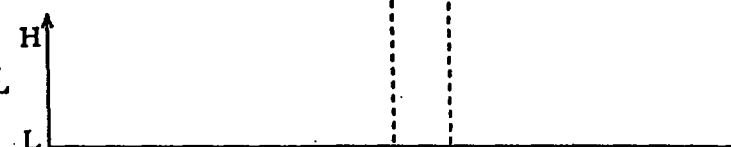
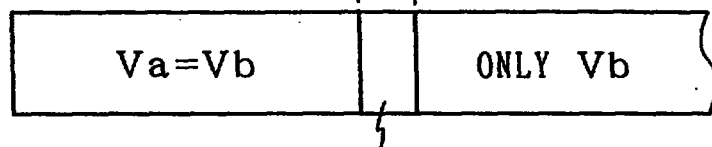


FIG. 4G
LOAD SUPPLY
SOURCE



ONLY V_a (SUPPLY OF VOLTAGE BY DISCHARGE CURRENT)

FIG. 5 (PRIOR ART)

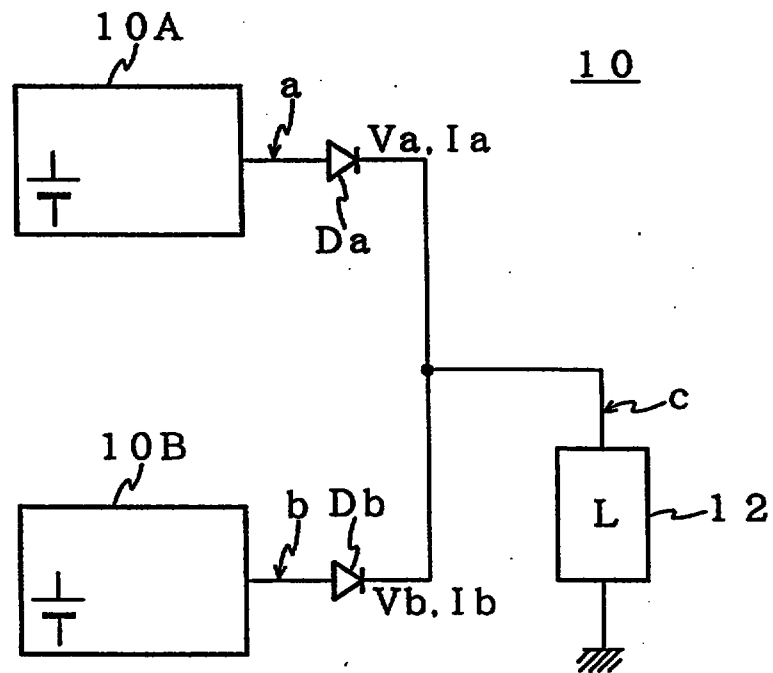


FIG. 6 (PRIOR ART)

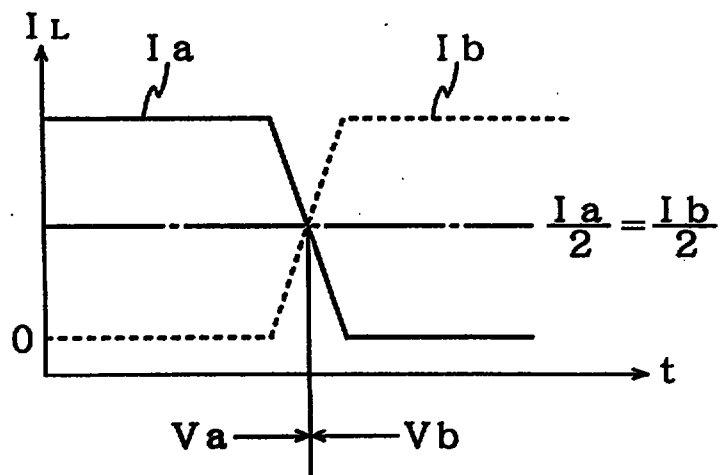
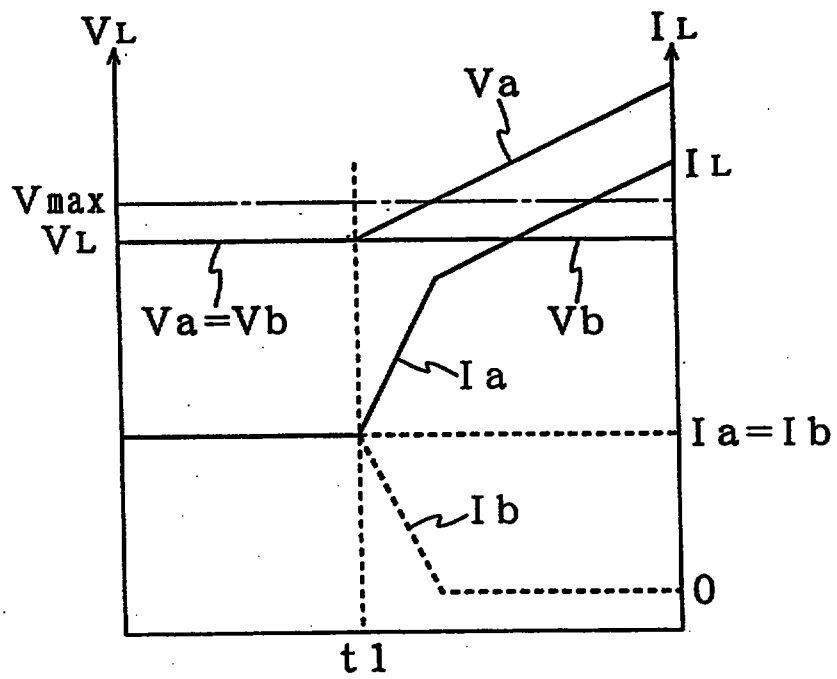


FIG. 7 (PRIOR ART)



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VCS WILL BY 2