METHODS OF FORMING SOLDER BUMPS ON EXPOSED METAL PADS AND RELATED STRUCTURES

Related Application

[0001] This application claims the benefit of priority from U.S. Provisional Patent Application No. 60/561,863 filed on April 13, 2004, the disclosure of which is hereby incorporated herein by reference in its entirety.

Field Of The Invention

[0002] The present application relates to the field of electronics, and more particularly, to methods of forming interconnection bumps and related structures.

Background Of The Invention

[0003] C4 (Controlled-Collapse Chip Connection) is used to connect IC (integrated circuit) chips to substrates in electronic packages. Moreover, C4 is a flip-chip technology in which the interconnections may be provided using relatively small solder balls on the chip surface. Because it is an area array, C4 technology may provide relatively high densities for chip interconnections.

[0004] C4 technology has been used since the 1960s and has proven reliable in the semiconductor field. Historically, PbSn (lead-tin) solder has been evaporated through a metal mask. In the 1990s, electrochemical fabrication of C4 interconnections was introduced. See, for example, M. Datta, et al., "Electrochemical Fabrication of Mechanically Robust PbSn Interconnections", J. Electrochem. Soc., 142, 3779 (1995), U.S. Pat. No. 5,162,257 to Yung, and WO 96/30933, the disclosures of which are hereby incorporated herein in their entirety by reference. Electroplating may be more extendible than evaporation to small C4-pad dimensions, and may provide closer pad spacing, larger wafers, and/or lower-melting solders (having a higher content of Sn).

[0005] U.S. Patent No. 5,937,320 discusses barrier layers for electroplated PbSn eutectic solder joints. An electrochemically fabricated C4 interconnection may have a barrier layer between the electroplated tin-rich solder bump and the ball-limiting

metallurgy that protects the terminal metal in the ball-limiting metallurgy from attack by the Sn in the solder. The barrier layer may be electroplated through the same photoresist mask as the solder and thus may not require a separate patterning step. A thin layer of electroplated nickel may serve as a reliable barrier layer between a copper-based ball-limiting metallurgy and a tin-lead (PbSn) eutectic C4 ball. U.S. Patent No. 6,622,907 discusses a sacrificial seed layer process for forming C4 solder balls. The disclosures of U.S. Patent No. 5,937,320 and U.S. Patent No. 6,622,907 are hereby incorporated herein in their entirety by reference.

Summary

[0006] According to embodiments of the present invention, methods of forming an electronic structure may include providing a substrate having a metal pad thereon. A conductive barrier layer may be formed on a first portion of the metal pad with a second exposed portion of the metal pad remaining free of the conductive barrier layer. In addition, an interconnection structure may be provided on the conductive barrier layer so that the conductive barrier layer is between the interconnection structure and the metal pad and so that the interconnection structure and the conductive barrier layer include different materials.

[0007] More particularly, forming the conductive barrier layer may include forming a conductive seed layer on the metal pad and on the substrate. The conductive barrier layer may be selectively formed on a portion of the conductive seed layer on the first portion of the metal pad so that a second portion of the seed layer on the second portion of the metal pad is free of the conductive barrier layer. The second portion of the seed layer may then be removed from the second portion of the metal pad after selectively forming the conductive barrier layer. Moreover, removing the second portion of the seed layer may include etching the second portion of the seed layer using an etch chemistry that etches at least a portion of the conductive seed layer preferentially with respect to the conductive barrier layer and the metal pad.

[0008] The exposed second portion of the metal pad may surround the conductive barrier layer, or a portion of the conductive barrier layer may extend beyond an edge of the metal pad. In addition, an insulating passivation layer may be formed on

the substrate surrounding the metal pad, with the insulating passivation layer extending on an edge portion of the metal pad so that the second portion of the metal pad is exposed between the conductive barrier layer and the insulating passivation layer. A portion of the conductive barrier layer may also extend on a portion of the insulating passivation layer. In addition or in alternatives, a center of the conductive barrier layer may be substantially aligned with respect to a center of the metal pad, or a center of the conductive barrier layer may be substantially offset with respect to a center of the metal pad.

[0009] A second metal pad may also be provided on the substrate, and the first and second metal pads may be spaced apart. A second conductive barrier layer may also be formed on a portion of the second metal pad, and an alignment of the first conductive barrier layer relative to the first metal pad may be different than an alignment of the second conductive barrier layer relative to the second metal pad. For example, the first conductive barrier layer may be substantially aligned relative to the first metal pad, and the second conductive barrier layer may be substantially offset relative to the second metal pad. In an alternative, the first conductive barrier layer may be substantially offset in a first direction relative to the first metal pad, and the second conductive barrier layer may be substantially offset in a second direction relative to the second metal pad, and the first and second directions may be different.

[0010] The interconnection structure may include a solder bump and/or a copper post. In addition, the metal pad may include aluminum, copper, gold, and/or alloys thereof, the conductive barrier layer may include nickel, copper, and/or alloys thereof, and the interconnection structure may include solder and/or copper. The metal pad may include aluminum, and the conductive barrier layer may include nickel.

[0011] According to additional embodiments of the present invention, an electronic structure may include a substrate having a metal pad thereon. A conductive barrier layer may be on a first portion of the metal pad with a second exposed portion of the metal pad being free of the conductive barrier layer. An interconnection structure may be provided on the conductive barrier layer so that the conductive barrier layer is between the interconnection structure and the metal pad and so that the interconnection structure and the conductive barrier layer include different materials.

[0012] For example, the exposed second portion of the metal pad may surround the conductive barrier layer, or a portion of the conductive barrier layer may extend beyond an edge of the metal pad. In addition, an insulating passivation layer on the substrate may surround the metal pad, and the insulating passivation layer may extend on an edge portion of the metal pad so that the second portion of the metal pad is exposed between the conductive barrier layer and the insulating passivation layer. Moreover, a portion of the conductive barrier layer may extend on a portion of the insulating passivation layer. A center of the conductive barrier layer may be substantially aligned with respect to a center of the metal pad, or a center of the conductive barrier layer may be substantially offset with respect to a center of the metal pad.

[0013] In addition, a second metal pad may be provided on the substrate with the first and second metal pads being spaced apart, and a second conductive barrier layer may be provided on a portion of the second metal pad. More particularly, an alignment of the first conductive barrier layer relative to the first metal pad may be different than an alignment of the second conductive barrier layer relative to the second metal pad. The first conductive barrier layer may be substantially aligned relative to the first metal pad, and the second conductive barrier layer may be substantially offset relative to the second metal pad. In an alternative, the first conductive barrier layer may be substantially offset in a first direction relative to the first metal pad, and the second conductive barrier layer may be substantially offset in a second direction relative to the second metal pad with the first and second directions being different.

[0014] The interconnection structure may include a solder bump and/or a copper post, and a seed layer may be provided between the conductive barrier layer and the metal pad, with the seed layer and the conductive barrier layer including different materials. The metal pad may include aluminum, copper, gold, and/or alloys thereof; the conductive barrier layer may include nickel, copper, and/or alloys thereof; and the interconnection structure may include solder and/or copper. More particularly, the metal pad may include aluminum and the conductive barrier layer may include nickel.

[0015] According to still additional embodiments of the present invention, methods of forming an electronic structure may include providing a substrate having a metal pad thereon. An underbump metallurgy layer may be formed on a surface of the

metal pad with the metal pad being between the underbump metallurgy layer and the substrate. A barrier layer may be formed on the underbump metallurgy layer with the underbump metallurgy layer being between the barrier layer and the metal pad. Moreover, an entirety of the barrier layer may be conformal with respect to the surface of the metal pad, and the barrier layer and the underbump metallurgy layers may include different materials. In addition, a solder bump may be formed on the barrier layer with the barrier layer being between the solder bump and the underbump metallurgy layer, and the barrier layer and the solder bump may include different materials.

[0016] According to yet additional embodiments of the present invention, methods of forming an electronic structure may include providing a substrate having a metal pad thereon. An underbump metallurgy layer may be formed on a surface of the metal pad with the metal pad being between the underbump metallurgy layer and the substrate. A barrier layer may be formed on the underbump metallurgy layer with the underbump metallurgy layer being between the barrier layer and the metal pad, and the barrier layer and the underbump metallurgy layer may include different materials. Moreover, a solder bump may be formed on the barrier layer with the barrier layer being between the solder bump and the underbump metallurgy layer. The barrier layer and the solder bump may include different materials, and a portion of the metal pad may be exposed adjacent to the underbump metallurgy layer, the barrier layer, and the solder bump.

[0017] According to more embodiments of the present invention, an electronic structure may include a substrate having a metal pad thereon and an underbump metallurgy layer on a surface of the metal pad with the metal pad being between the underbump metallurgy layer and the substrate. A barrier layer may be provided on the underbump metallurgy layer with the underbump metallurgy layer being between the barrier layer and the metal pad. Moreover, an entirety of the barrier layer may be conformal with respect to the surface of the metal pad, and the barrier layer and the underbump metallurgy layers may include different materials. In addition, a solder bump may be provided on the barrier layer with the barrier layer being between the solder bump and the underbump metallurgy layer, and the barrier layer and the solder bump may include different materials.

[0018] According to still more embodiments of the present invention, an electronic structure may include a substrate having a metal pad thereon and an underbump metallurgy layer on a surface of the metal pad with the metal pad being between the underbump metallurgy layer and the substrate. A barrier layer may be provided on the underbump metallurgy layer with the underbump metallurgy layer being between the barrier layer and the metal pad, and the barrier layer and the underbump metallurgy layer may include different materials. In addition, a solder bump may be provided on the barrier layer with the barrier layer being between the solder bump and the underbump metallurgy layer. The barrier layer and the solder bump may include different materials, and a portion of the metal pad may be exposed adjacent to the underbump metallurgy layer, the barrier layer, and the solder bump.

Brief Description Of The Drawings

[0019] Figures 1A-C are cross-sectional views illustrating steps of forming electronic structures according to embodiments of the present invention.

[0020] Figures 2A-C are cross-sectional views illustrating steps of forming electronic structures according to additional embodiments of the present invention.

[0021] Figures 3A-B are cross-sectional views illustrating steps of forming electronic structures according to still additional embodiments of the present invention.

[0022] Figures 4A-C are cross-sectional views illustrating steps of forming electronic structures according to yet additional embodiments of the present invention.

[0023] Figures 5, 6, and 7 are plan views of electronic structures according to embodiments of the present invention.

[0024] Figure 8 is a cross-sectional view illustrating a plurality of interconnection structures on a substrate according to embodiments of the present invention.

[0025] Figure 9 is a plan view illustrating an array of interconnection structures according to embodiments of the present invention.

[0026] Figures 10A-B are respective plan and cross-sectional views illustrating a plurality of interconnection structures on a substrate according to embodiments of the present invention.

Detailed Description

[0027] The present invention now will be described more fully hereinafter with reference to the accompanying drawings, in which embodiments of the invention are shown. This invention may, however, be embodied in many different forms and should not be construed as limited to the embodiments set forth herein. Rather, these embodiments are provided so that this disclosure will be thorough and complete, and will fully convey the scope of the invention to those skilled in the art.

[0028] In the drawings, the thickness of layers and regions are exaggerated for clarity. It will also be understood that when an element such as a layer, region or substrate is referred to as being on another element, it can be directly on the other element or intervening elements may also be present. In contrast, if an element such as a layer, region or substrate is referred to as being directly on another element, then no other intervening elements are present. Similarly, when an element such as a layer, region or substrate is referred to as being coupled or connected to/with another element, it can be directly coupled or connected to/with the other element or intervening elements may also be present. In contrast, if an element such as a layer, region or substrate is referred to as being directly coupled or connected to/with another element, then no other intervening elements are present. As used herein, the term "and/or" includes any and all combinations of one or more of the associated listed items. The symbol "/" is also used as a shorthand notation for "and/or".

[0029] Furthermore, relative terms, such as beneath, upper, lower, top, and/or bottom may be used herein to describe one element's relationship to another element as illustrated in the figures. It will be understood that relative terms are intended to encompass different orientations of the device in addition to the orientation depicted in the figures. For example, if the device in one of the figures is turned over, elements described as below other elements would then be oriented above the other elements. The exemplary term below, can therefore, encompasses both an orientation of above and below.

[0030] It will be understood that although the terms first and second are used herein to describe various regions, layers and/or sections, these regions, layers and/or

sections should not be limited by these terms. These terms are only used to distinguish one region, layer or section from another region, layer or section. Thus, a first region, layer or section discussed below could be termed a second region, layer or section, and similarly, a second region, layer or section could be termed a first region, layer or section without departing from the teachings of the present invention. Like numbers refer to like elements throughout.

[0031] The terminology used herein is for the purpose of describing particular embodiments only and is not intended to be limiting of the invention. As used herein, the singular forms "a", "an" and "the" are intended to include the plural forms as well, unless the context clearly indicates otherwise. It will be further understood that the terms "comprises" and/or "comprising," when used in this specification, specify the presence of stated features, integers, steps, operations, elements, and/or components, but do not preclude the presence or addition of one or more other features, integers, steps, operations, elements, components, and/or groups thereof. As used herein, the term "laterally" refers to a direction parallel to a surface of a substrate or die on which solder has been plated.

[0032] Unless otherwise defined, all terms (including technical and scientific terms) used herein have the same meaning as commonly understood by one of ordinary skill in the art to which this invention belongs. It will be further understood that terms, such as those defined in commonly used dictionaries, should be interpreted as having a meaning that is consistent with their meaning in the context of the relevant art and will not be interpreted in an idealized or overly formal sense unless expressly so defined herein.

[0033] When forming a solder bump on an existing device (input/output) pad, the device (input/output) pad may be sealed with an underbump metallurgy and/or passivation layer so that portions of the device pad are protected from the solder bump and/or from the environment. Such a structure, however, may result in a solder bump with a dimension larger than an exposed portion of the device pad. Accordingly, shorts between adjacent solder bumps may occur during reflow if the solder bumps extend laterally taking on a super-hemispheric profile.

[0034] A size of an exposed portion of an input/output pad may be reduced by forming and patterning an additional passivation layer thereon. In an alternative, an input/output pad may be reconfigured using a redistribution layer. Use of an additional passivation layer and/or a redistribution layer, however, may increase cost and/or complexity.

[0035] Methods and structures according to some embodiments of the present invention may provide a solder bump with dimensions smaller than an exposed portion of the device pad on which the solder bump is formed. Accordingly, bumping on tighter pitch designs may be provided without requiring forming an additional passivation layer on the device pad before bumping.

[0036] According to first embodiments of the present invention illustrated in the cross-sectional views of Figures 1A and 1B, a substrate **101** may be provided with a metal pad **103** thereon wherein the metal pad **103** is free of any passivation layer thereon. The substrate **101** may be an integrated circuit substrate including integrated circuit devices therein, and the metal pad **103** may provide electrical connection with integrated circuit devices of the substrate **101**. More particularly, an exposed surface of the metal pad **103** may comprise aluminum, gold, copper, and/or alloys thereof.

[0037] An underbump metallurgy (seed) layer **105** may then be formed on the metal pad **103** and on the substrate **101** to facilitate subsequent electroplating. The underbump metallurgy (seed) layer **105** may include an adhesion layer adjacent the substrate **101** and metal pad **103** and a conduction layer on the adhesion layer opposite the substrate **101** and metal pad **103**. More particularly, the adhesion layer may include titanium-tungsten (TiW), and the conduction layer may include copper (Cu), Silver (Ag), gold (Au), Palladium (Pd), and/or alloys thereof. The underbump metallurgy (seed) layer **105** may also include an intermediate layer between adhesion and conduction layers, and the intermediate layer may include titanium (Ti) and/or titanium nitride (TiN).

[0038] A plating stencil (mask) **107** is then formed on the underbump metallurgy (seed) layer **105**, and a hole **108** in the plating stencil **107** exposes portions of the underbump metallurgy (seed) layer **105**. More particularly, the hole **108** exposes an area of the underbump metallurgy (seed) layer **105** that is less than an area of the metal pad **103** so that portions of the metal pad **103** extend beyond boundaries of the hole **108**

as shown in Figure 1A. The plating stencil (mask) **107**, for example, may be a layer of an organic or inorganic photo-imagable material such as photoresist, and the hole may be formed using photolithography. More particularly, the plating stencil (mask) **107** may be formed by spinning or laminating the material on the underbump metallurgy (seed) layer **105**, baking the material, selectively exposing the material to radiation (such as light), and developing the material to form the hole **108**. In addition or in an alternative, the plating stencil (mask) **107** may be formed using electro-deposition.

[0039] A barrier layer **109** may then be selectively formed (such as by plating) on portions of the underbump metallurgy (seed) layer **105** exposed through the hole **108**. The barrier layer **109**, for example, may include nickel, copper, and/or alloys thereof. After plating the barrier layer **109**, a solder bump **111** is plated in the hole **108** on the barrier layer **109**. The solder bump **111** may include an alloy such as a tin-lead (SnPb) solder, or the solder bump **111** may be lead free.

[0040] Once the barrier layer **109** and the solder bump **111** are plated, the plating stencil (mask) **107** can be removed as shown in Figure 1B. As further shown in Figure 1B, portions of the underbump metallurgy (seed) layer **105** not covered by the barrier layer **109** and/or solder bump **111** may be removed, and the solder bump **111** may be subjected to reflow to provide a solder ball. For example, exposed portions of the underbump metallurgy (seed) layer **105** may be removed using an etch chemistry that removes the underbump metallurgy (seed) layer selectively with respect to the barrier layer **109**. Accordingly, the patterned underbump metallurgy (seed) layer **105** may be undercut with respect to the barrier layer **109**.

[0041] More particularly, the underbump metallurgy (seed) layer **105** may be removed using an etch chemistry that removes at least a remaining portion of the underbump metallurgy (seed) layer **105** selectively with respect to the metal pad **103**. For example, peroxide (H_2O_2) may be used to remove a TiW adhesion layer of the underbump metallurgy (seed) layer **105** selectively with respect to an aluminum (or other) pad metal **103**. Reflow of the solder bump **111** may be performed after removing a solder wettable conduction layer of the underbump metallurgy (seed) layer **105** but before removing a solder non-wettable adhesion layer of the underbump metallurgy (seed) layer

105 so that the solder bump **111** does not spread across exposed portions of the metal pad **103**.

[0042] In an alternative, the metal pad **103** may include a solder non-wettable metal (such as aluminum) on a surface thereof so that reflow of the solder bump **111** may be performed after removing the underbump metallurgy (seed) layer **105** without the solder bump **111** spreading across exposed portions of the metal pad **103**. In another alternative, reflow of the solder bump **111** may be performed without flux to maintain an oxide thereon so that the solder bump **111** does not spread across an exposed wettable surface such as a conduction layer of the underbump metallurgy (seed) layer **105** (before removing exposed portions of the underbump metallurgy layer) or the metal pad **103** (after removing exposed portions of the underbump metallurgy layer). Reflow of the solder bump **111** may be performed above a liquidus temperature of the solder bump **111**, or reflow of the solder bump **111** may not exceed a liquidus temperature of the solder bump **111**. In yet another alternative, the solder bump **111** may not be subjected to reflow.

[0043] As shown in Figure 1B, central portions of the metal pad **103** may be covered by the remaining portions of the underbump metallurgy (seed) layer **105**, the barrier layer **109**, and the solder bump **111**. Edge portions of the metal pad **103**, however, may remain exposed after forming the barrier layer **109** and the solder bump **111**, and/or after reflowing the solder bump **111**.

[0044] As further shown in Figures 1A and 1B, the metal pad **103** may be considered to be "above" a surface of the substrate because an entirety of the metal pad **103** may be exposed before forming the underbump metallurgy (seed) layer **105**, the barrier layer **109**, and the solder bump **111**. Accordingly, a surface portion of the substrate **101** may include an insulating passivation layer, and a hole and/or conductive via through the passivation layer may provide electrical coupling between the metal pad **103** and an electronic circuit(s) of the substrate **101**. According to some embodiments shown in Figure 1B, an entirety of the patterned underbump metallurgy (seed) layer **105** and an entirety of the barrier layer **109** may be conformal with respect to the metal pad **103** such that neither extends beyond an edge of the metal pad. According to other embodiments shown in the cross-sectional views of Figures 1B and 1C, portions of the

patterned underbump metallurgy (seed) layer **105** and the barrier layer **109** (shown in the cross-sectional view of Figure 1C) may extend beyond edges of the metal pad **103** while other portions of the patterned underbump metallurgy (seed) layer and barrier layer (shown in the cross-sectional view of Figure 1B) are set back from edges of the metal pad.

[0045] If the metal pad **103** is square and each of the patterned underbump metallurgy layer **105**, the barrier layer **109**, and the solder bump **111** are maintained within the metal pad **103**, the solder bump **111** may have a circular footprint as shown, for example, in Figure 5. In other embodiments, Figure 1C may be a cross-sectional view taken at an angle with respect to the cross-section of Figure 1B. As shown in Figure 1C, portions of the patterned underbump metallurgy (seed) layer **105**, the barrier layer **109**, and the solder bump **111** may extend beyond the metal pad **103** onto the substrate **103**. If the metal pad **103** is square when viewed from the top, and the cross-sections of Figures 1B and 1C are at an angle of 45 degrees with respect to each other, the solder bump **111** may have a circular footprint as shown, for example, in Figure 6. If the metal pad **103** is square when viewed from the top, and the cross-sections of Figures 1B and 1C are at an angle of 90 degrees with respect to each other, the solder bump **111** may have an oval footprint as shown, for example in Figure 7.

[0046] In alternatives, the underbump metallurgy (seed) layer **105** may be patterned using the barrier layer **109** without the solder bump **111**. The barrier layer **109**, for example, may be selectively formed (such as by plating) on the underbump metallurgy (seed) layer **105**, and portions of the underbump metallurgy (seed) layer **105** exposed by the barrier layer **109** may be selectively removed. After exposed portions of the underbump metallurgy (seed) layer **105** have been selectively removed, a solder bump or other interconnection structure may be provided on the barrier layer **109**. For example, a solid preformed solder structure may be placed on the barrier layer **109**, and/or the barrier layer **109** may be bonded with a solder structure on a second substrate.

[0047] In addition or in an alternative, a conductive post (such as a copper post) may be provided on the barrier layer **109** instead of the solder bump **111** or between the barrier layer **109** and the solder bump **111**. A conductive post may be selectively formed on the barrier layer **109** (such as by plating using plating stencil **107**) before

selectively removing exposed portions of the underbump metallurgy (seed) layer **105**, and/or a conductive post may be placed on the barrier layer **109** after selectively removing exposed portions of the underbump metallurgy (seed) layer **105**. A solder structure may then be formed on the conductive post, and/or a solid preformed solder structure may be placed on the conductive post. In an alternative, the conducive post may be bonded with a solder structure on a second substrate.

[0048] According to second embodiments of the present invention illustrated in the cross-sectional views of Figures 2A and 2B, a substrate **201** may be provided with a metal pad **203** and an inorganic dielectric passivation layer **204** (such as silicon oxide layer) thereon. For example, the inorganic passivation layer **204** may be formed over the substrate **201** and the metal pad **203** and then patterned to expose portions of the metal pad **203**. The substrate **201** may be an integrated circuit substrate including integrated circuit devices therein, and the metal pad **203** may provide electrical connection with integrated circuit devices of the substrate **201**. More particularly, an exposed surface of the metal pad **203** may comprise aluminum, gold, copper, and/or alloys thereof.

[0049] An underbump metallurgy (seed) layer **205** may then be formed on the metal pad **203** and on the inorganic passivation layer **204** to facilitate subsequent electroplating. The underbump metallurgy (seed) layer **205** may include an adhesion layer adjacent the passivation layer **204** and metal pad **203** and a conduction layer on the adhesion layer opposite the passivation layer **204** and metal pad **203**. More particularly, the adhesion layer may include titanium-tungsten (TiW), and the conduction layer may include copper (Cu), Silver (Ag), gold (Au), Palladium (Pd), and/or alloys thereof. The underbump metallurgy (seed) layer **205** may also include an intermediate layer between adhesion and conduction layers, and the intermediate layer may include titanium (Ti) and/or titanium nitride (TiN).

[0050] A plating stencil (mask) **207** is then formed on the underbump metallurgy (seed) layer **205**, and a hole **208** in the plating stencil **207** exposes portions of the underbump metallurgy (seed) layer **205**. More particularly, the hole **208** exposes an area of the underbump metallurgy (seed) layer **205** that is less than an area of the metal pad **203** exposed by the passivation layer **204** so that portions of the metal pad **203** exposed by the passivation layer **204** extend beyond boundaries of the hole **208** as shown

in Figure 2A. The plating stencil (mask) **207**, for example, may be a layer of an organic or inorganic photo-imagable material such as photoresist, and the hole may be formed using photolithography. More particularly, the plating stencil (mask) **207** may be formed by spinning or laminating the material on the underbump metallurgy (seed) layer **205**, baking the material, selectively exposing the material to radiation (such as light), and developing the material to form the hole **208**. In addition or in an alternative, the plating stencil (mask) **207** may be formed using electro-deposition.

[0051] A barrier layer **209** may then selectively formed (such as by plating) on portions of the underbump metallurgy (seed) layer **205** exposed through the hole **208**. The barrier layer **209**, for example, may include nickel, copper, and/or alloys thereof. After plating the barrier layer **209**, a solder bump **211** is plated in the hole **208** on the barrier layer **209**. The solder bump **211** may include an alloy such as a tin-lead (SnPb) solder, or the solder bump **211** may be lead free.

[0052] Once the barrier layer **209** and the solder bump **211** are plated, the plating stencil (mask) **207** can be removed as shown in Figure 2B. As further shown in Figure 2B, portions of the underbump metallurgy (seed) layer **205** not covered by the barrier layer **209** and/or solder bump **211** may be removed, and the solder bump **211** may be subjected to reflow to provide a solder ball. For example, exposed portions of the underbump metallurgy (seed) layer **205** may be removed using an etch chemistry that removes the underbump metallurgy (seed) layer selectively with respect to the barrier layer **209**. Accordingly, the patterned underbump metallurgy (seed) layer **205** may be undercut with respect to the barrier layer **209**.

[0053] More particularly, the underbump metallurgy (seed) layer **205** may be removed using an etch chemistry that removes at least a remaining portion of the underbump metallurgy (seed) layer **205** selectively with respect to the metal pad **203**. For example, peroxide (H_2O_2) may be used to remove a TiW adhesion layer of the underbump metallurgy (seed) layer **205** selectively with respect to an aluminum (or other) pad metal **203**. Reflow of the solder bump **211** may be performed after removing a solder wettable conduction layer of the underbump metallurgy (seed) layer **205** but before removing a solder non-wettable adhesion layer of the underbump metallurgy (seed) layer

205 so that the solder bump **211** does not spread across exposed portions of the metal pad **203**.

[0054] In an alternative, the metal pad **203** may include a solder non-wettable metal (such as aluminum) on a surface thereof so that reflow of the solder bump **211** may be performed after removing the underbump metallurgy (seed) layer **205** without the solder bump **211** spreading across exposed portions of the metal pad **203**. In another alternative, reflow of the solder bump **211** may be performed without flux to maintain an oxide thereon so that the solder bump **211** does not spread across an exposed wettable surface such as a conduction layer of the underbump metallurgy (seed) layer **205** (before removing exposed portions of the underbump metallurgy layer) or the metal pad **203** (after removing exposed portions of the underbump metallurgy layer). Reflow of the solder bump **211** may be performed above a liquidus temperature of the solder bump **211**, or reflow of the solder bump **211** may not exceed a liquidus temperature of the solder bump **211**. In yet another alternative, the solder bump **211** may not be subjected to reflow.

[0055] As shown in Figure 2B, edge portions of the metal pad **203** may be covered by the passivation layer **204**, and central portions of the metal pad **203** may be covered by the remaining portions of the underbump metallurgy (seed) layer **205**, the barrier layer **209**, and the solder bump **211**. Portions of the metal pad **203** between the passivation layer **204** and the patterned underbump metallurgy layer **205**, however, may remain exposed after forming the barrier layer **209** and the solder bump **211**, and/or after reflowing the solder bump **211**.

[0056] As further shown in Figures 2A and 2B, the metal pad **203** may be considered to be "below" or "beneath" a surface of the substrate because portions of the metal pad **203** may be covered by the passivation layer **204** before forming the underbump metallurgy (seed) layer **205**, the barrier layer **209**, and the solder bump **211**. Stated in other words, the passivation layer **204** may be considered as a part of the substrate. According to some embodiments shown in Figure 2B, an entirety of the patterned underbump metallurgy (seed) layer **205** and an entirety of the barrier layer **209** may be conformal with respect to the metal pad **203** such that neither extends beyond an edge of the metal pad or onto the passivation layer. According to other embodiments

shown in the cross-sectional views of Figure 2B and 2C, portions of the patterned underbump metallurgy (seed) layer **205** and the barrier layer **209** (shown in the cross-sectional view of Figure 2C) may extend to and/or overlap the passivation layer **204** while other portions of the patterned underbump metallurgy (seed) layer and barrier layer (shown in the cross-sectional view of Figure 2B) are set back from the passivation layer.

[0057] If the metal pad **203** is square and each of the patterned underbump metallurgy layer **205**, the barrier layer **209**, and the solder bump **211** are maintained within the metal pad **203**, the solder bump **211** may have a circular footprint as shown, for example, in Figure 5. In other embodiments, Figure 1C may be a cross-sectional view taken at an angle with respect to the cross-section of Figure 1B. As shown in Figure 1C, portions of the patterned underbump metallurgy (seed) layer **205**, the barrier layer **209**, and the solder bump **211** may extend beyond the metal pad **203** onto the passivation layer **204**. If the metal pad **203** is square when viewed from the top, and the cross-sections of Figures 1B and 1C are at an angle of 45 degrees with respect to each other, the solder bump **211** may have a circular footprint as shown, for example, in Figure 6. If the metal pad **203** is square when viewed from the top, and the cross-sections of Figures 1B and 1C are at an angle of 90 degrees with respect to each other, the solder bump **211** may have an oval footprint as shown, for example in Figure 7.

[0058] In alternatives, the underbump metallurgy (seed) layer **205** may be patterned using the barrier layer **209** without the solder bump **211**. The barrier layer **209**, for example, may be selectively formed (such as by plating) on the underbump metallurgy (seed) layer **205**, and portions of the underbump metallurgy (seed) layer **205** exposed by the barrier layer **209** may be selectively removed. After exposed portions of the underbump metallurgy (seed) layer **205** have been selectively removed, a solder bump or other interconnection structure may be provided on the barrier layer **209**. For example, a solid preformed solder structure may be placed on the barrier layer **209**, and/or the barrier layer **209** may be bonded with a solder structure on a second substrate.

[0059] In addition or in an alternative, a conductive post (such as a copper post) may be provided on the barrier layer **209** instead of the solder bump **211** or between the barrier layer **209** and the solder bump **211**. A conductive post may be selectively formed on the barrier layer **209** (such as by plating using plating stencil **207**) before

selectively removing exposed portions of the underbump metallurgy (seed) layer **205**, and/or a conductive post may be placed on the barrier layer **209** after selectively removing exposed portions of the underbump metallurgy (seed) layer **205**. A solder structure may then be formed on the conductive post, and/or a solid preformed solder structure may be placed on the conductive post. In an alternative, the conducive post may be bonded with a solder structure on a second substrate.

[0060] According to third embodiments of the present invention illustrated in the cross-sectional views of Figures 3A and 3B, a substrate **301** may be provided with a metal pad **303** and an inorganic dielectric passivation layer **304a** (such as silicon oxide layer) and an organic passivation layer **304b** (such as polyimide) thereon. For example, the inorganic passivation layer **304a** may be formed over the substrate **301** and the metal pad **303** and then patterned to expose portions of the metal pad **303**. The organic passivation layer **304b** may then be formed on the inorganic passivation layer **304a** and on the metal pad **303** and patterned to expose portions of the metal pad **303**.

[0061] The substrate **301** may be an integrated circuit substrate including integrated circuit devices therein, and the metal pad **303** may provide electrical connection with integrated circuit devices of the substrate **301**. More particularly, an exposed surface of the metal pad **303** may comprise aluminum, gold, copper, and/or alloys thereof.

[0062] An underbump metallurgy (seed) layer **305** may then be formed on the metal pad **303** and on the organic passivation layer **304b** to facilitate subsequent electroplating. The underbump metallurgy (seed) layer **305** may include an adhesion layer adjacent the organic passivation layer **304b** and metal pad **303** and a conduction layer on the adhesion layer opposite the organic passivation layer **304b** and metal pad **303**. More particularly, the adhesion layer may include titanium-tungsten (TiW), and the conduction layer may include copper (Cu), Silver (Ag), gold (Au), Palladium (Pd), and/or alloys thereof. The underbump metallurgy (seed) layer **305** may also include an intermediate layer between adhesion and conduction layers, and the intermediate layer may include titanium (Ti) and/or titanium nitride (TiN).

[0063] A plating stencil (mask) **307** is then formed on the underbump metallurgy (seed) layer **305**, and a hole **308** in the plating stencil **307** exposes portions of

the underbump metallurgy (seed) layer **305**. More particularly, the hole **308** exposes an area of the underbump metallurgy (seed) layer **305** that no greater than an area of the metal pad **303** exposed by the organic passivation layer **304b** so that portions of the underbump metallurgy (seed) layer **305** exposed by the hole **308** do not extend over the organic passivation layer **304b** as shown in Figure 3A. The plating stencil (mask) **307**, for example, may be a layer of an organic or inorganic photo-imagable material such as photoresist, and the hole may be formed using photolithography. More particularly, the plating stencil (mask) **307** may be formed by spinning or laminating the material on the underbump metallurgy (seed) layer **305**, baking the material, selectively exposing the material to radiation (such as light), and developing the material to form the hole **308**. In addition or in an alternative, the plating stencil (mask) **307** may be formed using electro-deposition.

[0064] A barrier layer **309** may then be selectively formed (such as by plating) on portions of the underbump metallurgy (seed) layer **305** exposed through the hole **308**. The barrier layer **309**, for example, may include nickel, copper, and/or alloys thereof. After plating the barrier layer **309**, a solder bump **311** is plated in the hole **308** on the barrier layer **309**. The solder bump **311** may include an alloy such as a tin-lead (SnPb) solder, or the solder bump **311** may be lead free.

[0065] Once the barrier layer **309** and the solder bump **311** are plated, the plating stencil (mask) **307** can be removed as shown in Figure 3B. As further shown in Figure 3B, portions of the underbump metallurgy (seed) layer **305** not covered by the barrier layer **309** and/or solder bump **311** may be removed, and the solder bump **311** may be subjected to reflow to provide a solder ball. For example, exposed portions of the underbump metallurgy (seed) layer **305** may be removed using an etch chemistry that removes the underbump metallurgy (seed) layer selectively with respect to the barrier layer **309**. Accordingly, the patterned underbump metallurgy (seed) layer **305** may be undercut with respect to the barrier layer **309**.

[0066] More particularly, the underbump metallurgy (seed) layer **305** may be removed using an etch chemistry that removes at least a remaining portion of the underbump metallurgy (seed) layer **305** selectively with respect to the metal pad **303** and/or the organic passivation layer **304b**. For example, peroxide (H_2O_2) may be used to

remove a TiW adhesion layer of the underbump metallurgy (seed) layer **305** selectively with respect to an aluminum (or other) pad metal **303**. Reflow of the solder bump **311** may be performed after removing a solder wettable conduction layer of the underbump metallurgy (seed) layer **305** but before removing a solder non-wettable adhesion layer of the underbump metallurgy (seed) layer **305** so that the solder bump **311** does not spread across exposed portions of the metal pad **303**.

[0067] In an alternative, the metal pad **303** may include a solder non-wettable metal (such as aluminum) on a surface thereof so that reflow of the solder bump **311** may be performed after removing the underbump metallurgy (seed) layer **305** without the solder bump **311** spreading across exposed portions of the metal pad **303**. In another alternative, reflow of the solder bump **311** may be performed without flux to maintain an oxide thereon so that the solder bump **311** does not spread across an exposed wettable surface such as a conduction layer of the underbump metallurgy (seed) layer **305** (before removing exposed portions of the underbump metallurgy layer) or the metal pad **303** (after removing exposed portions of the underbump metallurgy layer). In still another alternative, the organic passivation layer **304b** may act as a solder dam to confine the solder bump **311** during reflow.

[0068] Reflow of the solder bump **311** may be performed above a liquidus temperature of the solder bump **311**, or reflow of the solder bump **311** may not exceed a liquidus temperature of the solder bump **311**. In yet another alternative, the solder bump **311** may not be subjected to reflow.

[0069] As shown in Figure 3B, edge portions of the metal pad **303** may be covered by the organic passivation layer **304b**, and central portions of the metal pad **303** may be covered by the remaining portions of the underbump metallurgy (seed) layer **305**, the barrier layer **309**, and the solder bump **311**. According to particular embodiments of the present invention, an entirety of the surface of the metal pad **303** may be covered by the passivation layers **304a-b** and the barrier layer. The barrier layer **309** and/or remaining portions of the underbump metallurgy (seed) layer **305**, however, may not extend onto the organic passivation layer **304b**. An integrity of the patterned underbump metallurgy (seed) layer **305**, the barrier layer **309**, and/or the solder bump **311** may thus be enhanced by not providing portions thereof on the potentially flexible organic

passivation layer **304b**. In an alternative, portions of the metal pad **303** between the passivation layer **304b** and the patterned underbump metallurgy layer **305** may remain exposed after forming the barrier layer **309** and the solder bump **311**, and/or after reflowing the solder bump **311**.

[0070] As further shown in Figures 3A and 3B, the metal pad **303** may be considered to be "below" or "beneath" a surface of the substrate because portions of the metal pad **303** may be covered by the passivation layers **304a** and/or **304b** before forming the underbump metallurgy (seed) layer **305**, the barrier layer **309**, and the solder bump **311**. Stated in other words, the passivation layers **304a** and/or **304b** may be considered as a part of the substrate.

[0071] As shown in Figure 3B, the solder bump **311** may extend beyond the barrier layer **309** in a dimension parallel to the substrate after reflow. Accordingly, the solder bump **311** may partially overlap portions of the passivation layer **304b**. If the passivation layer **304b** exposes a square portion of the metal pad **303** and the barrier layer **309** and solder bump **311** are plated in a circular or oval hole **308** on a circular or oval portion of the metal pad **303**, the solder bump **311** may overlap portions of the passivation layer **304b** in some areas, and portions of the metal pad **303** may remain exposed in other areas, as illustrated, for example, in Figure 6 and/or Figure 7. According to some embodiments shown in Figure 3B, an entirety of the patterned underbump metallurgy (seed) layer **305** and an entirety of the barrier layer **309** may be conformal with respect to the metal pad **303** such that neither extends beyond an edge of the metal pad or onto the passivation layer. According to other embodiments shown in Figures 3B, portions of the patterned underbump metallurgy (seed) layer **305** and the barrier layer **309** (not shown in the cross-sectional view of Figure 3C) may extend to and/or overlap the passivation layers **704b** and/or **704a** while other portions of the patterned underbump metallurgy (seed) layer and barrier layer are set back from the passivation layer.

[0072] In alternatives, the underbump metallurgy (seed) layer **305** may be patterned using the barrier layer **309** without the solder bump **311**. The barrier layer **309**, for example, may be selectively formed (such as by plating) on the underbump metallurgy (seed) layer **305**, and portions of the underbump metallurgy (seed) layer **305**

exposed by the barrier layer **309** may be selectively removed. After exposed portions of the underbump metallurgy (seed) layer **305** have been selectively removed, a solder bump or other interconnection structure may be provided on the barrier layer **309**. For example, a solid preformed solder structure may be placed on the barrier layer **309**, and/or the barrier layer **309** may be bonded with a solder structure on a second substrate.

[0073] In addition or in an alternative, a conductive post (such as a copper post) may be provided on the barrier layer **309** instead of the solder bump **311** or between the barrier layer **309** and the solder bump **311**. A conductive post may be selectively formed on the barrier layer **309** (such as by plating using plating stencil **307**) before selectively removing exposed portions of the underbump metallurgy (seed) layer **305**, and/or a conductive post may be placed on the barrier layer **309** after selectively removing exposed portions of the underbump metallurgy (seed) layer **305**. A solder structure may then be formed on the conductive post, and/or a solid preformed solder structure may be placed on the conductive post. In an alternative, the conducive post may be bonded with a solder structure on a second substrate.

[0074] According to fourth embodiments of the present invention illustrated in the cross-sectional views of Figures 4A and 4B, a substrate **401** may be provided with a metal pad **403** and an inorganic dielectric passivation layer **404a** (such as silicon oxide layer) and an organic passivation layer **404b** (such as polyimide) thereon. For example, the inorganic passivation layer **404a** and the organic passivation layer **404b** may be formed over the substrate **401** and the metal pad **403**. Both the inorganic and organic passivation layers **404a-b** may then be patterned using a single masking step to expose portions of the metal pad **403**.

[0075] The substrate **401** may be an integrated circuit substrate including integrated circuit devices therein, and the metal pad **403** may provide electrical connection with integrated circuit devices of the substrate **401**. More particularly, an exposed surface of the metal pad **403** may comprise aluminum, gold, copper, and/or alloys thereof.

[0076] An underbump metallurgy (seed) layer **405** may then be formed on the metal pad **403** and on the passivation layers **404a-b** to facilitate subsequent electroplating. The underbump metallurgy (seed) layer **405** may include an adhesion

layer adjacent the passivation layers **404a-b** and metal pad **403** and a conduction layer on the adhesion layer opposite the passivation layers **404a-b** and metal pad **403**. More particularly, the adhesion layer may include titanium-tungsten (TiW), and the conduction layer may include copper (Cu), Silver (Ag), gold (Au), Palladium (Pd), and/or alloys thereof. The underbump metallurgy (seed) layer **405** may also include an intermediate layer between adhesion and conduction layers, and the intermediate layer may include titanium (Ti) and/or titanium nitride (TiN).

[0077] A plating stencil (mask) **407** is then formed on the underbump metallurgy (seed) layer **405**, and a hole **408** in the plating stencil **407** exposes portions of the underbump metallurgy (seed) layer **405**. More particularly, the hole **408** exposes an area of the underbump metallurgy (seed) layer **405** that is less than an area of the metal pad **403** exposed by the passivation layers **404a-b** so that portions of the underbump metallurgy (seed) layer **405** exposed by the hole **408** do not extend over the passivation layers **404a-b** as shown in Figure 4A. The plating stencil (mask) **407**, for example, may be a layer of an organic or inorganic photo-imagable material such as photoresist, and the hole may be formed using photolithography. More particularly, the plating stencil (mask) **407** may be formed by spinning or laminating the material on the underbump metallurgy (seed) layer **405**, baking the material, selectively exposing the material to radiation (such as light), and developing the material to form the hole **408**. In addition or in an alternative, the plating stencil (mask) **407** may be formed using electro-deposition.

[0078] A barrier layer **409** may then be selectively formed (such as by plating) on portions of the underbump metallurgy (seed) layer **405** exposed through the hole **408**. The barrier layer **409**, for example, may include nickel, copper, and/or alloys thereof. After plating the barrier layer **409**, a solder bump **411** is plated in the hole **408** on the barrier layer **409**. The solder bump **411** may include an alloy such as a tin-lead (SnPb) solder, or the solder bump **411** may be lead free.

[0079] Once the barrier layer **409** and the solder bump **411** are plated, the plating stencil (mask) **407** can be removed as shown in Figure 4B. As further shown in Figure 4B, portions of the underbump metallurgy (seed) layer **405** not covered by the barrier layer **409** and/or solder bump **411** may be removed, and the solder bump **411** may be subjected to reflow to provide a solder ball. For example, exposed portions of the

underbump metallurgy (seed) layer **405** may be removed using an etch chemistry that removes the underbump metallurgy (seed) layer selectively with respect to the barrier layer **409**. Accordingly, the patterned underbump metallurgy (seed) layer **405** may be undercut with respect to the barrier layer **409**.

[0080] More particularly, the underbump metallurgy (seed) layer **405** may be removed using an etch chemistry that removes at least a remaining portion of the underbump metallurgy (seed) layer **405** selectively with respect to the metal pad **403** and/or the organic passivation layer **404b**. For example, peroxide (H_2O_2) may be used to remove a TiW adhesion layer of the underbump metallurgy (seed) layer **405** selectively with respect to an aluminum (or other) pad metal **403**. Reflow of the solder bump **411** may be performed after removing a solder wettable conduction layer (such as copper) of the underbump metallurgy (seed) layer **405** but before removing a solder non-wettable adhesion layer (such as TiW) of the underbump metallurgy (seed) layer **405** so that the solder bump **411** does not spread across exposed portions of the metal pad **403**.

[0081] In an alternative, the metal pad **403** may include a solder non-wettable metal (such as aluminum) on a surface thereof so that reflow of the solder bump **411** may be performed after removing the underbump metallurgy (seed) layer **405** without the solder bump **411** spreading across exposed portions of the metal pad **403**. In another alternative, reflow of the solder bump **411** may be performed without flux to maintain an oxide thereon so that the solder bump **411** does not spread across an exposed wettable surface such as a conduction layer of the underbump metallurgy (seed) layer **405** (before removing exposed portions of the underbump metallurgy layer) or the metal pad **403** (after removing exposed portions of the underbump metallurgy layer). Reflow of the solder bump **411** may be performed above a liquidus temperature of the solder bump **411**, or reflow of the solder bump **411** may not exceed a liquidus temperature of the solder bump **411**. In yet another alternative, the solder bump **411** may not be subjected to reflow.

[0082] As shown in Figure 4B, edge portions of the metal pad **403** may be covered by the passivation layers **404a-b**, and central portions of the metal pad **403** may be covered by the remaining portions of the underbump metallurgy (seed) layer **405**, the barrier layer **409**, and the solder bump **411**. Portions of the metal pad **403** between the

passivation layers **404a-b** and the patterned underbump metallurgy layer **405**, however, may remain exposed after forming the barrier layer **409** and the solder bump **411**, and/or after reflowing the solder bump **411**.

[0083] As further shown in Figures 4A and 4B, the metal pad **403** may be considered to be "below" or "beneath" a surface of the substrate because portions of the metal pad **403** may be covered by the passivation layers **404a** and/or **404b** before forming the underbump metallurgy (seed) layer **405**, the barrier layer **409**, and the solder bump **411**. Stated in other words, the passivation layers **404a** and/or **404b** may be considered as a part of the substrate. According to some embodiments shown in Figure 4B, an entirety of the patterned underbump metallurgy (seed) layer **405** and an entirety of the barrier layer **409** may be conformal with respect to the metal pad **403** such that neither extends beyond an edge of the metal pad or onto the passivation layer. According to other embodiments shown in the cross-sectional views of Figures 4B and 4C, portions of the patterned underbump metallurgy (seed) layer **405** and the barrier layer **409** (shown in the cross-sectional view of Figure 4C) may extend to and/or overlap the passivation layers **404a** and/or **404b** while other portions of the patterned underbump metallurgy (seed) layer and barrier layer (shown in the cross-sectional view of Figure 4B) are set back from the passivation layer(s).

[0084] If the exposed portion of the metal pad **403** is square and each of the patterned underbump metallurgy layer **405**, the barrier layer **409**, and the solder bump **411** are maintained within the exposed portion of the metal pad **403**, the solder bump **411** may have a circular footprint as shown, for example, in Figure 5. In other embodiments, Figure 1C may be a cross-sectional view taken at an angle with respect to the cross-section of Figure 1B. As shown in Figure 1C, portions of the patterned underbump metallurgy (seed) layer **405**, the barrier layer **409**, and the solder bump **411** may extend beyond the metal pad **403** onto the passivation layers **404a** and **404b**. If the metal pad **403** is square when viewed from the top, and the cross-sections of Figures 1B and 1C are at an angle of 45 degrees with respect to each other, the solder bump **411** may have a circular footprint as shown, for example, in Figure 6. If the metal pad **403** is square when viewed from the top, and the cross-sections of Figures 1B and 1C are at an angle of 90

degrees with respect to each other, the solder bump **411** may have an oval footprint as shown, for example in Figure 7.

[0085] In alternatives, the underbump metallurgy (seed) layer **405** may be patterned using the barrier layer **409** without the solder bump **411**. The barrier layer **409**, for example, may be selectively formed (such as by plating) on the underbump metallurgy (seed) layer **405**, and portions of the underbump metallurgy (seed) layer **405** exposed by the barrier layer **409** may be selectively removed. After exposed portions of the underbump metallurgy (seed) layer **405** have been selectively removed, a solder bump or other interconnection structure may be provided on the barrier layer **409**. For example, a solid preformed solder structure may be placed on the barrier layer **409**, and/or the barrier layer **409** may be bonded with a solder structure on a second substrate.

[0086] In addition or in an alternative, a conductive post (such as a copper post) may be provided on the barrier layer **409** instead of the solder bump **411** or between the barrier layer **409** and the solder bump **411**. A conductive post may be selectively formed on the barrier layer **409** (such as by plating using plating stencil **407**) before selectively removing exposed portions of the underbump metallurgy (seed) layer **405**, and/or a conductive post may be placed on the barrier layer **409** after selectively removing exposed portions of the underbump metallurgy (seed) layer **405**. A solder structure may then be formed on the conductive post, and/or a solid preformed solder structure may be placed on the conductive post. In an alternative, the conducive post may be bonded with a solder structure on a second substrate.

[0087] As shown in the top view of Figure 5, edge portions of a metal pad **503** may be covered by a passivation layer **504**, such as a passivation layer including one or more organic and/or inorganic dielectric layers. Moreover, a solder bump **511** may be formed on a central portion of the metal pad **503** according to embodiments of the present invention such that portions of the metal pad **503** are exposed between the passivation layer **504** and the solder bump **511**. As discussed above with respect to Figures 1A-B, 2A-B, 3A-B, and 4A-B, an underbump metallurgy layer, a barrier layer, and/or a conductive post may be provided between the solder bump **511** and the metal pad **503**, but the underbump metallurgy layer, the barrier layer, and/or the conductive post are not visible in the top view of Figure 5. The structure of Figure 5, for example, may be

provided as discussed above with respect to Figures 1A-B, 2A-B, 3A-B, and/or 4A-B. As discussed above, a conductive post (such as a copper post) may be provided in addition to or instead of the solder bump **711**.

[0088] As shown in the top view of Figure 6, edge portions of a metal pad **603** may be covered by a passivation layer **604**, such as a passivation layer including one or more organic and/or inorganic dielectric layers. Moreover, a round solder bump **611** may be formed on a central portion of the metal pad **603** according to embodiments of the present invention such that portions of the metal pad **603** are exposed between the passivation layer **604** and the solder bump **611**. As discussed above with respect to Figures 1A-B, 2A-B, 3A-B, and 4A-B, an underbump metallurgy layer, a barrier layer, and/or a conductive post may be provided between the solder bump **611** and the metal pad **603**, but the underbump metallurgy layer, the barrier layer, and/or the conductive post are not visible in the top view of Figure 6. In the structure of Figure 6, portions of the solder bump, the underbump metallurgy layer, the barrier layer, and/or the conductive post may extend to and/or overlap the passivation layer **604** while other portions of the solder bump **611**, the underbump metallurgy layer, the barrier layer, and/or the conductive post are set back from the passivation layer **604**. The structure of Figure 6, for example, may be provided as discussed above with respect to Figures 1A-B, 2A-B, 3A-B, and 4A-B. As discussed above, a conductive post (such as a copper post) may be provided in addition to or instead of the solder bump **711**.

[0089] As shown in the top view of Figure 7, edge portions of a metal pad **703** may be covered by a passivation layer **704**, such as a passivation layer including one or more organic and/or inorganic dielectric layers. Moreover, an oval solder bump **711** may be formed on a central portion of the metal pad **703** according to embodiments of the present invention such that portions of the metal pad **703** are exposed between the passivation layer **704** and the solder bump **711**. As discussed above, an underbump metallurgy layer, a barrier layer, and/or a conductive post may be provided between the solder bump **711** and the metal pad **703**, but the underbump metallurgy layer, the barrier layer, and/or the conductive post are not visible in the top view of Figure 7. In the structure of Figure 7, portions of the solder bump, the underbump metallurgy layer, the barrier layer, and/or the conductive post may extend to and/or overlap the passivation

layer **704** while other portions of the solder bump **711**, the underbump metallurgy layer, the barrier layer, and/or the conductive post are set back from the passivation layer **704**. More particularly, portions of the patterned underbump metallurgy (seed) layer, the barrier layer, and/or the conductive post may extend to and/or overlap the passivation layer **704** while other portions of the patterned underbump metallurgy (seed) layer, barrier layer, and/or conductive post are set back from the passivation layer. The structure of Figure 7, for example, may be provided as discussed above with respect to Figures 1A-B, 2A-B, 3A-B, and 4A-B. As discussed above, a conductive post (such as a copper post) may be provided in addition to or instead of the solder bump **711**.

[0090] As shown in the cross-sectional view of Figure 8, solder bumps **811** provided according to embodiments of the present invention may allow a closer placement of metal pads **803** and solder bumps **811** to provide a tighter pitch on integrated circuit device **821**. More particularly, the solder bumps **811** can be provided on central portions of the metal pads **803** with portions of the metal pads **803** exposed adjacent to the solder bumps **811**. Accordingly, shorting of adjacent solder bumps **811** can be reduced. Moreover, an additional passivation layer is not required to confine the solder within the central portion of the metal pad **803**.

[0091] As discussed above, the metal pads **803** are provided on substrate **801**, and a passivation layer **804** may extend onto edge portions of the metal pads **803**. The underbump metallurgy (seed) layer **805**, the barrier layer **809**, and the solder bump **811** may be formed as discussed above with regard to Figures 1A-B, 2A-B, 3A-B, and/or 4A-B. In some embodiments, edge portions of the metal pads **803** may be free of the passivation layer **804** as discussed above with respect to Figures 1A-B.

[0092] Moreover, the metal pads **803** may be provided in staggered rows to further increase a pitch or density of the solder bumps **811** and/or to provide larger solder bumps **811** on the substrate **801**. For example, metal pads **803** may be arranged in a checker board pattern as illustrated in the top view of Figure 9. A likelihood of shorts between solder bumps **811** may be reduced if one or more solder bumps **811** extends beyond the exposed portion of the respective metal pad **803** over the passivation layer **804**.

[0093] Figure 10A is a plan view of an electronic substrate including a plurality of interconnection structures on a substrate according to additional embodiments of the present invention, and Figure 10B is a cross-sectional view taken along section line I-I' of Figure 10A. In particular, portions of a plurality of metal pads **1003a-c** may be exposed through a passivation layer **1004** on substrate **1001**. As shown, edge portions of the metal pads **1003a-c** may be covered by the passivation layer **1004**. In other embodiments, edge portions of the metal pads **1003a-c** may be free of the passivation layer **1004**. Moreover, patterned seed layers **1005a-c** and barrier layers **1009a-c** may be provided between respective solder bumps **1011a-c** and metal pads **1003a-c**. Moreover, the passivation layer **1004** may include one or more orgnanic and/or inorganic dielectric layers.

[0094] The structures of Figures 10A-B may be formed as discussed above with regard to Figures 1A-C, 2A-C, 3A-B, and/or 4A-C. For example, a continuous underbump metallurgy (seed) layer may be formed on the passivation layer **1004** and metal pads **1003a-c** to provide an electroplating electrode, and a plating stencil may be formed on the continuous underbump metallurgy (seed) layer. The plating stencil, for example, may expose circular areas of the continuous underbump metallurgy (seed) layer at least portions of which are on respective metal pads **1003a-c**. The barrier layers **1009a-c** can then be selectively formed (such as by plating) on exposed portions of the continuous underbump metallurgy layer. The plating stencil can then be removed, and portions of the continuous underbump metallurgy (seed) layer exposed by the barrier layers **1009a-c** can be removed to provide the patterned underbump metallurgy (seed) layers **1005a-c**.

[0095] The solder bumps **1011a-c** can be formed on the barrier layers, for example, by plating before removing the plating stencil and before removing exposed portions of the underbump metallurgy (seed) layer. In other embodiments, solid preformed solder structures may be placed on the barrier layers **1009a-c**, and/or the barrier layer **1009a-c** may be bonded with solder structures on a second substrate. In still other embodiments, conductive posts (such as copper posts) may be provided on the barrier layers **1009a-c** instead of the solder bumps **1011a-c** or between the barrier layers **1009a-c** and the solder bumps **1011a-c**. Conductive posts may be selectively formed on

the barrier layers **1009a-c** (such as by plating using the plating stencil) before selectively removing exposed portions of the continuous underbump metallurgy (seed) layer, and/or conductive posts may be placed on the barrier layers **1009a-c** after selectively removing exposed portions of the continuous underbump metallurgy (seed) layer. Solder structures may then be formed on the conductive posts, and/or solid preformed solder structures may be placed on the conductive posts. In an alternative, the conducive posts may be bonded with solder structures on a second substrate.

[0096] As shown in Figures 10A and 10B, relative placements of barrier layers **1009a-c** solder bumps **1011a-c** on respective metal pads **1003a-c** may vary. For example, the barrier layer **1009b** and solder bump **1011b** may be substantially centered with respect to metal pad **1003b**, while the barrier layers **1009a** and **1009c** and the solder bumps **1011a** and **1001c** may be offset in different directions relative to the metal pads **1003a** and **1003b**. Accordingly, barrier layers, solder bumps, and/or other interconnections structures may be redistributed with respect to metal pads without requiring redistribution lines and/or patterning thereof.

[0097] Embodiments of the present invention may thus allow forming a solder bump on a metal input/output pad without completely sealing the metal input/output pad with the patterned underbump metallurgy (seed) layer, the barrier layer, and/or passivation. The patterned underbump metallurgy (seed) layer and the barrier layer may thus be contained within exposed portions of the metal input/output pad and/or portions of the underbump metallurgy (seed) layer and the barrier layer may extend beyond exposed portions of the metal input/output pad. For example, portions of an insulating passivation layer may extend between the metal input/output pad and edge portions of the underbump metallurgy (seed) layer and barrier layer, while other portions of the insulating passivation layer may be separated from the underbump metallurgy (seed) layer and the barrier layer by exposed portions of the metal input/output pad therebetween. Accordingly, the resulting solder bump may be smaller than an exposed portion of the corresponding metal input/output pad in one or more dimensions without requiring another passivation step. Accordingly, solder bumps can be formed on more closely spaced pads without requiring an additional passivation layer and with reduced risk of electrical shorts therebetween.

[0098] While the present invention has been particularly shown and described with reference to embodiments thereof, it will be understood by those skilled in the art that various changes in form and details may be made therein without departing from the spirit and scope of the invention as defined by the appended claims and their equivalents.

That Which Is Claimed Is:

1. A method of forming an electronic structure, the method comprising:

providing a substrate having a metal pad thereon and an insulating layer surrounding the metal pad;

forming a conductive barrier layer on a first portion of the metal pad, wherein a second exposed portion of the metal pad is free of the conductive barrier layer and free of the insulating layer; and

providing an interconnection structure on the conductive barrier layer, wherein the conductive barrier layer is between the interconnection structure and the metal pad and wherein the interconnection structure and the conductive barrier layer include different materials.

2. A method of forming an electronic structure according to Claim 1 wherein forming the conductive barrier layer comprises,

forming a conductive seed layer on the metal pad and on the insulating layer,

selectively forming the conductive barrier layer on a portion of the conductive seed layer on the first portion of the metal pad so that a second portion of the seed layer on the second portion of the metal pad is free of the conductive barrier layer, and

after selectively forming the conductive barrier layer, removing the second portion of the seed layer from the second portion of the metal pad.

3. A method according to Claim 2 wherein removing the second portion of the seed layer comprises etching the second portion of the seed layer using an etch chemistry that etches at least a portion of the conductive seed layer preferentially with respect to the conductive barrier layer and the metal pad.

4. A method according to Claim 1 wherein the exposed second portion of the metal pad surrounds the conductive barrier layer.

5. A method according to Claim 1 wherein a portion of the conductive barrier layer extends beyond an edge of the metal pad.

6. A method according to Claim 1 wherein the insulating layer extends on an edge portion of the metal pad opposite the substrate so that the second portion of the metal pad is exposed between the conductive barrier layer and the insulating layer.

7. A method according to Claim 1 wherein a portion of the conductive barrier layer extends on a portion of the insulating layer.

8. A method according to Claim 1 wherein a center of the conductive barrier layer is substantially aligned with respect to a center of the metal pad.

9. A method according to Claim 1 wherein a center of the conductive barrier layer is substantially offset with respect to a center of the metal pad.

10. A method according to Claim 1 further comprising:

providing a second metal pad on the substrate, wherein the first and second metal pads are spaced apart; and

forming a second conductive barrier layer on a portion of the second metal pad, wherein an alignment of the first conductive barrier layer relative to the first metal pad is different than an alignment of the second conductive barrier layer relative to the second metal pad.

11. A method according to Claim 10 wherein the first conductive barrier layer is substantially aligned relative to the first metal pad and wherein the second conductive barrier layer is substantially offset relative to the second metal pad.

12. A method according to Claim 10 wherein the first conductive barrier layer is substantially offset in a first direction relative to the first metal pad and wherein the

second conductive barrier layer is substantially offset in a second direction relative to the second metal pad and wherein the first and second directions are different.

13. A method according to Claim 1 wherein the interconnection structure includes a solder bump and/or a copper post.

14. A method according to Claim 1 wherein the metal pad includes aluminum, copper, gold, and/or alloys thereof, wherein the conductive barrier layer includes nickel, copper, and/or alloys thereof, and wherein the interconnection structure includes solder and/or copper.

15. A method according to Claim 1 wherein the metal pad includes aluminum and the conductive barrier layer includes nickel.

16. A method according to Claim 1 wherein at least a portion of the metal pad is on a portion of the insulating layer so that a surface of the metal pad opposite the substrate is free of the insulating layer.

17. An electronic structure comprising:

a substrate having a metal pad thereon and an insulating layer surrounding the metal pad;

a conductive barrier layer on a first portion of the metal pad, wherein a second exposed portion of the metal pad is free of the conductive barrier layer and free of the insulating layer; and

an interconnection structure on the conductive barrier layer, wherein the conductive barrier layer is between the interconnection structure and the metal pad and wherein the interconnection structure and the conductive barrier layer include different materials.

18. An electronic structure according to Claim 17 wherein the exposed second portion of the metal pad surrounds the conductive barrier layer.

19. An electronic structure according to Claim 17 wherein a portion of the conductive barrier layer extends beyond an edge of the metal pad.

20. An electronic structure according to Claim 17 wherein the insulating layer extends on an edge portion of the metal pad opposite the substrate so that the second portion of the metal pad is exposed between the conductive barrier layer and the insulating layer.

21. An electronic structure according to Claim 17 wherein a portion of the conductive barrier layer extends on a portion of the insulating layer.

22. An electronic structure according to Claim 17 wherein a center of the conductive barrier layer is substantially aligned with respect to a center of the metal pad.

23. An electronic structure according to Claim 17 wherein a center of the conductive barrier layer is substantially offset with respect to a center of the metal pad.

24. An electronic structure according to Claim 17 further comprising:

a second metal pad on the substrate, wherein the first and second metal pads are spaced apart; and

a second conductive barrier layer on a portion of the second metal pad, wherein an alignment of the first conductive barrier layer relative to the first metal pad is different than an alignment of the second conductive barrier layer relative to the second metal pad.

25. An electronic structure according to Claim 24 wherein the first conductive barrier layer is substantially aligned relative to the first metal pad and wherein the second conductive barrier layer is substantially offset relative to the second metal pad.

26. An electronic structure according to Claim 24 wherein the first conductive barrier layer is substantially offset in a first direction relative to the first metal pad and

wherein the second conductive barrier layer is substantially offset in a second direction relative to the second metal pad and wherein the first and second directions are different.

27. An electronic structure according to Claim 17 wherein the interconnection structure includes a solder bump and/or a copper post.

28. An electronic structure according to Claim 17 further comprising:

a seed layer between the conductive barrier layer and the metal pad, wherein the seed layer and the conductive barrier layer include different materials.

29. An electronic structure according to Claim 17 wherein the metal pad includes aluminum, copper, gold, and/or alloys thereof, wherein the conductive barrier layer includes nickel, copper, and/or alloys thereof, and wherein the interconnection structure includes solder and/or copper.

30. An electronic structure according to Claim 17 wherein the metal pad includes aluminum and the conductive barrier layer includes nickel.

31. An electronic structure according to Claim 17 wherein at least a portion of the metal pad is on a portion of the insulating layer so that a surface of the metal pad opposite the substrate is free of the insulating layer.

32. A method of forming an electronic structure, the method comprising:

providing a substrate having a metal pad thereon;

forming an underbump metallurgy layer on a surface of the metal pad wherein the metal pad is between the underbump metallurgy layer and the substrate;

forming a barrier layer on the underbump metallurgy layer wherein the underbump metallurgy layer is between the barrier layer and the metal pad, wherein an entirety of the barrier layer is conformal with respect to the surface of the metal pad, and wherein the barrier layer and the underbump metallurgy layers comprise different materials; and

forming a solder bump on the barrier layer wherein the barrier layer is between the solder bump and the underbump metallurgy layer, and wherein the barrier layer and the solder bump comprise different materials.

33. A method of forming an electronic structure, the method comprising:

providing a substrate having a metal pad thereon;

forming an underbump metallurgy layer on a surface of the metal pad wherein the metal pad is between the underbump metallurgy layer and the substrate;

forming a barrier layer on the underbump metallurgy layer wherein the underbump metallurgy layer is between the barrier layer and the metal pad, and wherein the barrier layer and the underbump metallurgy layer comprise different materials; and

forming a solder bump on the barrier layer wherein the barrier layer is between the solder bump and the underbump metallurgy layer, wherein the barrier layer and the solder bump comprise different materials, and wherein a portion of the metal pad is exposed adjacent to the underbump metallurgy layer, the barrier layer, and the solder bump.

34. An electronic structure comprising:

a substrate having a metal pad thereon;

an underbump metallurgy layer on a surface of the metal pad wherein the metal pad is between the underbump metallurgy layer and the substrate;

a barrier layer on the underbump metallurgy layer wherein the underbump metallurgy layer is between the barrier layer and the metal pad, wherein an entirety of the barrier layer is conformal with respect to the surface of the metal pad, and wherein the barrier layer and the underbump metallurgy layers comprise different materials; and

a solder bump on the barrier layer wherein the barrier layer is between the solder bump and the underbump metallurgy layer, and wherein the barrier layer and the solder bump comprise different materials.

35. An electronic structure comprising:

a substrate having a metal pad thereon;

an underbump metallurgy layer on a surface of the metal pad wherein the metal pad is between the underbump metallurgy layer and the substrate;

a barrier layer on the underbump metallurgy layer wherein the underbump metallurgy layer is between the barrier layer and the metal pad, and wherein the barrier layer and the underbump metallurgy layer comprise different materials; and

a solder bump on the barrier layer wherein the barrier layer is between the solder bump and the underbump metallurgy layer, wherein the barrier layer and the solder bump comprise different materials, and wherein a portion of the metal pad is exposed adjacent to the underbump metallurgy layer, the barrier layer, and the solder bump.