DIGITAL MAGNETIC RECORDING AND REPRODUCING APPARATUS

BACKGROUND OF THE INVENTION

Field of the Invention

The invention relates to digital magnetic recording and reproducing circuit and apparatus for recording and reproducing digital information to and from a recording medium such as a magnetic disk or the like and, more particularly, relates to a signal processor for performing a PR equalization and a Viterbi decoding and an apparatus using such a processor.

Description of the Related Art

A demand for a high density and high speed recording to a magnetic disk apparatus is more and more increasing. A signal processing technique of a recording and reproducing system has also coped with the high density and high speed recording. As a recording code, a coding rate R is raised for realization of the high speed and R = 8/9 is often used at present. Further, in recent years, various higher rate 16/17 codes have been proposed and are becoming a main stream of the recording code. In order to cope with the deterioration of an S/N ratio due to an intercode interference in association with the high density recording, the Partial Response (hereinafter, abbreviated to "PR") equalizing system, for detecting a signal sequence that is closest to a reproduction signal by using an

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already-known interference on a reproducing channel, has been put into practical use. Particularly, a PR4ML (Partial Response Class 4 with Maximum Likelihood Detection) system has already been installed as an LSI to a magnetic disk product.

Fig. 1 shows a construction of a digital magnetic recording and reproducing apparatus which has hitherto been used. A case of using the EPR4 (Extended PR4) system as a PR equalizer will now be described. In the diagram, on the recording side, digital information A is error-correction-encoded by an ECC (error correction code) encoder 10 by using a Reed-Solomon code or the like. The Reed-Solomon code is often used in a magnetic recording and reproducing apparatus which requires high reliability because byte errors can be corrected. The above-mentioned ECC encoded sequence is modulation code-encoded by a modulation code encoder 11. By performing a run length limitation or the like to the modulation code-encoded sequence, the sequence is converted into a format according to the magnetic reproducing characteristics. The 8/9 code and, further, recently, the 16/17 code are most frequently used. The modulation code encoded sequence is further converted into an NRZI (Non Return to Zero Inverted) format by a precoder 12. After that, the converted sequence passes through an amplifier 13 and a recording head 14 and is magnetically recorded to a recording medium 15 such as a magnetic disk or the like.

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On the other hand, on the reproducing side, the information recorded on the magnetic recording medium 15 is reproduced as an electric analog signal by a reproducing head 16 and an amplifier 17 and is controlled so as to have a predetermined amplitude by a variable gain amplifier 18, thereby preventing an overflow of an input amplitude to an A/D (Analog to Digital) converter 19. The A/D converter 19 converts the analog signal to a digital signal and all of the subsequent reproducing processes are digitally processed. The digital signal is sampled every bit intervals at proper timings and inputted to a PR equalizer 20. In the PR equalization (EPR4 equalization here), the signal is EPR4 equalized to a channel having transmission characteristics of (1 + D - D^2 - D^3) by using an input sample sequence. D denotes a channel memory and ^ indicates a power arithmetic operation. The EPR4 channel is expressed by a state transition diagram of eight states as shown in Fig. 24. In the diagram, S0, S1, ..., and S7 denote channel states 000, 001, ..., and 111, respectively. In accordance with a value (0, 1; expressed by -, + in the diagram) of an input signal to a certain state, equalization signals corresponding to the upper path and lower path are outputted and they are transferred to the next channel states, respectively. In the EPR4 channel, the equalization output has five values (2, 1, 0, -1, -2).

The EPR4 equalized sequence is maximum-likelihood-decoded by a Viterbi detector 21. The above process is for presuming (maximum likelihood sequence

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presumption) a career of the path transitted at a most likelihood probability by using the state transition diagram shown in Fig. 24. A decoded result (0, 1) obtained by the maximum likelihood sequence presumption is modulation code decoded by a modulation code decoder 22 and is inversely converted to an input sequence of the modulation code encoder on the reproducing side. The recording-decoded sequence is byte-error-corrected by a Reed-Solomon decoding or the like by an ECC (error correction code) decoder 23 and, after that, reproduction information A' is reproduced.

Fig. 2 shows a construction of the Viterbi detector 21. A bold signal line and a thin signal line denote a bus of a plurality of bits and a bus of one bit (hereinafter, they are similarly expressed in the following other diagrams), respectively. In the diagram, as for a sequence yk which was EPR4 equalized at time k, a probability at which EPR4 equalization output candidates (2, 1, 0, -1, -2) were outputted is calculated as a branch metric by a branch metric calculator 41. The branch metric is calculated as a square distance between the yk and the EPR4 equalization output candidate. The branch metrics corresponding to 2, 1, 0, -1, and -2 are expressed by BM(2), BM(1), BM(0), BM(-1), and BM(-2), respectively.

When the branch metrics are calculated, adding, comparing, and selecting processes are executed by an ACS (Add, ComPare, Select) circuit 42. Fig. 3 shows a detailed circuit construction. As shown in the diagram, in the ACS

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circuit, the branch metric BM and a state likelihood S (accumulated value of the branch metrics) are added every state by an adder 100 in accordance with the EPR4 state transition diagram (Fig. 24). The likelihood having a larger value and the corresponding path are outputted from a comparator 101 as new state likelihoods S0, ..., and S7 and survivor path information SP0, ..., and SP7, respectively. In the state transition diagram (Fig. 24), each of the survivor path information SP0, ..., and SP7 is a value which is expressed by one bit (0, 1) to identify the upper path and the lower path. The state likelihoods S0, ..., and S7 are respectively stored in delay elements T 102, thereby preparing for the next ACS arithmetic operating process. Although not shown in order to avoid complication in the diagram, it is assumed that outputs of the delay elements 102 are feedback connected to inputs of the adders 100, respectively.

The survivor paths SP0, ..., and SP7 are inputted to data selectors 103 and corresponding binary data d0, ..., and d7 are outputted from the survivor path information to a path memory circuit 43. The path memory circuit 43 stores the binary data d0, ..., and d7 for a sufficiently long period of time (path memory length) and generates the data which is preceding by a time of the path memory length as a Viterbi decoded result by a trace back process (ordinarily, well-known register exchanging process).

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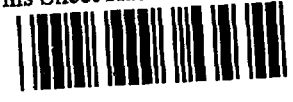
When paying an attention to the encoding, a trellis code is highlighted and examined as a system which enables a high density recording over the EPR4ML. The trellis code is one of recording code and is a scheme for encoding information after completion of the ECC encoding by a certain rule and combining the encoded information with the PR channel, thereby enlarging an MSED (Minimum Squared Euclidean Distance) between signals. The trellis code based on the PR4 channel (hereinafter, referred to as a PR4 trellis code) has been examined.

There is an MSN (Matched Spectral Null) code as a PR4 trellis code applied to the magnetic recording. The MSN code intends to obtain a larger MSED by matching the frequency characteristics of the code to those of the magnetic channel. Its principle has been described in detail in the literature, "Matched Spectral-Null Codes for Partial-Response Channels", IEEE Transactions on Information Theory, Vol. 37, No. 3, pp. 818 - 855, May 1991. According to the above method, by performing the encoding while using the PR4 channel as a base, MSED = 4 is realized and an S/N gain of 3 dB is obtained for a non-encoded PR4ML.

The MSN code can be also applied to the EPR4 channel. Actually, a case that MSED = 12 can be realized is also described in the above literature. However, only a low coding rate of 1/2 has been found out in this case.

At present, an LSI using the MSN code in which a coding rate is equal to 8/10, 6 state has been manufactured

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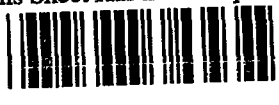


on an experimental basis as a PR4 trellis. Characteristics of such an LSI have been described in the literature, "Design and Performance of a VLSI 120 Mb/s Trellis-Coded Partial Response Channels", IEEE, Proceedings of 1994, The Magnetic Recording Conference.

Further in recent years, a trellis coding scheme by permutation has been proposed as a method of improving the MSN code and, further, realizing a high rate. According to such a system, a channel state corresponding to a code word final bit and a state corresponding to the next code word head bit are permutation connected while keeping only the channel bit. The trellis coding scheme has been described in detail in the literature, "Improved Trellis-Coding for Partial-Response Channels", IEEE, Proceedings of 1994, The Magnetic Recording Conference, the literature, "Finite Truncation Depth Trellis Codes for the Dicode Channel", IEEE, Transactions on Magnetics, Vol. 31, No. 6, pp. 3027 - 3029, November 1995, and U.S.P. No. 5497384, "Permuted Trellis Codes for Input Restricted Partial Response Channels", respectively. According to the trellis coding scheme by the permutation, a degree of code allocation freedom is raised and a high rate recording code that is equivalent to 8/9 can be relatively easily realized.

Because of the rapid progress to the high density recording in association with a demand to a large capacity storage, it is impossible to satisfy a requirement for the super high density recording by only the EPR4ML. In

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addition, the PR4 trellis cannot be applied to a high recording linear density region and there is also a limitation of the MSED. Although an enlargement of the MSED can be expected by applying the trellis code to the EPR4 channel, it is not only difficult to raise a coding rate, but also the number of channel states and its circuit scale may become very large.

SUMMARY OF THE INVENTION

In consideration of the above problems, it is an object of the invention to provide a digital magnetic recording and reproducing circuit with simple structure using a signal processing method which can achieve higher density recording than the conventional one, and to provide a digital magnetic recording and reproducing apparatus using such a circuit.

According to the invention, in a reproducing apparatus, an apparatus for detecting an erasure bit in the decoding process is provided for a Viterbi detector, an apparatus for detecting an erasure byte is provided for a modulation code decoder, and an apparatus for performing an erasure byte error correction is provided for an ECC decoder.

Or, in a recording apparatus, an apparatus for performing a first ECC encoding and a second ECC encoding is provided, in a reproducing apparatus, an apparatus for detecting an erasure bit is provided for a Viterbi

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detector, and an apparatus for detecting an erasure error by performing a second ECC decoding and an apparatus for performing a first ECC decoding by using the erasure error are provided for a decoder.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a constructional diagram of a digital magnetic recording and reproducing apparatus according to the conventional technique;

Fig. 2 is a constructional diagram of a Viterbi detector according to the conventional technique;

Fig. 3 is a constructional diagram of an ACS circuit according to the conventional technique;

Fig. 4 is a constructional diagram of an example of a digital magnetic recording and reproducing apparatus according to the present invention;

Fig. 5 is a constructional diagram of an example of a Viterbi detector in Fig. 4;

Fig. 6 is a constructional diagram of an ACS circuit in Fig. 5;

Fig. 7 is a constructional diagram of a path memory circuit in Fig. 5;

Fig. 8 is a constructional diagram of an erasure error detector in Fig. 5;

Fig. 9 is a constructional diagram of another example of the Viterbi detector in Fig. 4;

Fig. 10 is a constructional diagram of an example of an ACS circuit in Fig. 9;

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Fig. 11 shows a construction diagram of a path memory circuit in Fig. 9;

Fig. 12 shows a construction diagram of an erasure error detector in Fig. 9;

Fig. 13 is a constructional diagram of another example of the ACS circuit in Fig. 9;

Fig. 14 is a constructional diagram of a path discriminator in Fig. 13;

Fig. 15 is a constructional diagram of a path memory circuit in Fig. 13;

Fig. 16 is a constructional diagram of another example of a digital magnetic recording and reproducing apparatus according to the present invention;

Figs. 17A and 17B are diagrams for explaining an encoding processes according to the invention;

Fig. 18 is a constructional diagram of an example of a Viterbi detector in Fig. 16;

Fig. 19 is a constructional diagram of a second ECC decoder in Fig. 18;

Fig. 20 is a constructional diagram of another example of the Viterbi detector in Fig. 16;

Fig. 21 is a constructional diagram of an example of a second ECC decoder in Fig. 20;

Fig. 22 is a constructional diagram of another example of the second ECC decoder in Fig. 20;

Figs. 23A and 23B are diagrams for explaining a searching method of a best sequence and a second sequence by the Viterbi detector of the present invention; and

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Fig. 24 is a trellis diagram showing a state transition of a signal sequence.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

(1) First embodiment

Embodiments of the present invention will now be described hereinbelow with reference to the drawings. Fig. 4 is a diagram showing the first embodiment in the invention. In the diagram, a construction and functions of the ECC encoder 10, modulation code encoder 11, precoder 12, amplifier 13, recording head 14, magnetic recording medium 15, reproducing head 16, amplifier 17, variable gain amplifier 18, A/D converter 19, and PR equalizer 20 are the same as those of the conventional apparatus (refer to Fig. 1).

An apparatus for detecting an erasure bit, an apparatus for detecting an erasure byte, and an apparatus for correcting an erasure byte are respectively added for a Viterbi detector 24, a modulation code decoder 25, and an ECC decoder 26 according to the invention. In the embodiment, a bit or byte, which is determined such that a possibility of the occurrence of a decoding error is high, is called an erasure bit or erasure byte. Fig. 5 shows a construction of the Viterbi detector 24. A construction until branch metrics are calculated by the branch metric calculator is the same as that of the conventional Viterbi detector (Fig. 2).

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When the branch metrics are calculated, adding, comparing, and selecting processes are subsequently executed in an ACS circuit 52.

A likelihood in each state is calculated in the ACS circuit. If the signal is not influenced by noises or the like, only a value of one state likelihood is high and values of the other state likelihoods approach 0 as close as possible. On the contrary, when the signal is strongly influenced by noises or the like, a difference between the state likelihood having the highest value and the other state likelihood is small.

In the embodiment, when the absolute value of the difference between the likelihoods to be compared in the ACS circuit is smaller than a certain threshold value, a possibility such that a decoding error due to a reduction in S/N ratio occurs is high and it is determined that the reliability of the selected path for data is low. Such an error is decided as an erasure error.

Fig. 6 shows a construction of the ACS circuit. As shown in the diagram, in the ACS circuit 52, the branch metric and the state likelihood (accumulated value of the branch metrics) are added every state by the adder 100 in accordance with the EPR4 state transition diagram (refer to Fig. 24) and an addition result is inputted to a comparator 111. The comparators 111 output differential values DM0, ..., and DM7 between the two state likelihoods, respectively, and code bits are set to survivor path

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information SP0, ..., and SP7. The differential value denotes a difference between the two input signals in the comparator 111 and, for example, is calculated as DM0 = (BM(0) + S0)) - (BM(-1) + S4) in case of state S0. The differential values are also similarly calculated with respect to DM1, ..., and DM7. Since all of the digital processes are executed by a 2's complement, the code bit can be used to show the survivor path information SP0, ..., and SP7. The state likelihoods S0, ..., and S7 are respectively stored into the corresponding delay elements 102, thereby preparing for the next ACS operating processes. Although not shown, outputs of the delay elements 102 are respectively feedback connected to inputs of the adders 100.

In a threshold decision circuit 112, the absolute value |DMi| of the differential value DMi and the value of the threshold value R are compared on the basis of the foregoing theory, thereby detecting an erasure error. As a threshold R, the value of the half of the maximum likelihood in the ideal case, namely, in case of no error, specifically speaking, the value of (MSED of the PR channel)/4 is used. The threshold decision circuit 112 outputs ai = 0 when |DMi| > R and outputs ai = 1 in the other cases. ai functions as a control signal.

On the other hand, a data selector 113 receives the survivor path information SPi and control signal ai and outputs corresponding data d0', ..., and d7' from the survivor path information SPi to a path memory circuit 53.

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Each of the data d0', ..., and d7' is set to any one of three values of 1, 0, and erasure X (= 0.5). X denotes an erasure bit and has an intermediate value between 1 and 0, namely, 0.5. ai (i = 0, ..., 7) denotes the control signal to decide which one of 1, 0, and X an output di' of the data selector has. The data selector 113 outputs di' = X irrespective of the value of SPi when ai = 1 and outputs binary data corresponding to SPi when ai = 0.

Fig. 7 shows a constructional conceptual diagram of the path memory circuit 53. In accordance with the inputted survivor path information SP0, ..., and SP7, the path memory circuit 53 selects path memory registers 200 ((reg0.1, reg0.2), ..., (reg7.1, reg7.2)) inputted to a selector 0, ..., and a selector 7 (201) and outputs them to registers reg0, ..., and reg7 (202), respectively. The selector i (i = 0, ..., 7) (201) is a circuit to select an output of the path memory register 200 (regi.1, regi.2) in a state Si. A data career of the path which reaches the state Si has been stored in each of the registers regi.1 and regi.2 and its depth is equal to a path memory length.

On the other hand, the regi (202) also operates as a shift register and its depth is equal to the path memory length (in case of the EPR4ML, usually, about 20 bits). The binary data di' inputted from the data selectors 113 is serially inputted to the regi (202) and the shift-out data is outputted from the opposite side as a Viterbi decoded result. The decoded result has any one of

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1, 0, and X. Each of register outputs R0, ..., and R7 is feedback connected to a signal line shown at the corresponding position and the contents in the path memory registers 200 (regi.1, regi.2) are updated. When the path memory length is sufficiently set to be long, all of the serial outputs of regi (202) are the same (the path after the trace back has been merged). The decoding data, therefore, is derived by using the reg0 (202) in the state S0 here.

For easy understanding of the operation concept here, the path memory registers 200 are shown in the diagram. In the actual circuit construction, however, the above operation can be realized by directly connecting to the selector i (201) by using only the regi (202) without using the path memory registers 200.

Since the data sequence as a Viterbi decoded result obtained by the above processes is based on the maximum likelihood, it is outputted as a best sequence to an erasure error detector 54 in Fig. 5. Fig. 8 shows a construction of the erasure error detector 54. The best sequence is set to any one of 1, 0, and erasure X = 0.5 and those values are discriminated by a threshold decision circuit 81. That is, when the input data d lies within a range of ($0.25 < d \leq 0.75$), it is determined that the erasure X has arrived, so that an erasure bit detection flag flg-ebit is set to 1 and is outputted. In the other cases, the input data is determined to be 1 or 0, so that

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the erasure bit detection flag flg-ebit is set to 0 and is outputted.

By the above processes, the Viterbi detector 24 in Fig. 4 outputs the Viterbi decoded result and the erasure bit detection flag to the modulation code decoder 25. The modulation code decoder 25 inputs the Viterbi decoded result and the erasure bit detection flag and executes a modulation code decoding process. The process is executed on a byte unit basis here. When the erasure bit detection flag is equal to 1, it is known that there is an error in the byte after the decoding, so that the modulation code decoder 25 outputs an erasure byte detection flag flg-ebyte (= 1) together with the modulation code decoded result to the ECC decoder 26. When the erasure bit detection flag is set to 0, it is decided that there is no erasure error in the byte after the modulation code decoding, so that the erasure byte detection flag flg-ebyte (= 0) is outputted together with the decoded result to the ECC decoder 26.

The ECC decoder 26 inputs the modulation code decoded result and the erasure byte detection flag and executes an erasure error correction. Now, assuming that the minimum Hamming distance of the code is equal to d (bytes), in case of the ordinary random error correction, errors of up to t (bytes) can be corrected. It is now assumed that t satisfies the relation of $d = 2t + 1$. The erasure byte detection flag adds information of an error location to the modulation code decoded result, so that an

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error correcting ability is raised. By applying the erasure error correction to the code having the Hamming distance, erasure errors of up to d - 1 = 2t (bytes) can be recovered. This means that if the erasure error can be properly detected, a correcting ability of about two times as high as that of the random error correction can be obtained.

According to the embodiment, therefore, by detecting the decoding error at the time of the maximum likelihood sequence presumption and by correcting the erasure byte that is derived therefrom, decoding error characteristics as a reproducing process can be improved.

(2) Second embodiment

Fig. 9 is a constructional diagram of a Viterbi detector showing the second embodiment. A system construction (Fig. 4) is the same as that of the first embodiment except for the Viterbi detector. Therefore, the construction of the Viterbi detector will now be described.

In Fig. 9, a construction of the branch metric calculator 41 is the same as that of the first embodiment and the branch metrics BM(2), BM(1), BM(0), BM(-1), and BM(-2) derived by the above calculator are inputted to an ACS circuit 62. The ACS circuit 62 and a path memory circuit 63 are characterized in that the best sequence obtained by the maximum likelihood sequence presumption and the 2nd sequence that is optimum subsequently to the best sequence with respect to the likelihood are simultaneously

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outputted. In the embodiment, both of the sequences are compared and a different portion is regarded as a decoding error at the time of the maximum likelihood sequence presumption and is labeled as an erasure bit. In the embodiment, a systematic searching method is proposed as a method of outputting the 2nd sequence and is applied to the ACS arithmetic operation.

According to the systematic searching method, in the ACS arithmetic operation, a state likelihood storage register and a path memory for searching the 2nd sequence are provided at every state and the maximum likelihood and the second maximum likelihood and the corresponding paths are respectively selected by a sorting process and are stored. When the path memories for the best sequence and the 2nd sequence perfectly coincide, in order to avoid the complete coincidence between the best sequence and the 2nd sequence, the third maximum likelihood and the corresponding path memory are stored as a 2nd sequence. A fundamental arithmetic operation of the sorting process is as follows. Namely, as shown in Fig. 23A, for example, as an ACS arithmetic operating process in the state S0, {S0 + BM(0), S0' + BM(0), S4 + BM(-1), S4' + BM(-1)} are sequentially rearranged from the large value and the maximum value and the next large value among them and the corresponding survivor paths are selected. Si and Si' (i = 0, ..., 7) denote state likelihoods which are obtained in correspondence to the best sequence and the 2nd sequence,

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respectively. By the above processes, in addition to the best sequence in the ACS arithmetic operation and the 2nd sequence which is presumed as a sequence having the next high probability can be simultaneously obtained. Similar processes are also executed with respect to the other states S1, ..., and S7.

Fig. 24 shows a presumption example of the best sequence and the 2nd sequence. For simplicity, it is now assumed that the all-0 data sequence was transmitted to the best sequence and the path memory length is equal to 10 bits. In this instance, "0000000000" and "0011000000" have been stored in the path memories for the best sequence and the 2nd sequence, respectively. When a decoding error occurs due to noises or the like for a time interval from time (n - 7) to time (n - 4), the relation between the best sequence and the 2nd sequence is reversed. In the conventional construction, since only the best sequence is processed as a maximum likelihood decoded output, a decoding error occurs at this time point. On the other hand, according to the invention, the 2nd sequence in which the correct decoded result has been stored is provided. If either the best sequence or the 2nd sequence is outputted, the correct decoded result can be obtained. By performing the decoding also using the 2nd sequence as mentioned above, an error event of MSED = 4 in the EPR4ML can be eliminated and the MSED can be equivalently enlarged to 6. This means that 1.8 dB S/N gain is obtained by the EPR4ML using the 2nd sequence.

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The fundamental concept of the ACS arithmetic operation using the best and 2nd sequences by the systematic searching method of the invention has been described above. Fig. 10 shows a construction of the ACS circuit 62 to realize the above processes. That is, in each state, the branch metrics BM(2), BM(1), BM(0), BM(-1), and BM(-2), the state likelihoods S0, ..., and S7 for the best sequence, and the state likelihoods S0', ..., and S7' for the 2nd sequence are added by the adders 100 on the basis of the state transition diagram (Fig. 24). The maximum likelihood (best), the second (2nd) and third (3rd) maximum likelihoods, and corresponding survivor path information (C0-1, C0-2, C0-3), ..., and (C7-1, C7-2, C7-3) are outputted by sorting circuits 120. Although the information regarding the 3rd maximum likelihood is also outputted, the reason why it is outputted is to avoid the perfect coincidence between the best sequence and the 2nd sequence as mentioned above. That is, the path memory circuit 63 compares the path memories corresponding to the best sequence and the 2nd sequence. When the path memories of both of the sequences coincide, the path memory circuit 63 generates "1" to the control signals p0, ..., and p7. Selectors 121 of the ACS circuits select the likelihood for the 3rd sequence in response to the control signals and set it to 2nd likelihoods Si' (i = 0, ..., 7). The state likelihoods Si' of the best and 2nd sequences obtained as mentioned above are stored into the respective

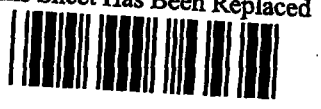
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corresponding delay elements 102, thereby preparing for the next ACS processes. It is assumed that the outputs Si of the delay elements 102 are respectively feedback connected to the inputs of the adders 100. Survivor path information Ci-1, Ci-2, and Ci-3 (i = 0, ..., 7) for the best, 2nd, and 3rd sequences are inputted to the path memory circuit 63. Each of the survivor path information Ci-1, Ci-2, and Ci-3 is expressed by two bits.

Fig. 11 shows a constructional conceptual diagram of the path memory circuit 63. In Fig. 11, the selector 0, ..., and selector 7 (210) are circuits for selecting the path memory registers corresponding to the best, 2nd, and 3rd maximum likelihoods from the path memory registers 200 ((reg0.1, reg0.2, reg0.3, reg0.4), ..., (reg7.1, reg7.2, reg7.3, reg7.4)) in the states S0, ..., and S7, respectively. Data careers (for example, expressed by R0, R0', R4, and R4' in the state S0) of the paths which reach the states Si and Si' corresponding to the amounts of the path memory lengths have been stored in the path memory registers 200 (regi.1, regi.2, regi.3, regi.4) (i = 0, ..., 7), respectively. The path memory registers corresponding to the best, 2nd, and 3rd sequences are selected in the selectors 210 on the basis of the survivor path information Ci-1, Ci-2, and Ci-3 and are outputted to registers ri-1, ri-2, and ri-3 (202), respectively. The registers 202 are also shift registers to which data Di-1, Di-2, and Di-3 for the best, 2nd, and 3rd sequences are serially inputted from

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a data selector 214, respectively. In the state S0, data D0-1' among data D0-1', D0-2', and D0-3' which were shifted out is a decoded result for the best sequence. The data D0-2' and D0-3' are inputted as 2nd and 3rd decoded outputs to a selector 213, respectively. When the path memory length is set to be sufficiently long, the serial outputs in all of the states are the same (the paths after the trace back have been merged). Therefore, the decoded results of the best, 2nd, and 3rd sequences are obtained by using the serial output in the state S0 here.

A comparator 211 discriminates whether the contents of the registers ri-1 and ri-2 (202) coincide or not. The comparator 211 generates a control signal pi = 1 when they coincide and generates the control signal pi = 0 when they differ. The control signal pi is transmitted to the selector 121 in the ACS circuit 62. When pi = 1, the ri-3 output and D0-3' are selected from (the ri-2 output and D0-2') and (the ri-3 output and D0-3') which were supplied to the selector 213. When pi = 0, the ri-2 output and D0-2' are selected. The selected result of D0-2' or D0-3' becomes a final decoded result for the 2nd sequence.

As mentioned above, the path memory registers for the best and 2nd sequences are selected and stored as Ri and Ri' into the registers ri-best and ri-2nd (212), respectively. They are reconnected back to the corresponding signal lines and are stored as updated path memories into the corresponding path memory registers 200 shown, respectively.

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For easily understanding the operation concept here, the path memory registers 200 are shown in the diagram. In the actual circuit construction, however, the above operation can be realized by directly connecting to a selector (210) by using only the registers ri-best and ri-2nd (212) without using the path memory registers 200.

By the above processes, in the Viterbi detector in Fig. 9, the data for the best and 2nd sequences is decoded by the path memory circuit 63 and the decoded results are outputted to an erasure error detector 64. Fig. 12 shows a construction of the erasure error detector 64. After the best and 2nd sequences were converted to parallel data of one byte by an S/P (Serial to Parallel) converter 91, it is inputted to an exclusive OR circuit 92. The exclusive OR of every bit in the parallel data is calculated here. A processing result is compared with the all-0 byte data by a comparator 93. When they differ, it is determined that an erasure error occurred, and the erasure bit detection flag flg-ebit (= 1) is outputted to the modulation code decoder 25. When they coincide, flg-ebit (= 0) is outputted to the modulation code decoder 25.

The modulation code decoder 25 receives the Viterbi decoded result and the erasure bit detection flag and executes a modulation code decoding process. The ECC decoder 26 receives the modulation code decoded result and the erasure byte detection flag and executes an erasure error correction. The modulation code decoder 25 and ECC

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decoder 26 operate in a manner similar to the embodiment 1.

(3) Third embodiment

The third embodiment will now be described with reference to Fig. 9. A fundamental idea of the embodiment is the same as that of the second embodiment and uses the system using both of the best and 2nd sequences. A method of obtaining the 2nd sequence differs from that of the second embodiment and a threshold decision method is used. Therefore, the construction of the ACS circuit 62 and path memory circuit 63 also differs. Construction of the other parts is the same as that of the second embodiment. Accordingly, a 2nd sequence presuming system by the threshold decision method in the Viterbi detector will now be described.

Fig. 23B shows a principle of the 2nd sequence detection system according to the threshold decision method. According to this system, in the ACS arithmetic operation, when a difference between the likelihoods to be compared is smaller than a certain threshold value, the best sequence is outputted as a path memory of the path selected by the ACS and the 2nd sequence is outputted as a path memory of the path which is not selected by the ACS. When the likelihood difference is not smaller than the certain threshold value, the path memory of the path selected by the ACS is outputted for both of the best and 2nd sequences. That is, when the likelihood difference in the ACS is small, it is decided that a probability that a

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decoding error occurs is high. The selected path is determined to be the best sequence as a first candidate and the path which is not selected is decided to be the 2nd sequence as a second candidate. When the likelihood difference is sufficiently large, the sequence which was likelihood presumed is stored for both of the best and 2nd sequences without distinguishing them. For example, in the ACS in the state S0, the likelihoods to be compared are {α = S0 + BM(0), β = S4 + BM(-1)}. Now, assuming that either one of α and β is correct, the absolute value of the likelihood difference dM = α - β is theoretically equal to 4 when there is no noise. However, actually, dM varies depending on the noises and a situation that α and β cannot be clearly distinguished occurs. Therefore, whether the reliability of the selected result by the ACS is high or not depends on the magnitude of likelihood difference dM, and consequently, the 2nd sequence is determined on the basis of evaluating dM. Now, assuming that the threshold value is equal to DM, as shown in Fig. 23B, the best and 2nd sequences are determined depending on the regions A, B, C and D where the magnitude relations between the likelihood difference dM and threshold value DM are labeled. They are also similarly decided with respect to the other states S1, ..., and S7.

As a threshold value DM, the value of the half of the maximum likelihood in an ideal case, namely, in case of no error, specifically speaking, the value of (MSED of the PR4 channel)/4 is used.

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Fig. 13 shows a construction of the ACS circuit 62 to realize the above processes. In the diagram, the best and 2nd sequences are obtained by applying the threshold decision method. In the diagram, the processes up to the addition and the comparison are the same as those of the conventional invention and the first embodiment.

In the embodiment, likelihood differences DM0, ..., and DM7 are outputted as outputs of the comparators 111 in place of the survivor paths. The likelihood differences DMi (i = 0, ..., 7) are inputted to a path discriminator 7. On the basis of the foregoing principle, the survivor path information (C0-1, C0-2), ..., and (C7-1, C7-2) showing the best sequence and the 2nd sequence are outputted to the path memory circuit by the values of DMi. (Ci-1, Ci-2) (i = 0, ..., 7) are expressed by one bit of 0 or 1. A construction of the path discriminator 7 is shown in Fig. 14. In the diagram, when the likelihood difference DMi is inputted, its absolute value is calculated in an absolute value converter 71. At the same time, a code bit of the DMi is inputted to a path selector 73. The absolute value is compared with a threshold value DM by a comparator 72. In the actual process, the threshold value DM is subtracted from the absolute value and the code bit is outputted to the path selector 73. From the two bits of the code bit of the DMi and an output of the comparator 72, the path selector 73 outputs the survivor path information Ci-1 and Ci-2 (i = 0, ..., 7) for the best and 2nd

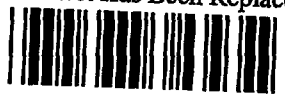
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sequences to the path memory circuit 63. By the processes of the construction shown in Fig. 14, any one of the decision regions A, B, C, and D (refer to Fig. 23B) to which the likelihood difference DMi belongs is specified, thereby deciding the survivor path information Ci-1 and Ci-2 for the decision region.

On the other hand, the path memory circuit 63 outputs the Viterbi decoded results for the best and 2nd sequences by the trace back process from the survivor path information. Fig. 15 shows a constructional conceptual diagram of the path memory circuit 63. In the diagram, the selectors (0.1, 0.2), ..., and selectors (7.1, 7.2) (221) are circuits for selecting the registers corresponding to the survivor path information (Ci-1, Ci-2) (i = 0, ..., 7) from the path memory registers 200 ((reg0.1.1, reg0.1.2), ..., (reg7.1.1, reg7.1.2) and (reg0.2.1, reg0.2.2), ..., (reg7.2.1, reg7.2.2)) for the best and 2nd sequences in the states S0, ..., and S7, respectively. Best parallel data careers R0, ..., and R7 and 2nd parallel data careers R0', ..., and R7' of the paths which are the same as path memory length have been stored in the path memory registers 200, at each corresponding state respectively. They are feedback connected to the corresponding signal lines, respectively. When the survivor path information (Ci-1, Ci-2) is inputted, a selector 221 selects the corresponding path memory register 200 by those information and outputs the data into the registers (ri.1, ri.2) (202), respectively. On the other hand, a data selector 222

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outputs the corresponding data by the survivor path information (Ci-1, Ci-2). The registers (ri.1, ri.2) (202) are also shift registers to which the data (outputs of the data selectors 222) for the selected best and 2nd paths is serially inputted. The data which was shifted out is a decoding output. When the path memory length is set to be sufficiently long, the serial outputs in all of the states are the same (the paths after the trace back have been merged). Therefore, the Viterbi decoded results for the best and 2nd sequences are obtained here by using the serial output in the state S0, respectively.

For easy understanding of the operation concept here, the path memory registers 200 are shown in the diagram. In the actual circuit construction, however, the above operation can be realized by directly connecting to the selector 221 by using only the registers ri.1 and ri.2 (202) without using the path memory registers 200.

By the above processes, in the Viterbi detector in Fig. 6, the decoding data for the best and 2nd sequences is outputted to the erasure error detector 64 by the path memory circuit 63. The subsequent processes are the same as those in the second embodiment (Fig. 9).

(4) Fourth embodiment

Although the first to third embodiments are characterized by the step of decoding by the reproducing apparatus, the fourth embodiment is characterized by both of a step of encoding information and a step of decoding.

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Fig. 16 shows a whole constructional diagram of the embodiment.

In Fig. 16, a second ECC encoder 9 and a second ECC decoder 28 are provided in place of the modulation code encoder 11 and modulation code decoder 22 in the conventional invention (Fig. 1).

An encoding of recording information will now be described.

The digital information A is subjected to a first ECC encoding by using the Reed-Solomon code or the like by the ECC encoder 10 in a manner similar to the conventional technique and becomes a format shown in Fig. 17A.

The sequence which was subjected to the first ECC encoding is further subjected to a second encoding by the second ECC encoder 9. First, the sequence shown in Fig. 17A is divided into small blocks of a fixed length, for example, on a 8-bit or 16-bit unit basis. A second ECC encoding is executed on the small blocks. A Hamming code, a parity check code, or the like can be applied to the encoding in this instance. The first ECC encoding and the second ECC encoding can employ any method so long as it is an ECC encoding. However, in order to raise a coding rate and error correcting ability, it is better to use different methods. After the second ECC encoding was executed, the data becomes a data block of a form shown in Fig. 17B. The data block comprises a sync signal and a recording code. The sync signal is an overhead to detect the head of the

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data block. The overhead portion is removed upon inputting to the recording medium.

The sequence encoded as mentioned above is magnetically recorded to the recording medium 15 such as a magnetic disk or the like through the precoder 12, amplifier 13, and recording head 14 in a manner similar to the conventional invention.

On the reproducing side as well, information recorded on the magnetic recording medium 15 is reproduced as an electric analog signal by the reproducing head 16 and amplifier 17 and passes through the variable gain amplifier 18 and A/D converter 19 and is inputted to the PR equalizer (EPR4 equalization, here) 20 as a digital signal which was sampled at a proper timing. The EPR4 equalized sequence is maximum likelihood decoded by a Viterbi detector 27. The Viterbi detector 27 outputs the decoded result (there is also a case where it is outputted together with the 2nd sequence) obtained by the maximum likelihood sequence presumption to the second ECC decoder 28. In the second ECC decoder 28, a second ECC decoding is executed on every recording block by using the Viterbi decoded result and the erasure bit detection flag, thereby correcting errors which cannot be corrected by the Viterbi decoding. The corrected sequence is further subjected to a random byte error correction (first ECC decoding) in the ECC decoder 26 by using the Reed-Solomon decoding or the like and, after that, reproducted information A' is obtained.

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Fig. 18 shows a construction of the Viterbi detector 27 and second ECC decoder 28 showing the embodiment. In the diagram, although the Viterbi detector 27 is constructed by the branch metric calculator 41, ACS circuit 52, and path memory circuit 53, since they have the same construction as that (refer to Figs. 5, 6, and 7) mentioned in the first embodiment, their descriptions are omitted. The Viterbi decoded result (1, 0, X) obtained as mentioned above is inputted to the second ECC decoder 28. In the second ECC decoder 28, the erasure error corrector with the construction shown in Fig. 19 is used. In the embodiment, the Viterbi decoded output has three values of 1, 0, and erasure X (= 0.5) and the erasure error correction circuit in Fig. 19 executes the erasure error correcting process by using those values. That is, the Viterbi decoded result is converted from the serial data to the parallel data (data length is equal to A in Fig. 17B) by an S/P converter 170 and an erasure error is corrected by executing an ordinary ECC decoding by an erasure error correction circuit 171. A corrected result becomes a decoded output. When the erasure error cannot be corrected by the erasure error correction circuit 171, namely, when the number of errors exceeds the error correcting ability by the ECC decoding, the erasure byte detection flag flg-ebyte (= 1) is outputted together with the decoded result to the ECC decoder 26. The ECC decoder 26 inputs the decoded result and the erasure byte detection flag and executes an erasure error correction. As mentioned in the

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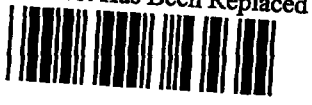
first embodiment, if the erasure error can be properly detected, its correcting ability is improved to about two times of that of the random error correction.

(5) Fifth embodiment

The fifth embodiment is almost the same as the fourth embodiment except that a construction of the Viterbi detector 27 and the second ECC decoder 28, as shown in Figs. 20 and 21, slightly differs from that shown in Figs. 18 and 19.

In Fig. 20, the Viterbi detector 27 is constructed by the branch metric calculator 41, ACS circuit 62, and path memory circuit 63, since they have the same construction as that (refer to Figs. 9, 10, 11, 13, and 15) mentioned in the second and third embodiments, their descriptions are omitted. In the embodiment, the best sequence and the 2nd sequence are outputted from the Viterbi detector to the second ECC decoder 28 by the foregoing method, namely, the systematic searching method or threshold decision method. A decoding error detector with a construction shown in Fig. 21 is used in the second ECC decoder 28. In the diagram, the best and 2nd sequences are converted into the parallel data (data length is equal to A in Fig. 17B) by the S/P converters 170 and a process is executed in an error detection circuit 180 on a data length unit basis. In the error detection circuit 180, the second ECC decoding is simultaneously and independently

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executed for each of the best and 2nd sequences and the error detection is performed. The error detection circuit 180 calculates error detection result for each of the best and 2nd sequences, namely, syndromes S1 and S2 and outputs them to a selector 181 together with the decoded best and 2nd sequences, respectively. The selector 181 determines that the sequence in which both of the syndromes S1 and S2 are equal to 0 (no error detection) is the correct decoded result, and selects and outputs it. At the same time, the erasure byte detection flag flg-ebyte is outputted as 0. When both of S1 and S2 are equal to 0, any one of the best and 2nd sequences can be outputted. At this instance, the erasure byte detection flag flg-ebyte is equal to 0. When both of S1 and S2 are equal to 1 (an error is detected), since this means that an error occurs in both of the sequences, the erasure byte detection flag flg-ebyte is set to 1 and the best sequence is outputted. The sequence selected by the selector 181 is sent as a decoded result to the ECC decoder 26 together with the flag flg-ebyte. The ECC decoder 26 receives the decoded result and the erasure byte detection flag and executes an erasure error correction (first ECC decoding).

(6) Sixth embodiment

The sixth embodiment is a modification of the fifth embodiment and differs from the fifth embodiment with respect to only the second ECC decoder 28. A construction

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of the second ECC decoder 28 of the embodiment is shown in Fig. 22.

In the diagram, each of the best and 2nd sequences are converted into the parallel data by the S/P converters 170 (data length is equal to A in Fig. 17B) and a process is executed on a data length unit basis. The exclusive OR of the best and 2nd sequences converted into the parallel data is calculated every bit by an exclusive OR circuit 190. A result is outputted as an erasure error detection signal to an erasure error correction circuit 191. When all bits of the erasure error detection signal are equal to 0, it is possible to decide that no erasure error occurs. When any one of the bits of the erasure error detection signal is equal to 1, it is considered that an erasure error occurs at the bit position. The erasure error correction circuit 191 inputs the best sequence converted into the parallel data and the erasure error detection signal and executes an erasure error correction decoding (second ECC decoding) process. Thus, when the error is corrected, the erasure byte detection flag flg-ebyte (= 0) is outputted. When the error cannot be corrected, the flg-ebyte (= 1) is outputted. The sequence which was erasure error correction decoded by the above process is sent as a decoded result to the ECC decoder 26 together with flg-ebyte. The ECC decoder 26 inputs the decoded result and the erasure byte detection flag and executes an erasure error correction (first ECC decoding).

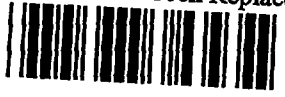
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(7) Modifications

The invention can be also applied to arbitrary PR channels (PR4, EEPR4, etc.) other than the EPR4 channel. The invention can also be applied to a signal processing system to which a maximum likelihood detecting function based on the concept of the Viterbi decoding or the like is generally applied, for example, a DFE-FDTS (Decision Feedback Equalizer with Finite Delay Tree Search) system and the like.

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WHAT IS CLAIMED IS:

1. A digital magnetic reproducing apparatus comprising:

an apparatus for partial response (PR) equalizing a signal which is reproduced from a magnetic recording medium and is error correction code (ECC) encoded and outputting a PR equalized sequence;

a Viterbi detector for performing a maximum likelihood sequence presumption on said PR equalized sequence and outputting a maximum likelihood sequence; and

an ECC decoder for ECC decoding said maximum likelihood sequence,

wherein said Viterbi detector detects an erasure error at the time of the maximum likelihood sequence presumption and outputs erasure error information indicating that an erasure error is detected and showing a position of the detected error in the sequence together with said maximum likelihood sequence, and

said ECC decoder executes an ECC decoding by using said erasure error information.

2. An apparatus according to claim 1, wherein

when each state likelihood is calculated, compared, and selected, in the case where an absolute value of a difference between two state likelihoods to be compared is equal to or less than a certain threshold value, said Viterbi detector determines the occurrence of an erasure error.

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3. An apparatus according to claim 2, wherein said certain threshold value is a value of a (Minimum Squared Euclidean Distance (MSED))/4 of the PR sequence.

4. An apparatus according to claim 2, wherein said Viterbi detector sets a flag on a bit in which the erasure error of said maximum likelihood sequence is detected and outputs as said erasure error information together with said maximum likelihood sequence.

5. An apparatus according to claim 1, wherein said Viterbi detector selects a best sequence and a second sequence at the time of the maximum likelihood sequence presumption, obtains an exclusive OR of both of said sequences, and outputs the exclusive OR as erasure error information together with the best sequence.

6. An apparatus according to claim 5, wherein said Viterbi detector stores paths having a maximum likelihood and a second maximum likelihood every state at the time of the maximum likelihood sequence presumption and sets said paths to the best sequence and the second sequence.

7. An apparatus according to claim 5, wherein when each state likelihood is calculated, compared, and selected, in the case where an absolute value of a difference between two state likelihoods to be compared is smaller than a certain threshold value, said Viterbi detector sets a path corresponding to the large state likelihood to the best sequence, sets a path corresponding to the small state likelihood to the second sequence, and when the absolute value of the difference

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between the state likelihoods is equal to or larger than said certain threshold value, said Viterbi detector equalizes the best sequence and the second sequence.

8. An apparatus according to claim 7, wherein said certain threshold value is a value of a (Minimum Squared Euclidean Distance (MSED))/4 of the PR sequence.

9. A digital magnetic recording and reproducing apparatus comprising:

an ECC encoder for performing a first ECC encoding on data, further dividing the data which is first ECC encoded into predetermined lengths, executing a second ECC encoding on the divided data, and forming data to be recorded to a recording medium;

an apparatus for partial response (PR) equalizing a reproduction signal reproduced from said recording medium and outputting a PR equalized sequence;

a Viterbi detector for performing a maximum likelihood sequence presumption on said PR equalized sequence and outputting a maximum likelihood sequence; and

an ECC decoder for executing a second ECC decoding on said maximum likelihood sequence and, further, executing a first ECC decoding,

wherein said Viterbi detector detects an erasure error at the time of the maximum likelihood sequence presumption and sets a maximum likelihood sequence corresponding to a position where an erasure error is detected to a predetermined value X other than 0.1, and

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at the time of the second ECC decoding, said ECC decoder regards that the value of X as an error, executes an ECC decoding, when the error correction is impossible, determines that said data which is second ECC decoded includes the erasure error, and gives erasure error information, and at the time of the first ECC decoding, said ECC decoder executes the error correction by using said erasure error information.

10. An apparatus according to claim 9, wherein when each state likelihood is calculated, compared, and selected, in the case where an absolute value of a difference between two state likelihoods to be compared is equal to or less than a certain threshold value, said Viterbi detector determines the occurrence of an erasure error.

11. An apparatus according to claim 10, wherein said certain threshold value is a value of a (Minimum Squared Euclidean Distance (MSED))/4 of the PR sequence.

12. A digital magnetic recording and reproducing apparatus comprising:

an ECC encoder for performing a first ECC encoding on data, further dividing the data which is first ECC encoded into predetermined lengths, executing a second ECC encoding on the divided data, and forming data to be recorded to a recording medium;

an apparatus for partial response (PR) equalizing a reproduction signal reproduced from said recording medium and outputting a PR equalized sequence;

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a Viterbi detector for performing a maximum likelihood sequence presumption on said PR equalized sequence, selecting a best sequence and a second sequence, and outputting both of said sequences; and

an ECC decoder for executing a second ECC decoding to both of said sequences and, further, executing a first ECC decoding to one of said sequences.

13. An apparatus according to claim 12, wherein said Viterbi detector stores paths having a maximum likelihood and a second maximum likelihood at every state at the time of the maximum likelihood sequence presumption and sets said paths to the best sequence and the second sequence.

14. An apparatus according to claim 12, wherein

when each state likelihood is calculated, compared, and selected, in the case where an absolute value of a difference between two state likelihoods to be compared is smaller than a certain threshold value, said Viterbi detector sets a path corresponding to the large state likelihood to the best sequence, sets a path corresponding to the small state likelihood to the second sequence, and when the absolute value of the difference between the state likelihoods is equal to or larger than said certain threshold value, said Viterbi detector equalizes the best sequence and the second sequence.

15. An apparatus according to claim 14, wherein said certain threshold value is a value of a (Minimum Squared Euclidean Distance (MSED))/4 of the PR sequence.

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16. An apparatus according to claim 12, wherein said ECC decoder respectively calculates syndromes at the time of the second ECC decoding of both of said sequences and executes a first ECC decoding on the sequence in which said syndrome is equal to 0, and when both of the syndromes of both of said sequences are equal to 1, said ECC decoder determines that said data which is second ECC decoded includes an erasure error, adds erasure error information, and executes a first ECC decoding by using the best sequence and said erasure error information.

17. An apparatus according to claim 12, wherein said ECC decoder sets an exclusive OR of results of said second ECC decoding of both of said sequences to erasure error information and executes a first ECC decoding by using the best sequence and said erasure error information.

18. A reproducing method of a digital magnetic signal, comprising the steps of:

partial response (PR) equalizing a signal which is reproduced from a magnetic recording medium and is ECC encoded and outputting a PR equalized sequence;

performing a maximum likelihood sequence presumption on said PR equalized sequence and outputting a maximum likelihood sequence;

ECC decoding said maximum likelihood sequence;

detecting an erasure error at the time of said maximum likelihood sequence presumption and outputting erasure error information indicating that the erasure error

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is detected and showing a position of the detected error in the sequence together with said maximum likelihood sequence; and

executing an ECC decoding by using said erasure error information at the time of said ECC decoding.

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