A CONTROL SYSTEM OF FIFO MEMORIES

ABSTRACT

To reduce access frequency to a CPU for recording/reproducing digital audio data, a control system of FIFO memories of the invention applied to an sound codec apparatus comprises means (2, 4, 7, 9 and 10) for controlling a first and a second FIFO memory (3 and 8) to store recording data sequentially and to output stored recording data sequentially when the apparatus is used exclusively for recording; and controlling the first and the second FIFO memory to store the reproducing data sequentially and to output the stored reproducing data sequentially when the apparatus is used exclusively for reproducing.

Fig. 1