ABSTRACT

LOW TRIGGERING N MOS TRANSISTOR FOR ESD PROTECTION WORKING UNDER FULLY SILICIDED PROCESS WITHOUT SILICIDE BLOCKS

An ESD device and method using parasitic bipolar transistors that are silicided. The first embodiment is a parasitic Bipolar Junction Transistor comprised of n+/n- /p-/n-/n+ regions. The emitter is formed of the second N+ region and the second N- well. The parasitic base is formed by the p- substrate or well. The collector is formed of the first well and the first n+ region. The benefit of the first embodiment is the trigger voltage is lower because the junction between the n- well (emitter) and P- substrate (base) and the junction between P-substrate (base) and the n-well have lower cross over concentrations. The second embodiment is similar to the first embodiment with the addition of the first gate. The first gate is preferably connected to the first n+ region and the Vpad. The third embodiment contains the same elements as the second embodiment with the addition of a third n+ region. The third n+ region is preferably shorted (or connected) to the first p+ region and the second n+ region. The third embodiment forms a second NPN parasitic bipolar using the third N+ region as an emitter. The forth embodiment contains the same elements as the third embodiment with the addition of a second gate over the first isolation region. The second gate is preferably connected to the third n+ region to the first p+ region and the second n+ region. The gate changes the electrical characteristics of the first parasitic bipolar transistor.

(FIGURE 1 IS SUGGESTED FOR PUBLICATION)