CLAIMS:

1. A switching device comprising:

Peripheral Component Interconnect Express (PCIe) upstream ports configured to couple to a host;

a PCIe downstream port coupled to the PCIe upstream ports and configured to couple to an input/output (I/O) device;

an internal connection line; and

an internal processing apparatus coupled to the PCIe downstream port using the internal connection line and configured to:

transmit a configuration read/write packet to the PCIe downstream port using the internal connection line,

receive, from the PCIe downstream port, in response to the configuration read/write packet, and using the internal connection line, a configuration read/write response packet comprising a completer identification,

determine, according to the completer identification, that the switching device is coupled to the I/O device whose identification is the completer identification;

whereby when it is determined that the switching device is coupled to the I/O device whose identification is the completer identification, PCIe configuration content of the I/O device is stored, a function of the I/O device is virtualized; and a mapping between a first PCIe domain corresponding to the host and a second PCIe domain corresponding to the I/O device is implemented.

2. The switching device of claim 1, wherein the internal processing apparatus is further configured to store a first mapping relationship from a first identification in the first PCIe domain to a second identification in the second PCIe domain.

3. The switching device of claim 2, wherein the internal processing apparatus is further configured to store a second mapping relationship from the second identification to the first identification.

4. The switching device of claim 3, wherein the switching device is configured to store a mapping table comprising a base address register (BAR) address and a BAR size of a virtual function of the I/O device.

5. The switching device of claim 1, further comprising:

a host switching device comprising the PCIe upstream ports;

an Ethernet interface; and

an I/O switching device coupled to the host switching device via the Ethernet interface and comprising:

the internal processing apparatus,

a virtual endpoint device,

a mirroring endpoint device, and

the PCIe downstream port.

6. The switching device of claim 1, wherein the internal processing apparatus is further configured to:

receive an initialization instruction from a management baseboard management controller (BMC) in the host; and

further transmit the configuration read/write packet according to the initialization instruction

7. The switching device of claim 6, wherein the internal processing apparatus is further configured to report, to the management BMC after the I/O device couples to the switching device, identification information identifying the I/O device.

8. The switching device of claim 1, wherein the internal processing apparatus is further configured to:

receive configuration management information from a management baseboard management controller (BMC) in the host; and

configure the PCIe upstream ports and the PCIe downstream port according to the configuration management information.

9. The switching device of claim 1, wherein the internal processing apparatus is further configured to process an exception event and a hot swap event.

10. A Peripheral Component Interconnect Express (PCIe) system comprising:

a host comprising a management baseboard management controller (BMC), wherein the management BMC comprises a configuration management function;

an input/output (I/O) device; and

a switching device comprising:

Peripheral Component Interconnect Express (PCIe) upstream ports configured to couple to the host;

a PCIe downstream port coupled to the PCIe upstream ports and configured to couple to the I/O device;

an internal connection line; and

an internal processing apparatus coupled to the PCIe downstream port using the internal connection line and configured to:

transmit a configuration read/write packet to the PCIe downstream port using the internal connection line,

receive, from the PCIe downstream port, in response to the configuration read/write packet, and using the internal connection line, a configuration read/write response packet comprising a completer identification,

determine, according to the completer identification, that the switching device is coupled to the I/O device whose identification is the completer identification;

whereby when it is determined that the switching device is coupled to the I/O device whose identification is the completer identification, PCIe configuration content of the I/O device is stored, a function of the I/O device is virtualized; and a mapping between a first PCIe domain corresponding to the host and a second PCIe domain corresponding to the I/O device is implemented.

11. The PCIe system of claim 10, further comprising a PCIe switch, wherein the PCIe downstream port is further configured to further couple to the I/O device using the PCIe switch.

12. The PCIe system of claim 10, further comprising a shelf management module (SMM), wherein the management BMC is configured to send, to the SMM, networking configuration information of the host, the switching device, and the I/O device.