

Claims

1. A method of making an integrated circuit, the method comprising:
depositing a cap layer containing at least one dopant onto a gapfill metal; and
5 annealing so that the at least one dopant migrates to grain boundaries and/or
interfaces of the gapfill metal, the interfaces comprising:
tantalum and/or tantalum nitride,
titanium and/or titanium nitride,
an organic layer,
10 a self-assembled monolayer,
an organic self-assembled monolayer, or
an amorphous carbon layer.
2. The method of claim 1, wherein the at least one dopant comprises manganese.
- 15 3. The method of claim 1, wherein the cap layer comprises cobalt or nickel and the
at least one dopant comprises manganese.
4. The method of claim 1, wherein the cap layer comprises cobalt or nickel and the
20 at least one dopant comprises arsenic, gallium, germanium, iron, lead, mercury,
vanadium, or mixtures thereof.
5. The method of claim 1, wherein the at least one dopant comprises arsenic,
gallium, germanium, iron, lead, mercury, vanadium, or mixtures thereof.
- 25 6. The method of claim 1, wherein the at least one dopant comprises antimony,
bismuth, cadmium, chromium, gold, indium, iridium, molybdenum, osmium, palladium,
platinum, rhenium, rhodium, ruthenium, silver, technetium, thallium, tin, zinc, or
mixtures thereof.
- 30 7. The method of claim 1, wherein the at least one dopant comprises boron,
molybdenum, phosphorus, tungsten, or mixtures thereof.

8. The method of claim 1, wherein the cap layer comprises gold, palladium, platinum, rhenium, ruthenium, silver, zinc, or mixtures thereof and the at least one dopant comprises manganese.

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9. The method of claim 1, wherein the cap layer comprises gold, palladium, platinum, rhenium, ruthenium, silver, zinc, or mixtures thereof and the at least one dopant comprises arsenic, gallium, germanium, iron, lead, mercury, vanadium, or mixtures thereof.

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10. The method of claim 1, wherein the cap layer comprises gold, palladium, platinum, rhenium, ruthenium, silver, zinc, or mixtures thereof and the at least one dopant comprises antimony, bismuth, cadmium, chromium, indium, iridium, molybdenum, osmium, rhodium, technetium, thallium, tin, or mixtures thereof.

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11. The method of claim 1, wherein the interfaces comprise:
tantalum and/or tantalum nitride; or
titanium and/or titanium nitride.

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12. The method of claim 1, wherein the cap layer further comprises tungsten and/or boron.

13. The method of claim 1, wherein the cap layer comprises cobalt, tungsten, and boron.

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14. The method of claim 1, wherein the cap layer comprises cobalt, tungsten, and phosphorous.

15. An integrated circuit made by the method of claim 1.

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16. A method of making an integrated circuit comprising:
forming a metal gapfill;
depositing a cap layer on the metal gapfill, the cap layer having at least one
dopant;
- 5 annealing to cause the at least one dopant to migrate to interfaces and/or grain
boundaries of the metal gapfill, the interfaces comprising:
- tantalum and/or tantalum nitride,
titanium and/or titanium nitride,
an organic layer,
- 10 a self-assembled monolayer,
an organic self-assembled monolayer, or
an amorphous carbon layer.
17. The method of claim 16, wherein depositing a cap layer on the metal gapfill is
15 accomplished using electroless deposition.
18. The method of claim 16, wherein forming a metal gapfill is accomplished using
electroless deposition and/or electrochemical plating.
- 20 19. The method of claim 16, wherein depositing a cap layer is accomplished using
chemical vapor deposition.
20. The method of claim 16, wherein forming a metal gapfill is accomplished using
electroless deposition and/or electrochemical plating of copper.
- 25 21. The method of claim 16, wherein depositing a cap layer is accomplished using
selective deposition.
22. The method of claim 16, wherein forming a metal gapfill is accomplished by
30 forming a substantially pure metal gapfill.

23. The method of claim 16, wherein forming a metal gapfill is accomplished by forming a substantially pure seed layer and electrochemically plating the metal gapfill on the seed layer.

5 24. A method of making an integrated circuit, the method comprising:
providing a substrate having vias and/or trenches formed in a dielectric for damascene or dual damascene metallization;
depositing a barrier layer on the dielectric, the barrier layer comprising:
10 tantalum and/or tantalum nitride,
an organic layer,
a self-assembled monolayer, or
an organic self-assembled monolayer;
depositing a substantially pure copper seed layer; growing gapfill copper on the copper seed layer so as to substantially fill the vias and/or trenches;
15 electrolessly depositing a cap layer comprising cobalt and/or nickel, and further comprising manganese onto the gapfill copper; and
annealing so that the manganese migrates to grain boundaries and/or interfaces of the copper.

20 25. The method of claim 24, wherein the barrier layer comprises tantalum and/or tantalum nitride.

26. The method of claim 24, wherein the cap layer further comprises boron, phosphorous, and/or tungsten.

25 27. The method of claim 24, wherein the cap layer comprises cobalt, tungsten, and boron.

28. The method of claim 24, wherein the cap layer comprises cobalt, tungsten, and
30 phosphorous.

29. An integrated circuit made by the method of claim 24.

30. The method of claim 1, wherein the interfaces of the gapfill metal comprise an organic layer.

5 31. The method of claim 1, wherein the interfaces of the gapfill metal comprise a self-assembled monolayer.

32. The method of claim 1, wherein the interfaces of the gapfill metal comprise an organic self-assembled monolayer.

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33. The method of claim 24, wherein the barrier layer is an organic layer.

34. The method of claim 24, wherein the barrier layer comprises a self-assembled monolayer.

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35. The method of claim 24, wherein the barrier layer is an organic self-assembled monolayer.

20 36. The method of claim 1, wherein the interfaces of the gapfill metal comprise an amorphous carbon layer.

CLAIMS

What is claimed is:

- 5 1. A method of making an integrated circuit, the method comprising:
depositing a cap layer containing at least one dopant onto a gapfill metal;
and
annealing so that the at least one dopant migrates to grain boundaries
and/or interfaces of the gapfill metal.
- 10 2. The method of claim 1, wherein the at least one dopant comprises manganese.
3. The method of claim 1, wherein the cap layer comprises cobalt or nickel and
the at least one dopant comprises manganese.
- 15 4. The method of claim 1, wherein the cap layer comprises cobalt or nickel and
the at least one dopant comprises arsenic, gallium, germanium, iron, lead,
mercury, vanadium, or mixtures thereof.
- 20 5. The method of claim 1, wherein the at least one dopant comprises arsenic,
gallium, germanium, iron, lead, mercury, vanadium, or mixtures thereof.
6. The method of claim 1, wherein the at least one dopant comprises antimony,
bismuth, cadmium, chromium, gold, indium, iridium, molybdenum, osmium,
25 palladium, platinum, rhenium, rhodium, ruthenium, silver, technetium, thallium, tin,
zinc, or mixtures thereof.
7. The method of claim 1, wherein the at least one dopant comprises boron,
molybdenum, phosphorus, tungsten, or mixtures thereof.

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8. The method of claim 1, wherein the cap layer comprises gold, palladium, platinum, rhenium, ruthenium, silver, zinc, or mixtures thereof and the at least one dopant comprises manganese.
- 5 9. The method of claim 1, wherein the cap layer comprises gold, palladium, platinum, rhenium, ruthenium, silver, zinc, or mixtures thereof and the at least one dopant comprises arsenic, gallium, germanium, iron, lead, mercury, vanadium, or mixtures thereof.
- 10 10. The method of claim 1, wherein the cap layer comprises gold, palladium, platinum, rhenium, ruthenium, silver, zinc, or mixtures thereof and the at least one dopant comprises antimony, bismuth, cadmium, chromium, indium, iridium, molybdenum, osmium, rhodium, technetium, thallium, tin, or mixtures thereof.
- 15 11. The method of claim 1, wherein the interfaces comprise:
tantalum and/or tantalum nitride; or
titanium and/or titanium nitride.
12. The method of claim 1, wherein the cap layer further comprises tungsten
20 and/or boron.
13. The method of claim 1, wherein the cap layer comprises cobalt, tungsten, and boron.
- 25 14. The method of claim 1, wherein the cap layer comprises cobalt, tungsten, and phosphorous.
15. An integrated circuit made by the method of claim 1.
- 30 16. A method of making an integrated circuit comprising:
forming a metal gapfill;

depositing a cap layer on the metal gapfill, the cap layer having at least one dopant;

annealing to cause the at least one dopant to migrate to interfaces and/or grain boundaries of the metal gapfill.

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17. The method of claim 16, wherein depositing a cap layer on the metal gapfill is accomplished using electroless deposition.

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18. The method of claim 16, wherein forming a metal gapfill is accomplished using electroless deposition and/or electrochemical plating.

19. The method of claim 16, wherein depositing a cap layer is accomplished using chemical vapor deposition.

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20. The method of claim 16, wherein forming a metal gapfill is accomplished using electroless deposition and/or electrochemical plating of copper.

21. The method of claim 16, wherein depositing a cap layer is accomplished using selective deposition.

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22. The method of claim 16, wherein forming a metal gapfill is accomplished by forming a substantially pure metal gapfill.

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23. The method of claim 16, wherein forming a metal gapfill is accomplished by forming a substantially pure seed layer and electrochemically plating the metal gapfill on the seed layer.

24. A method of making an integrated circuit, the method comprising:

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providing a substrate having vias and/or trenches formed in a dielectric for damascene or dual damascene metallization;

depositing a barrier layer on the dielectric;

depositing a substantially pure copper seed layer; growing gapfill copper on the copper seed layer so as to substantially fill the vias and/or trenches; electrolessly depositing a cap layer comprising cobalt and/or nickel, and further comprising manganese onto the gapfill copper; and
5 annealing so that the manganese migrates to grain boundaries and/or interfaces of the copper.

25. The method of claim 24, wherein the barrier layer comprises tantalum and/or tantalum nitride.

26. The method of claim 24, wherein the cap layer further comprises boron, phosphorous, and/or tungsten.

27. The method of claim 24, wherein the cap layer comprises cobalt, tungsten, and boron.

28. The method of claim 24, wherein the cap layer comprises cobalt, tungsten, and phosphorous.

29. An integrated circuit made by the method of claim 24.

30. The method of claim 1, wherein the interfaces of the gapfill metal comprise an organic layer.

31. The method of claim 1, wherein the interfaces of the gapfill metal comprise a self-assembled monolayer.

32. The method of claim 1, wherein the interfaces of the gapfill metal comprise an organic self-assembled monolayer.

33. The method of claim 24, wherein the barrier layer is an organic layer.

34. The method of claim 24, wherein the barrier layer comprises a self-assembled monolayer.

5 35. The method of claim 24, wherein the barrier layer is an organic self-assembled monolayer.

36. The method of claim 1, wherein the interfaces of the gapfill metal comprise an amorphous carbon layer.

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