SIGNAL PROCESSING SYSTEM

ABSTRACT OF THE DISCLOSURE:

A CMOS integrated signal processing system for a sampling receiver includes a timing recovery circuit, wherein an on-chip numerically controlled oscillator is operative at periods T that are initially equal to the nominal baud rate of the signals controls a sinc interpolator receiving samples at the sampling rate. A loop filter is coupled to the sinc interpolator and to the numerically controlled oscillator. The arrangement is capable of handling various symbol rates. The system includes a circuit for carrier recovery, having a second on-chip numerically controlled oscillator, a digital derotation circuit responsive to the second numerically controlled oscillator, accepting an in phase component and a quadrature component of the sampled signals. An adaptive phase error estimation circuit is coupled in a feedback loop.

FIGURE 19