ASYMMETRY COMPENSATION FOR MAGNETORESISTIVE SENSOR

This application claims priority from U.S. Provisional Application Serial No. 60/129,654, filed April 16, 1999, which is hereby incorporated by reference in its entirety as if fully set forth herein.

BACKGROUND OF THE INVENTION

FIELD OF THE INVENTION

The present invention relates to disk drives and, particularly, to improved magneto-resistive asymmetry compensation for sampled amplitude read channels.

DESCRIPTION OF THE RELATED ART

Magnetic recording systems store information on a magnetic medium using regions of different magnetization. The magnetic transitions are read to and written by magnetic heads. It is desirable for the positive and negative pulses to have equal amplitudes. However, magneto-resistive heads can produce an asymmetric response signal. That is, the positive and negative peaks can have differing amplitudes. This can cause inaccuracies in readback.

As such, there is a need for magneto-resistive asymmetry compensation in magnetic recording systems employing magneto-resistive heads.

SUMMARY OF THE INVENTION

These and other drawbacks in the prior art are overcome in large part by a system and method according to the present invention. A magneto-resistive asymmetry compensation system includes a linearizer interposed in a data path and a control loop. The control loop uses signal estimates from an interpolated timing response unit to derive a magneto-resistive asymmetry error. The error term is used to obtain a control scaling input to the linearizer. The linearizer functions to multiply the scaling multiple to the square of the input signal and then to add it back to the input signal. A DC offset control loop may be also provided.

A better understanding of the invention is obtained when the following detailed description is considered in conjunction with the following drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a block diagram of a read/write channel according to a specific embodiment of the invention;

FIG. 2 is a diagram of a read/write channel including an magneto-resistive asymmetry (MRA) control loop according to an implementation of the invention;

FIG. 3 is a diagram of an MRA error estimator according to an embodiment of the invention;

FIG. 4 is a diagram of an accumulator in an MRA asymmetry control loop according to an embodiment of the invention; and

FIG. 5 is a diagram illustrating magneto-resistive asymmetry compensation and DC-restore circuits according to an embodiment of the invention.

DETAILED DESCRIPTION OF THE INVENTION

FIGs. 1-5 illustrate a read/write channel with magneto-resistive asymmetry compensation according to an implementation of present invention. A magneto-resistive asymmetry compensation system includes a linearizer interposed in a data path and a control loop. The control loop uses signal estimates from an interpolated timing response unit to derive a magneto-resistive asymmetry error. The error term is used to obtain a control scaling input to the linearizer. The linearizer functions to multiply the scaling multiple to the square of the input signal and then to add it back to the input signal. A DC offset control loop is further provided.

FIG. 1 is a block diagram of a read/write channel according to a specific embodiment of the invention. In the read channel, a bit sequence is provided to a variable gain amplifier 10 to adjust the amplitude of the signal. DC offset control 65 and loop filter/gain error correction also may be provided. Further, an asymmetry control unit 67 including an asymmetry adjustment unit 61 and

asymmetry control 63 according to an implementation of the present invention are provided to compensate for magneto-resistive asymmetry effects.

The signal is provided to a continuous time filter (CTF) 13, such as a four pole Butterworth filter, for example, to attenuate high frequency noise and minimize aliasing into baseband after sampling. The signal is then provided to an analog-to-digital converter (ADC) 15 to sample the output of CTF 13.

A finite impulse response (FIR) filter 17 provides additional equalization of the signal to the desired response. The output of the FIR 17 is provided to an interpolated timing recovery unit 25, which is used to recover the discrete time sequence. Exemplary timing recovery is described in commonly-assigned U.S. Patent Application Serial No. 09/497,301, "Asynchronous Timing for Interpolated Timing Recovery," filed February 2, 2000, and commonly-assigned U.S. Patent Application Serial No. 09/496,617, "Synchronous Timing for Interpolated Timing Recovery," filed February 2, 2000, which are hereby incorporated by reference in their entireties as if fully set forth herein.

The output of the interpolated timing recovery unit 25 is used to provide a feedback control to the DC offset control 65, the gain error, the asymmetry control 63 and the FIR 17. The output of the interpolated timing recovery 25 is further provided to a Viterbi detector 30 and a sync detector 20. Sync mark information is then provided to the Viterbi detector 30 for use in sequence detection. The Viterbi detector output is then provided to the decoder 31 which decodes the encoding provided by the encoder (not shown). Exemplary sync mark detection is described in commonly-assigned U.S. Patent Application Serial No. 09/435,333, "Phase Assisted Synchronization Detector," filed November 5, 1999, which is hereby incorporated by reference in its entirety as if fully set forth herein. As described therein, relatively short sync byte detection may be performed, thereby saving overhead. Further, the sync byte detector is programmably polarity sensitive such that the polarity of the data stream entering the sync detector and the Viterbi detector may be flipped. Exemplary acquisition signal estimation is described in U.S. Patent Application Serial No. 09/480,314, titled "An Acquisition Signal Error Estimator," filed January 10, 2000, which is hereby incorporated by reference in its entirety as if fully set forth herein.

Exemplary Viterbi detection is described in commonly-assigned U.S. Patent Application Serial No., 09/347,598, titled "Trellis Code for EPRML", filed July 1, 1999, commonly-assigned U.S. Patent Application Serial No. 09/465,52, titled "Survival Selection Rule," filed December 16, 1999, and commonly-assigned U.S. Patent Application Serial No. 09/503,534, titled "Supporting ME2PRML and M2EPRML with the Same Trellis Structure," filed February 14, 2000, all of which are hereby incorporated by reference in their entireties as if fully set forth herein.

The magneto-resistive asymmetry compensation loop 67 is illustrated more clearly with reference to FIG. 2. As shown in FIG. 2, the output of the VGA 10 is received into the magneto-resistive (MR) linearizer unit 61, the CTF 13, ADC 15, the finite impulse response (FIR) filter 17, and the interpolated timing recovery unit 25, as discussed above. The output of the ITR 25 is then provided to an MRA error estimator 200. The MRA error estimator 200 estimates the value of the asymmetry error at the ITR output. In the implementation illustrated, the error estimate e_k is provided to a sample rate reducer and Franck filter (SRR/FF) unit 202. The sample rate reducer adds together two successive asymmetry error estimates so that the output can be sub-sampled at half speed. The remaining digital part of the MRA loop downstream from the sample rate reducer can operate at half speed. The Franck filter is a finite state machine that reduces jitter in the values being added to the MRA accumulator 60, which in turn reduces the analog switching noise in he MR linearizer 61.

The MRA accumulator 60 is a simple accumulator (integrator) where the input is scaled to vary the closed loop bandwidth. An MRA shadow register 204 is used to program a gain value. Finally, as will be explained in greater detail below, the MR linearizer 61 adds a controlled multiple of squared signal output to the signal input in order to compensate for the input distortion due to the MR head.

The MRA Aysmmetry Error Estimator 200 is illustrated in greater detail in FIG. 3. The MRA Error Estimator 200 receives two inputs r_k, s_k from the ITR unit 25. In the implementation illustrated, the input r_k is the Extended Partial Response IV (EPR4) equalized and retimed received values; the s_k are the corresponding 5-level slicer values s_k is in the set {-2, -1, 0, 1, 2}. It is noted that

the invention is not limited to an extended partial response system. Higher of lower orders of partial response may also be implemented.

Returning to FIG. 3, the received value inputs r_k are delayed (D) 220 and input to a sample error calculator unit 226. The slicer values s_k are similarly delayed (D) 222 and input to the sample error calculator 226. The sample error calculator 226 performs the subtraction $r_k - ms_k$, where ms_k is the slicer estimate of the ideal equalized sample value.

The slicer values are delayed further (D) 224 and then input to a block sign lookup unit 230, along with the two prior slicer values. The block sign lookup 230 performs the operation defined by the following table:

(s_{k-2}, s_{k-1}, s_k)	Bsgn
+/-(x, 2, y)	1
+/- (0,1,0)	1
+/- (1,1,0)	1
+/- (0,1,1)	1
+/- (1,0,x)	-1
+/- (2,0,x)	-1
+/- (x,0,1)	-1
+/- (x,0,2)	-1
All others	0

The error term e_k is then obtained by multiplying (232) the outputs of the block sign lookup 230 and the sample error calculator 226, which has been processed by the sign function 228.

The MRA error term e_{2k-1} at each odd time is added to the gain error output e_{2k} at the following (even) time. The result $e_{sac}(2k) = e_{2k-1} + e_{2k}$ is clocked into the Franck filter at half the clock rate.

The Franck filter may be implemented as a state machine operating on the half speed clock. The following table defines its operation:

	-4	-3	-2	-1	0	1	2	3

-2	-2/-4	-2/-3	0/-4	0/-3	0/-2	0/-1	0/0	0/1
-1	-1/-4	-1/-3	0/-3	0/-2	0/-1	0/0	0/1	0/2
0	0/-4	0/-3	0/-2	0/-1	0/1	0/1	0/2	0/3
1	0/-3	0/-2	0/-1	0/0	0/1	0/2	½	1/3
2	0/-2	0/-1	0/0	0/1	0/2	0/3	2/2	3/3

The rows correspond to the five possible values of the input signal $e_{sac}(2k)$, and the columns correspond to the eight possible values of a state variable σ_{2k}. The entries are of the form $f_{2k}/\ \sigma_{2k+2}$, where f_{2k} is the output and σ_{2k+2} is the next state.

The MRA accumulator 60 is shown in FIG. 4. Essentially, the MRA accumulator is a simple scaled integrator used to average the scaling value, as described below. The output f_{2k} is received into a shifter 402, which also receives an MRA gain input 404. The output of the shifter 402 is summed (406) with the delayed saturator output (408, 409), truncated (410) and then output to the MRA DAC 62. The saturator 408 performs the operation x = max (L, min(x, U)), where L is the smallest and U is the largest value that the register 409 can hold. The MRA shadow register 204 (FIG. 2) is used to program the gain value 404. More particularly, the accumulator accumulates a value M_n, where $M_{n+1} = M_n + (Y_{mr} \times f_{2k})$ and the loop gain $Y_{mr} = 2^{-11}$. In this implementation the loop gain Y_{mr} has only setting. The output M_n is provided to a DAC 62; the resulting output V_{mr} of the DAC 62 is provided to the MR linearizer 61 and is the control signal that adjusts the degree of compensation.

The MR linearizer 61 is shown in greater detail with reference to FIG. 5. A shown, the output V of the variable gain amplifier (VGA) 10 is squared and then added to signal $A=V_{mr} x\ V^2$. Thus, the signal V^2 is scaled by the control signal V_{mr} and added to the output of the VGA so that the output of the MR asymmetry compensation loop becomes $V+ V_{mr} x\ V^2$. The feedback loop acts to adjust $V_{mr} x\ V^2$ to the exact value needed to compensate for the second harmonic distortion due to the magneto-resistive head.

In addition to the MR asymmetry compensation loop, a DC restore loop 65, as shown in FIG. 5, is provided. As can be appreciated, the squared term

provided by the MR asymmetry compensation adds some DC into the signal. The DC restore loop compensates for this. The DC restore loop 65 derives a voltage V_{dc}, which is used to null the DC value of the signal into the CTF 13 and analog-to-digital converter (ADC) 15. The DC offset is measured both during preamble and data acquisition by using the output samples of the ADC 15. At each synchronous clock cycle, the error term g_n is calculated such that $g_n=r_n-s_n$, where r_n is the ITR output sample and s_n is the corresponding slicer estimate of the ideal output. According to one embodiment, the error term is calculated such that the loop gain $Y_{dc} = 2^{-9}$ (a high gain setting that is used during WRITE to IDLE recovery), or $Y_{dc}=2^{-11}$ (a low gain setting that is used when reading data). The error term is then added to the DC error accumulator 70 (box R) that accumulates a value P_n, where $P_{n+1}=P_n+g_n$. The accumulator 70 drives a digital-to-analog converter (DAC) 72, whose output V_{dc} in turn adds the DC voltage V_{dc} to the analog signal path before the CTF 13. Thus, the control loop functions to null the DC offset as measured at the ADC output.

The invention described in the above detailed description is not intended to be limited to the specific form set forth herein, but is intended to cover such alternatives, modifications and equivalents as can reasonably be included within the spirit and scope of the appended claims.

What is claimed:



1. A magneto-resistive asymmetry correction circuit, comprising:

a magneto-resistive linearizer circuit adapted to receive an input from an amplifier; and

a control circuit providing an input to said magneto-resistive linearizer circuit, said control circuit receiving as inputs a plurality of signal estimates.

2. A magneto-resistive asymmetry correction circuit in accordance with claim 1, wherein said plurality of signal estimates comprise outputs from an interpolated timing response unit.

3. A magneto-resistive asymmetry correction circuit in accordance with claim 1, wherein said control circuit determines an error term whose computation depends on a plurality of successive signal estimates.

4. A magneto-resistive asymmetry correction circuit in accordance with claim 1, wherein said control circuit includes a rate reduction unit and state machine filter operating at a half speed clock.

5. A magneto-resistive asymmetry correction circuit in accordance with claim 1, said control circuit including an error estimator, said error estimator adapted to estimate a magneto-resistive asymmetry error.

6. A magneto-resistive asymmetry correction circuit in accordance with claim 5, said control circuit including a sample rate reducer.

7. A magneto-resistive asymmetry correction circuit in accordance with claim 6, said control circuit including a state machine defined substantially as follows:

	-4	-3	-2	-1	0	1	2	3
-2	-2/-4	-2/-3	0/-4	0/-3	0/-2	0/-1	0/0	0/1
-1	-1/-4	-1/-3	0/-3	0/-2	0/-1	0/0	0/1	0/2
0	0/-4	0/-3	0/-2	0/-1	0/1	0/1	0/2	0/3
1	0/-3	0/-2	0/-1	0/0	0/1	0/2	½	1/3
2	0/-2	0/-1	0/0	0/1	0/2	0/3	2/2	3/3

wherein rows correspond to five possible values of an input signal $e_{sac}(2k)$, and columns correspond to eight possible values of a state variable σ_{2k}; and

entries are of the form f_{2k}/σ_{2k+2}, where f_{2k} is the output and σ_{2k+2} is the next state.

8. A magneto-resistive asymmetry correction circuit in accordance with claim 5, said linearizer adapted to add a multiple of a square of an input signal to said input signal.

9. A magneto-resistive asymmetry correction circuit in accordance with claim 5, including a digital finite state machine filter for attenuating analog switching noise.

10. A sampled amplitude read channel, comprising

means for receiving encoded data; and

a magneto-resistive asymmetry control loop, said magneto-resistive asymmetry control loop including:

a magneto-resistive linearizer circuit adapted to receive an input from an amplifier; and

a control circuit providing an input to said magneto-resistive linearizer circuit, said control circuit receiving as inputs a plurality of signal estimates.

11. A sampled amplitude read channel according to claim 10, wherein said plurality of signal estimates comprise outputs from an interpolated timing response unit.

12. A sampled amplitude read channel in accordance with claim 10, wherein said control circuit determines an error term whose computation depends on a plurality of successive signal estimates.

13. A sampled amplitude read channel according to claim 11, wherein said control circuit includes a rate reduction unit and state machine filter operating at a half speed clock.

14. A sampled amplitude read channel according to claim 10, said control circuit including an error estimator, said error estimator adapted to estimate a magneto-resistive asymmetry error.

15. A sampled amplitude read channel in accordance with claim 10, said linearizer adapted to add a multiple of a square of an input signal to said input signal.

16. A sampled amplitude read channel in accordance with claim 10, including a digital finite state machine filter for attenuating analog switching noise.

17. A sampled amplitude read channel in accordance with claim 10, further including a DC offset control loop adapted to compensate for a DC offset.