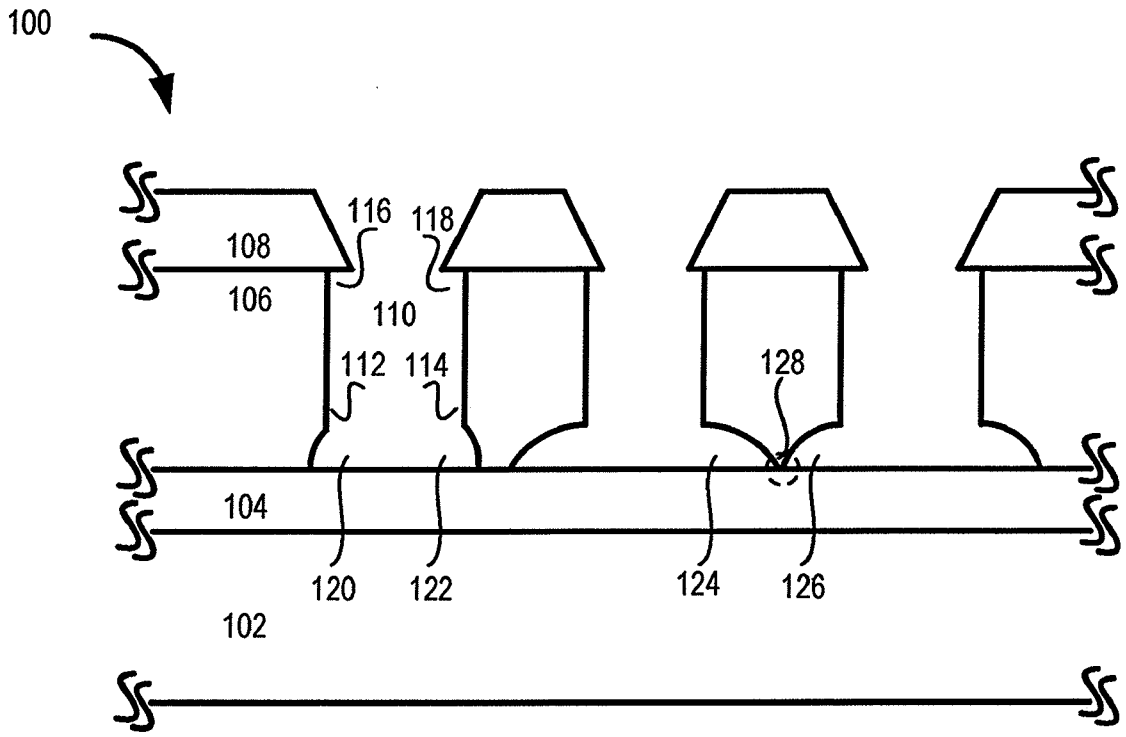


FIGURE 1
(PRIOR ART)

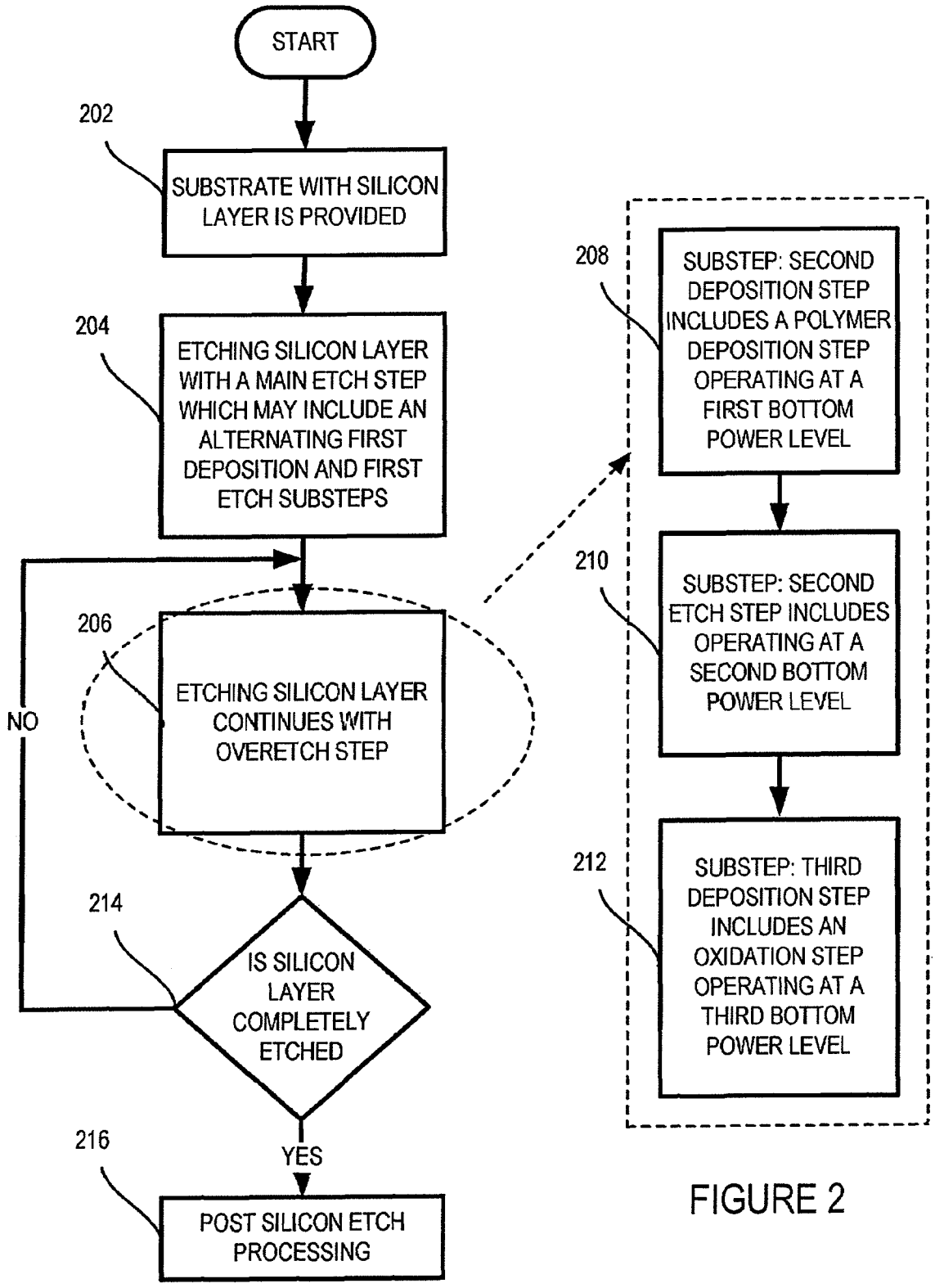

START
202
SUBSTRATE WITH SILICON LAYER IS PROVIDED
204
ETCHING SILICON LAYER WITH A MAIN ETCH STEP WHICH MAY INCLUDE AN ALTERNATING FIRST DEPOSITION AND FIRST ETCH SUBSTEPS
206
ETCHING SILICON LAYER CONTINUES WITH OVERETCH STEP
NO
214
IS SILICON LAYER COMPLETELY ETCHED
YES
216
POST SILICON ETCH PROCESSING
208
SUBSTEP: SECOND DEPOSITION STEP INCLUDES A POLYMER DEPOSITION STEP OPERATING AT A FIRST BOTTOM POWER LEVEL
210
SUBSTEP: SECOND ETCH STEP INCLUDES OPERATING AT A SECOND BOTTOM POWER LEVEL
212
SUBSTEP: THIRD DEPOSITION STEP INCLUDES AN OXIDATION STEP OPERATING AT A THIRD BOTTOM POWER LEVEL

FIGURE 2

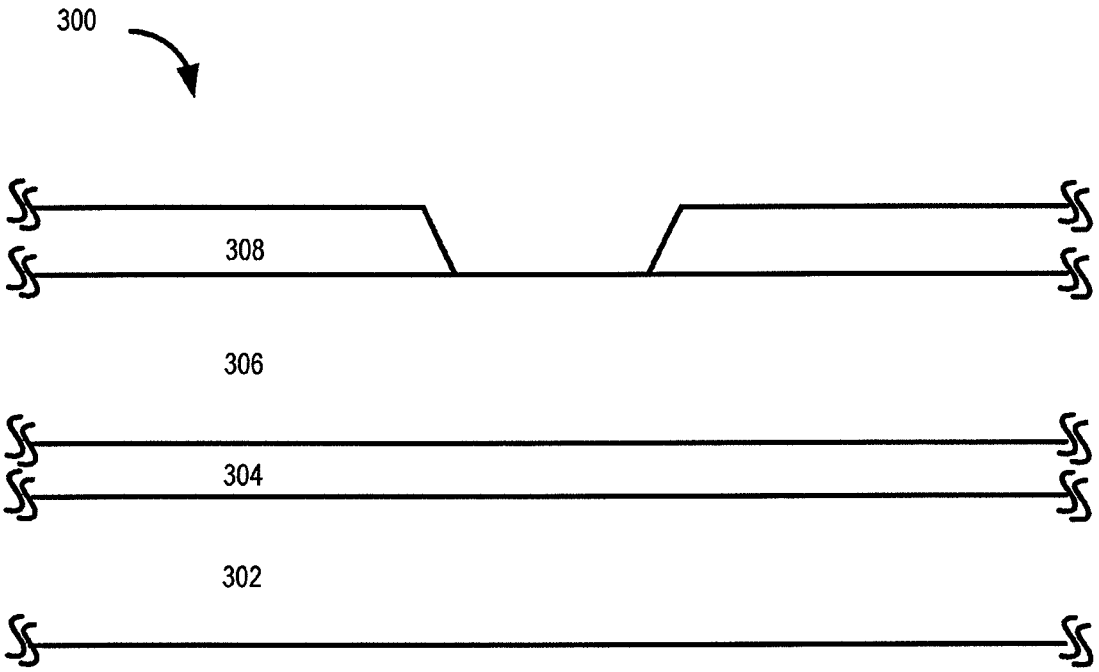


FIGURE 3

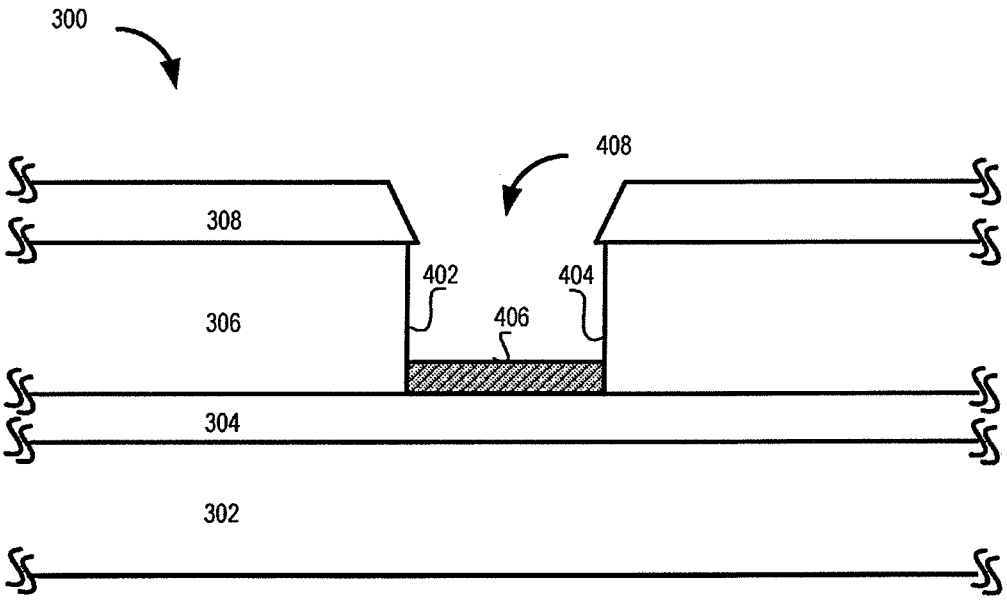


FIGURE 4

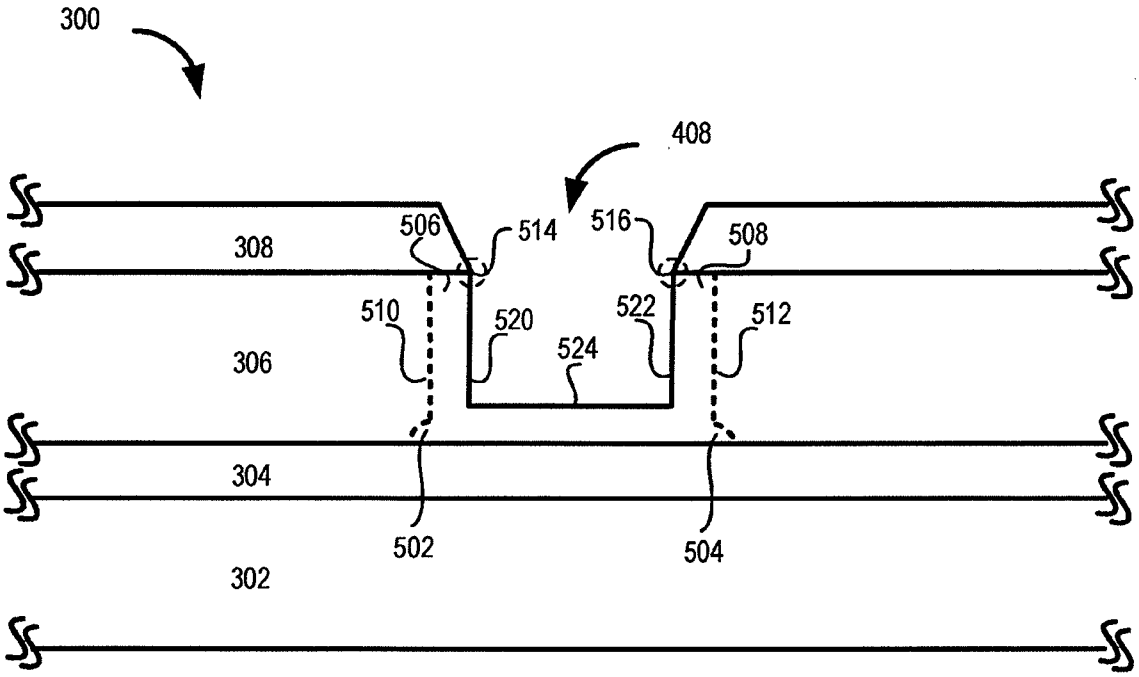

300
408
308
506
514
516
508
510
520
522
512
306
524
304
502
504
302

FIGURE 5

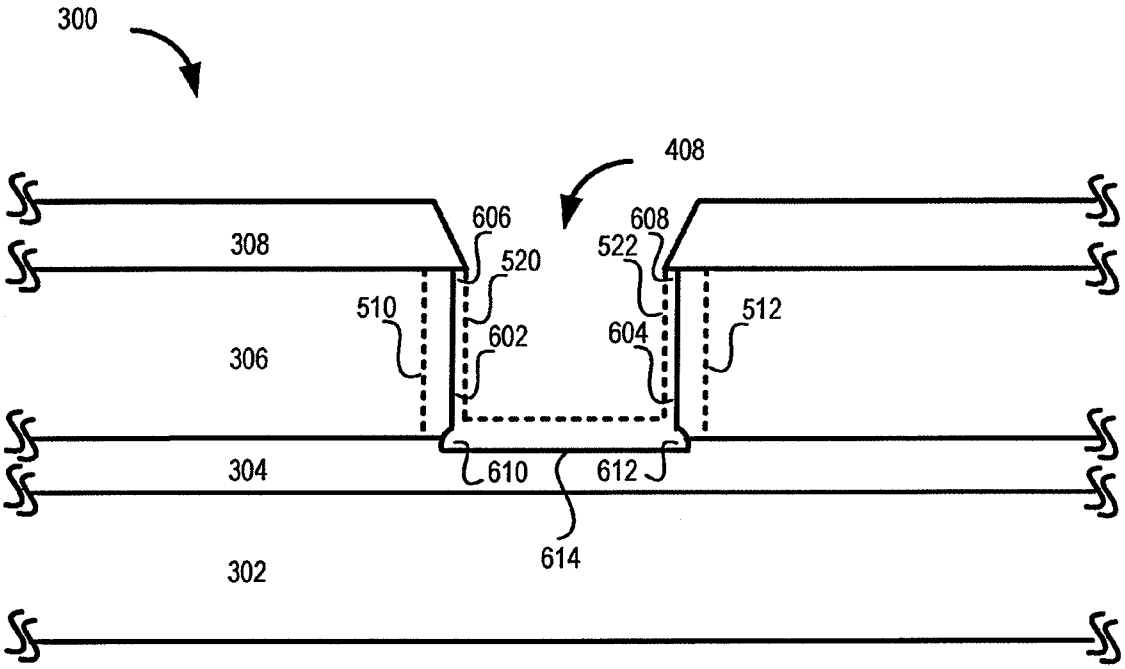

300
408
606
608
308
520
522
510
602
604
512
306
304
610
612
614
302

FIGURE 6

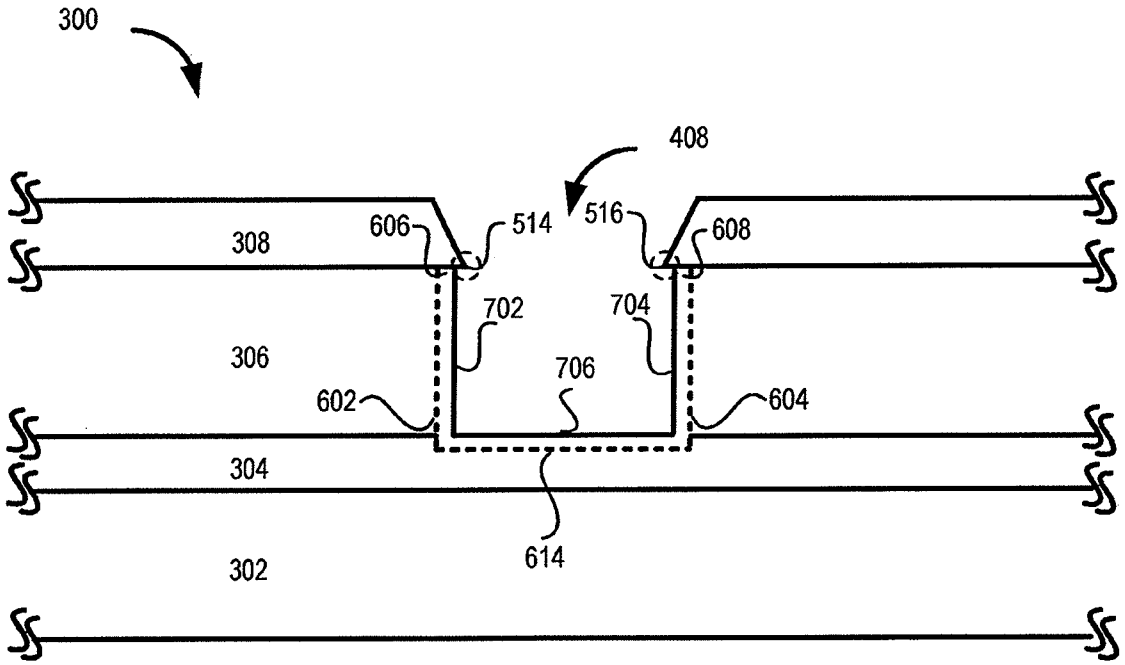


FIGURE 7

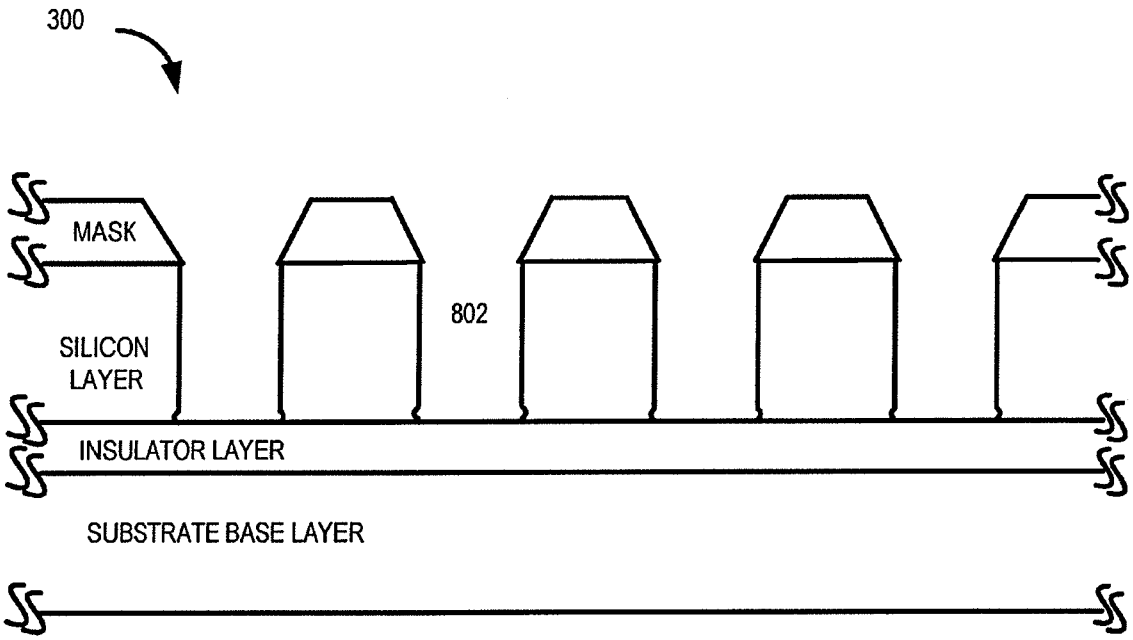

300
MASK
802
SILICON
LAYER
INSULATOR LAYER
SUBSTRATE BASE LAYER

FIGURE 8A

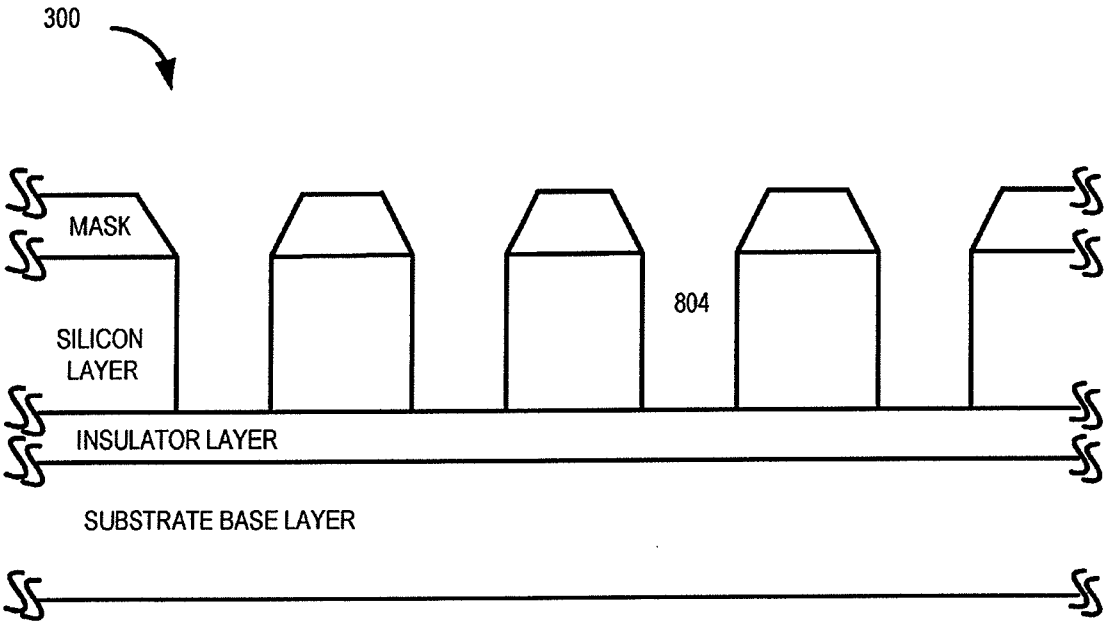

300
MASK
804
SILICON
LAYER
INSULATOR LAYER
SUBSTRATE BASE LAYER

FIGURE 8B