Fig. 1
(Prior Art)

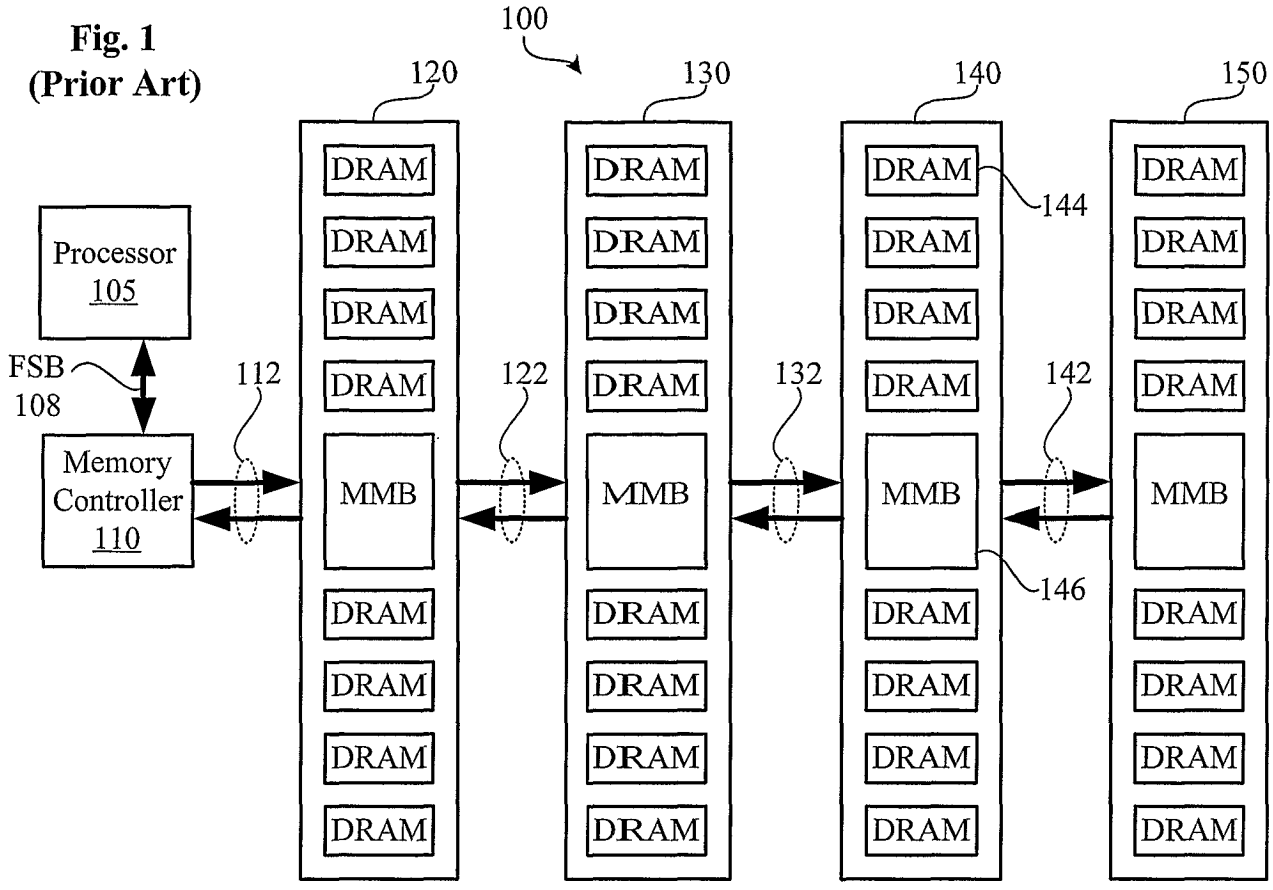
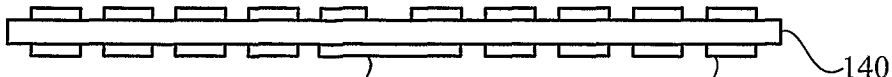


Fig. 2a
(Prior Art)



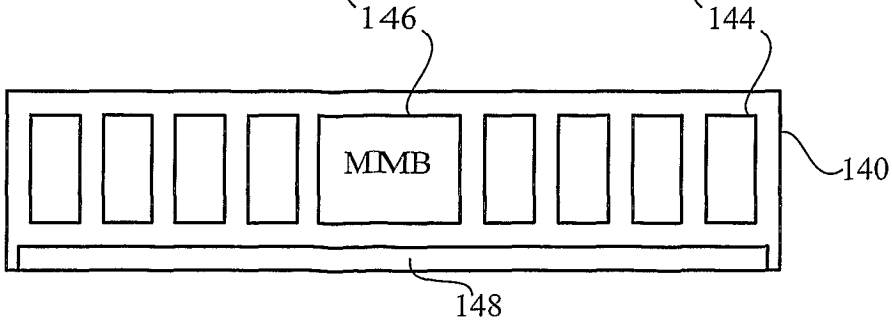


Fig. 2b
(Prior Art)

Fig. 3

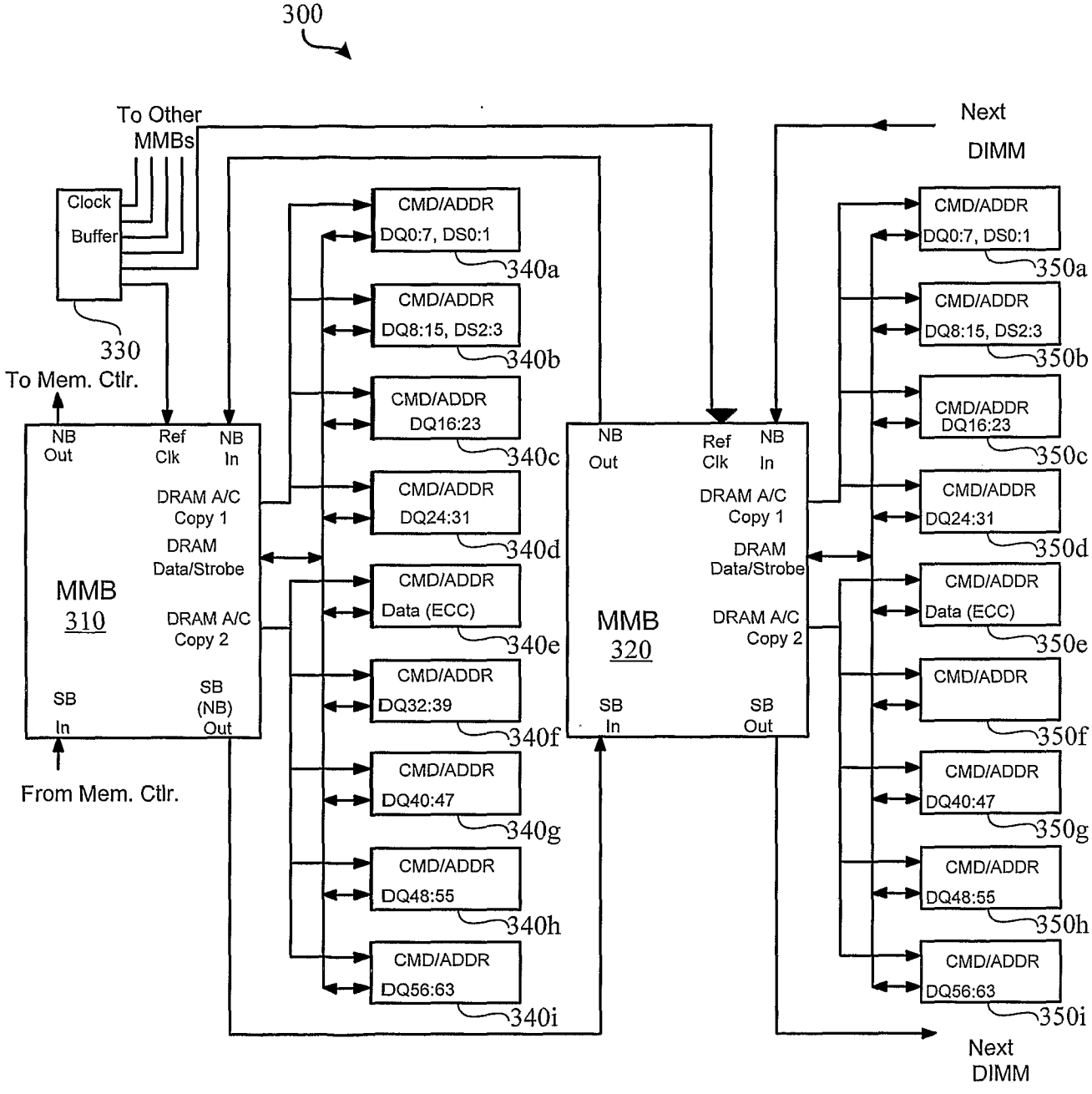

300
To Other MMBs
Clock Buffer
330
To Mem. Ctlr.
From Mem. Ctlr.
NB Out
Ref Clk
NB In
DRAM A/C Copy 1
DRAM Data/Strobe
DRAM A/C Copy 2
SB In
SB (NB) Out
MMB 310
MMB 320
SB Out
CMD/ADDR DQ0:7, DS0:1
CMD/ADDR DQ8:15, DS2:3
CMD/ADDR DQ16:23
CMD/ADDR DQ24:31
CMD/ADDR Data (ECC)
CMD/ADDR DQ32:39
CMD/ADDR DQ40:47
CMD/ADDR DQ48:55
CMD/ADDR DQ56:63
340a
340b
340c
340d
340e
340f
340g
340h
340i
Next DIMM
350a
350b
350c
350d
350e
350f
350g
350h
350i
Next DIMM

Fig. 4

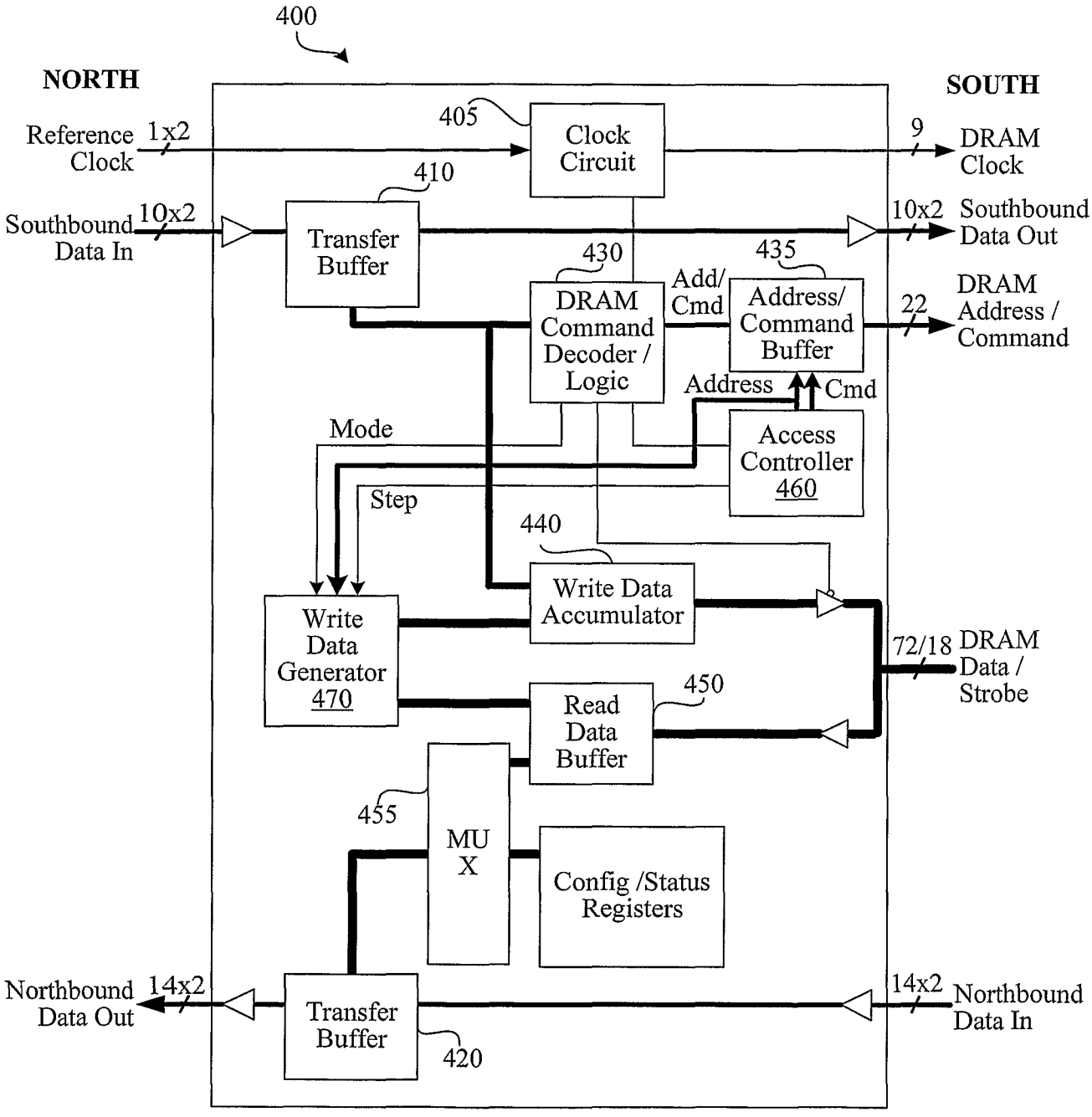
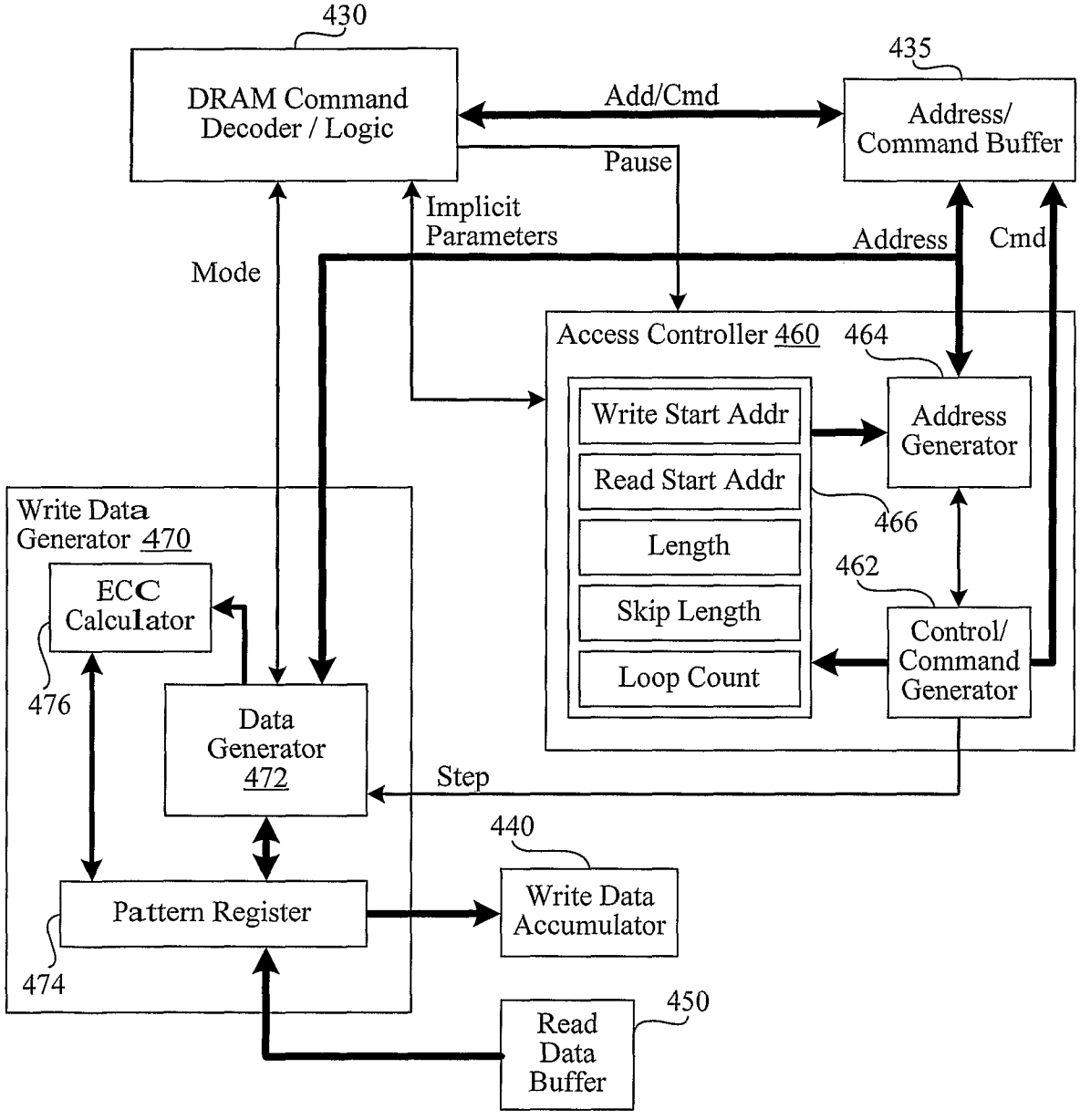

400
NORTH
SOUTH
Reference Clock
1x2
405
Clock Circuit
9
DRAM Clock
410
Southbound Data In
10x2
Transfer Buffer
10x2
Southbound Data Out
430
435
DRAM Command Decoder / Logic
Add/ Cmd
Address/ Command Buffer
22
DRAM Address / Command
Address
Cmd
Mode
Access Controller 460
Step
440
Write Data Accumulator
Write Data Generator 470
72/18
DRAM Data / Strobe
450
Read Data Buffer
455
MU X
Config /Status Registers
Northbound Data Out
14x2
Transfer Buffer
420
14x2
Northbound Data In

Fig. 5


430
DRAM Command Decoder / Logic
435
Address/ Command Buffer
Add/Cmd
Pause
Implicit Parameters
Address
Cmd
Mode
Access Controller 460
464
Write Start Addr
Read Start Addr
Length
Skip Length
Loop Count
Address Generator
466
462
Control/ Command Generator
Write Data Generator 470
ECC Calculator
476
Data Generator 472
Step
440
Write Data Accumulator
Pattern Register
474
450
Read Data Buffer