FIG. 1
Prior Art

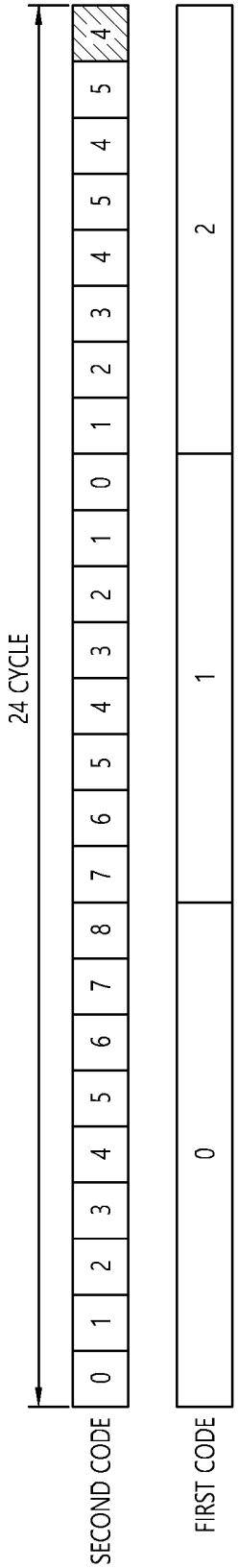


FIG. 2

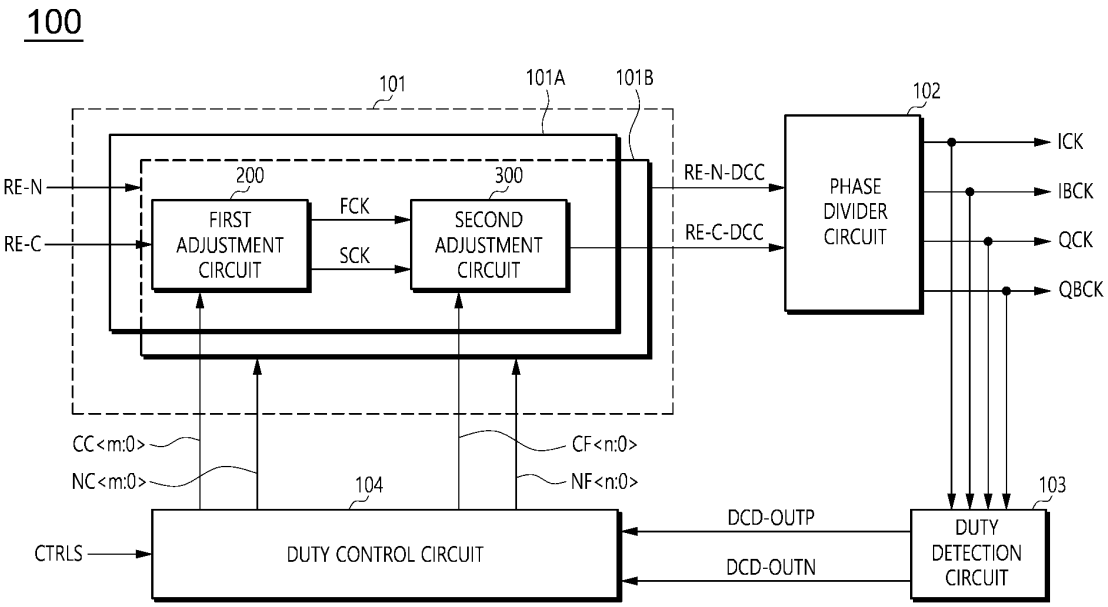

100
101
101A
101B
102
RE-N
RE-C
200
FIRST ADJUSTMENT CIRCUIT
FCK
SCK
300
SECOND ADJUSTMENT CIRCUIT
RE-N-DCC
RE-C-DCC
PHASE DIVIDER CIRCUIT
ICK
IBCK
QCK
QBCK
CC<m:0>
NC<m:0>
104
CF<n:0>
NF<n:0>
103
DCD-OUTP
DCD-OUTN
DUTY DETECTION CIRCUIT
CTRLS
DUTY CONTROL CIRCUIT

FIG. 3

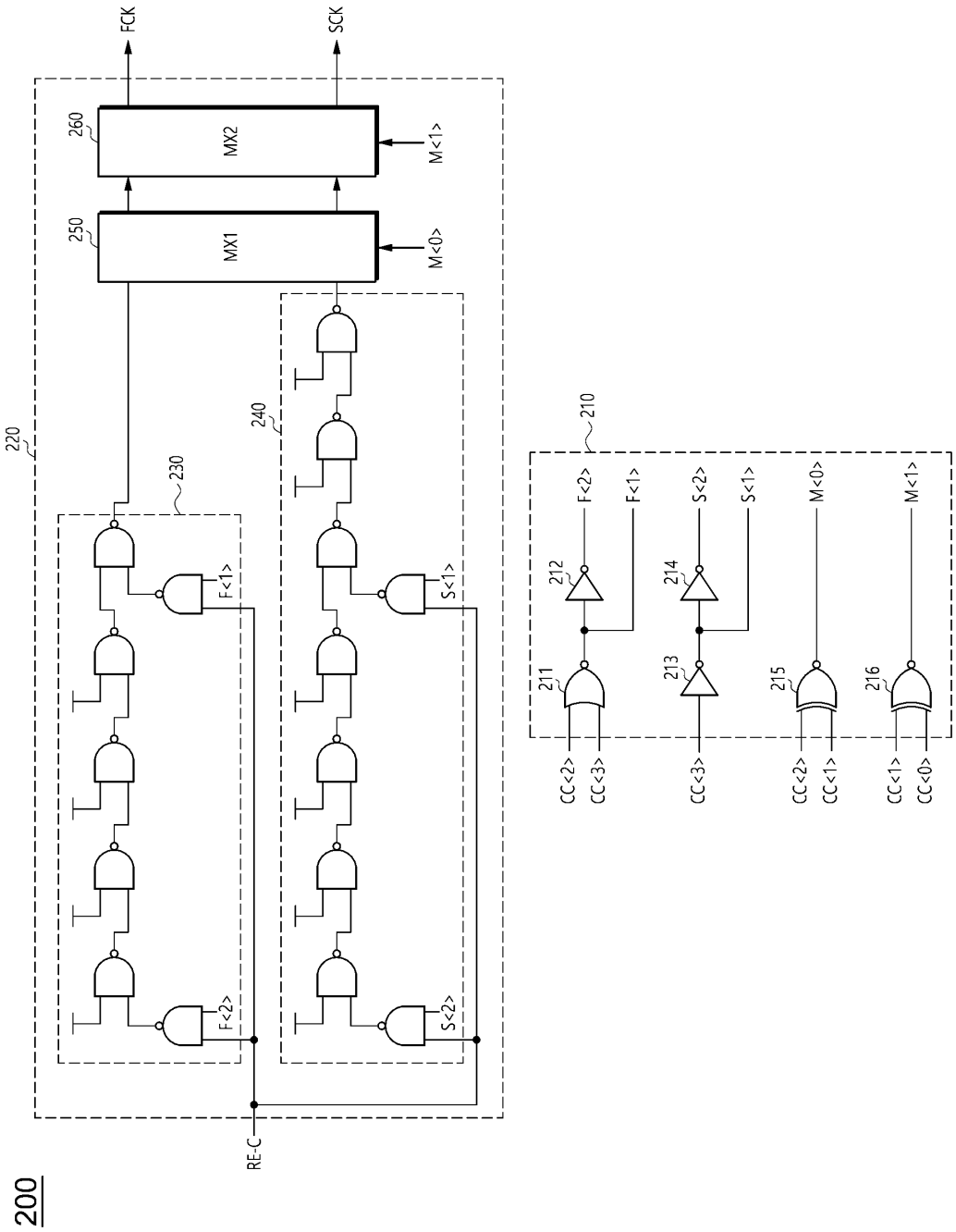

200
220
FCK
SCK
260
MX2
M<1>
250
MX1
M<0>
230
240
F<1>
F<2>
S<1>
S<2>
RE-C
210
211
212
213
214
215
216
F<2>
F<1>
S<2>
S<1>
M<0>
M<1>
CC<2>
CC<3>
CC<3>
CC<2>
CC<1>
CC<1>
CC<0>

FIG. 4

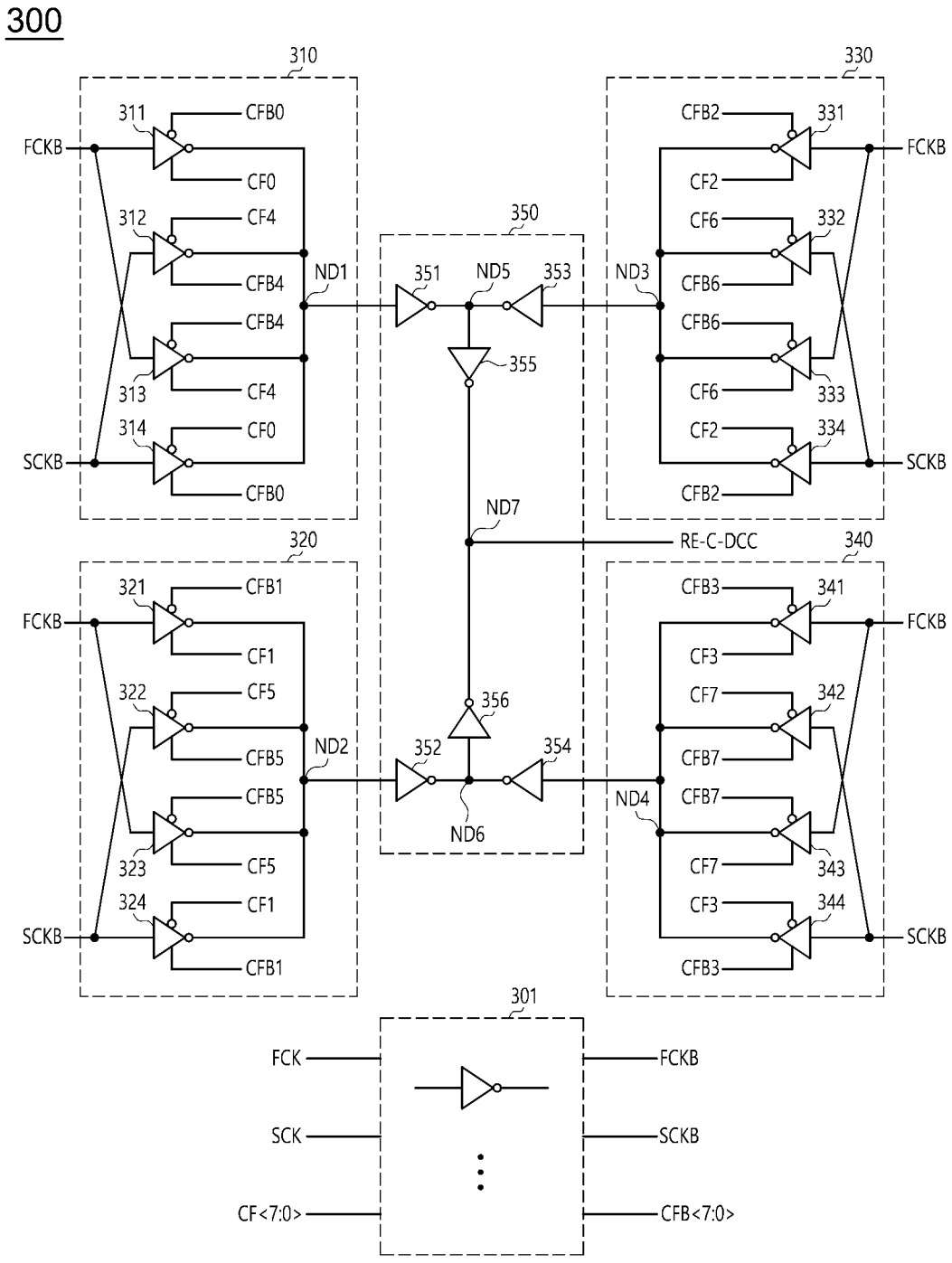

300
310
311
CFB0
FCKB
CF0
312
CF4
CFB4
ND1
CFB4
313
CF4
314
CF0
SCKB
CFB0
350
351
ND5
353
355
ND7
356
352
354
ND6
330
CFB2
331
FCKB
CF2
CF6
332
CFB6
ND3
CFB6
CF6
333
CF2
334
SCKB
CFB2
RE-C-DCC
320
321
CFB1
FCKB
CF1
322
CF5
CFB5
ND2
CFB5
323
CF5
324
CF1
SCKB
CFB1
340
CFB3
341
FCKB
CF3
CF7
342
CFB7
ND4
CFB7
CF7
343
CF3
344
SCKB
CFB3
301
FCK
FCKB
SCK
SCKB
CF<7:0>
CFB<7:0>

FIG. 5

CF<7:0>	CF<7>	CF<6>	CF<5>	CF<4>	CF<3>	CF<2>	CF<1>	CF<0>
0	1	1	1	1	1	1	1	1
1	1	1	1	1	1	1	1	0
2	1	1	1	1	1	1	0	0
3	1	1	1	1	1	0	0	0
4	1	1	1	1	0	0	0	0
5	1	1	1	0	0	0	0	0
6	1	1	0	0	0	0	0	0
7	1	0	0	0	0	0	0	0
8	0	0	0	0	0	0	0	0

FIG. 6

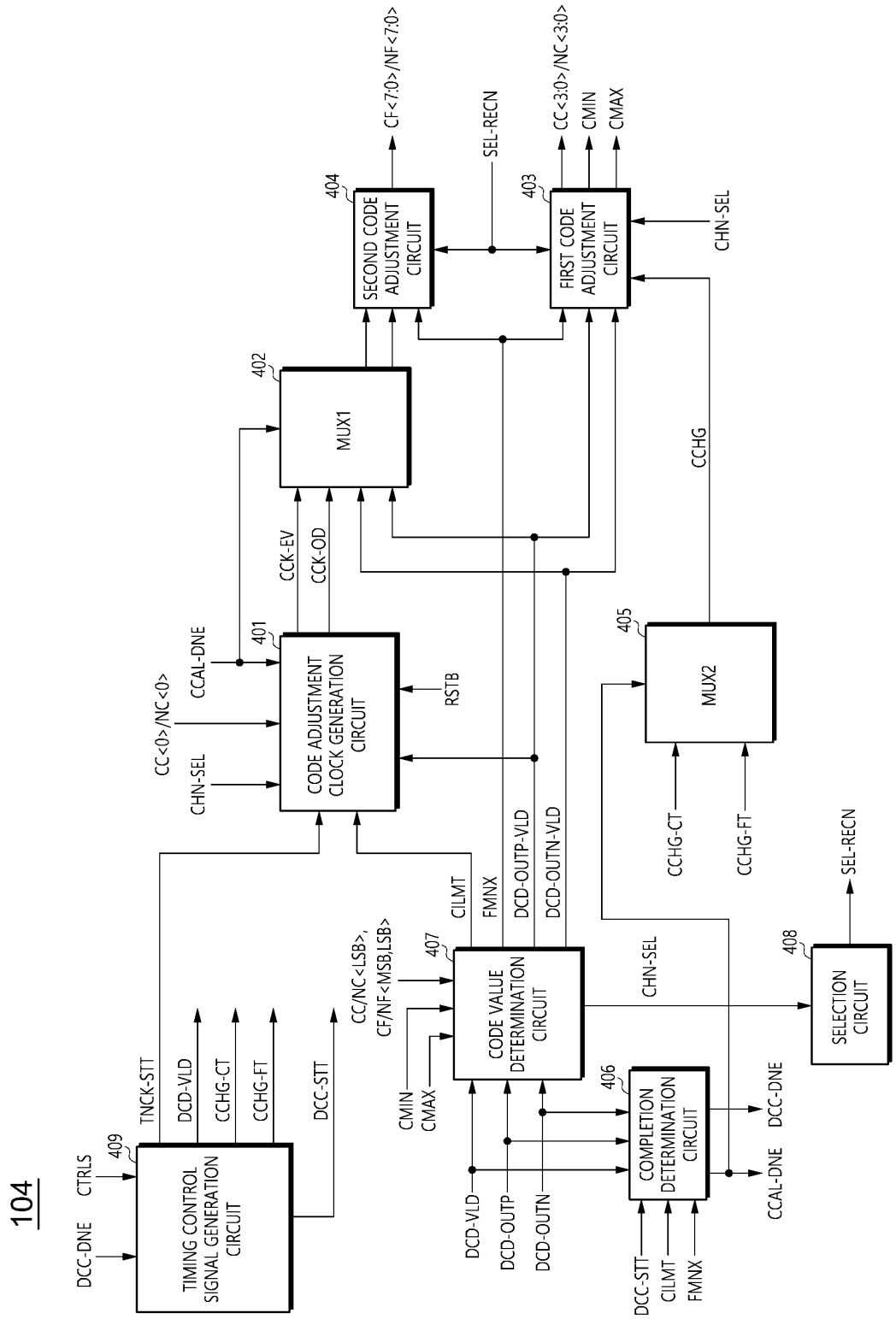

104
TIMING CONTROL SIGNAL GENERATION CIRCUIT
409
DCC-DNE
CTRLS
TNCK-STT
DCD-VLD
CCHG-CT
CCHG-FT
DCC-STT
CODE ADJUSTMENT CLOCK GENERATION CIRCUIT
401
CCAL-DNE
CC<0>/NC<0>
CHN-SEL
RSTB
CCK-EV
CCK-OD
MUX1
402
SECOND CODE ADJUSTMENT CIRCUIT
404
FIRST CODE ADJUSTMENT CIRCUIT
403
CF<7:0>/NF<7:0>
SEL-RECN
CC<3:0>/NC<3:0>
CMIN
CMAX
CHN-SEL
CCHG
MUX2
405
CCHG-CT
CCHG-FT
CODE VALUE DETERMINATION CIRCUIT
407
CC/NC<LSB>,
CF/NF<MSB:LSB>
CMIN
CMAX
CILMT
FMNX
DCD-OUTP-VLD
DCD-OUTN-VLD
DCD-VLD
DCD-OUTP
DCD-OUTN
CHN-SEL
COMPLETION DETERMINATION CIRCUIT
406
DCC-STT
CILMT
FMNX
DCC-DNE
CCAL-DNE
SELECTION CIRCUIT
408
SEL-RECN

FIG. 7

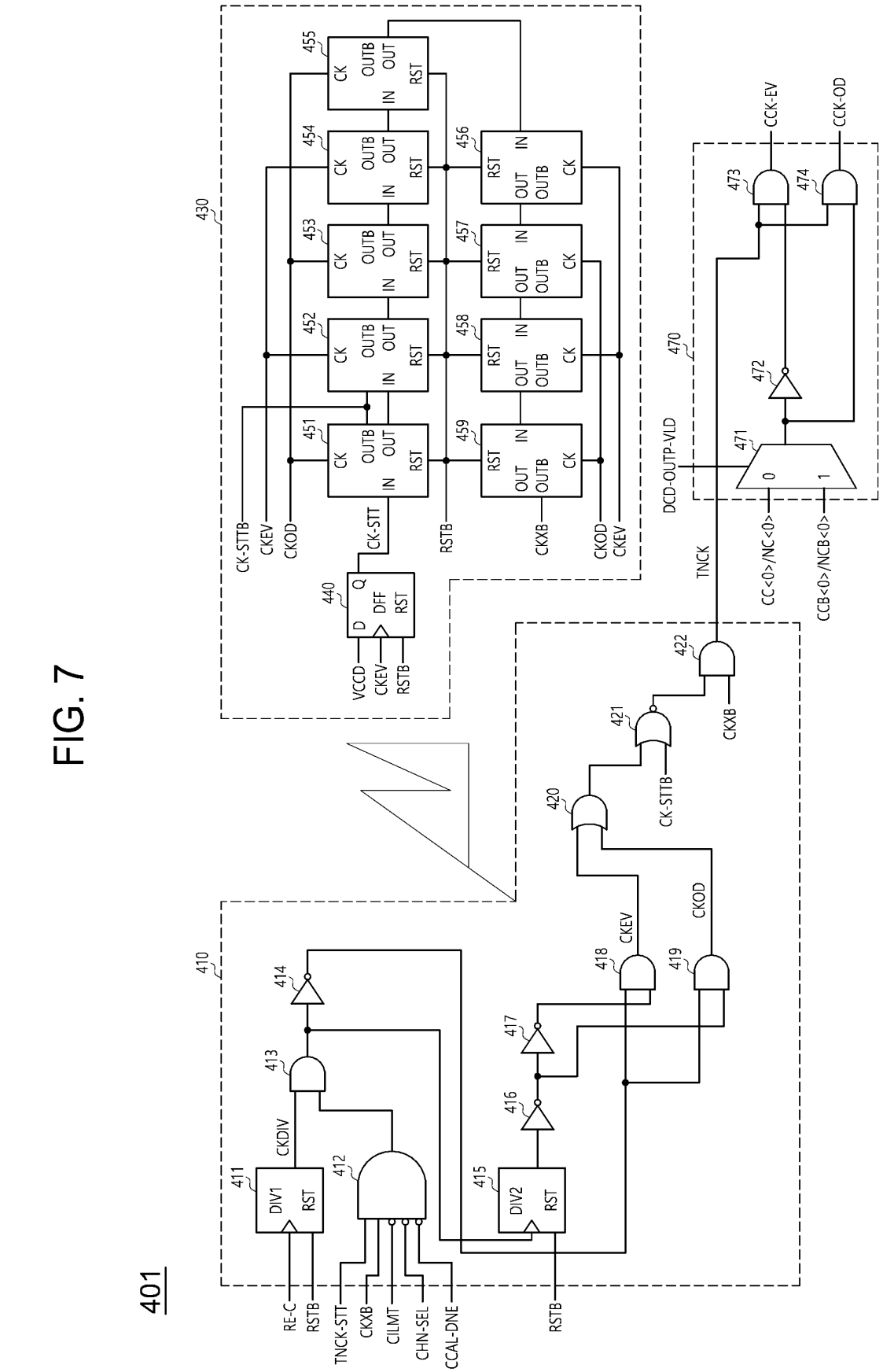

401
410
411
DIV1
RST
CKDIV
412
413
414
415
DIV2
RST
416
417
418
CKEV
419
CKOD
420
421
422
CKXB
CK-STTB
TNCK
RE-C
RSTB
TNCK-STT
CKXB
CILMT
CHN-SEL
CCAL-DNE
RSTB
430
440
D
Q
DFF
RST
VCCD
CKEV
RSTB
CK-STT
451
452
453
454
455
456
457
458
459
CK
OUTB
OUT
IN
RST
CK-STTB
CKEV
CKOD
RSTB
CKXB
CKOD
CKEV
470
471
472
473
474
0
1
DCD-OUTP-VLD
CC<0>/NC<0>
CCB<0>/NCB<0>
CCK-EV
CCK-OD

FIG. 8

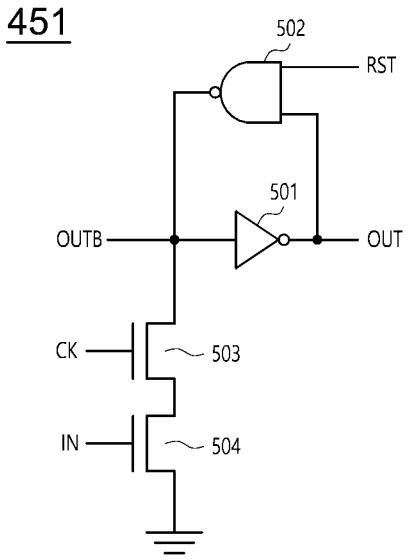


FIG. 9

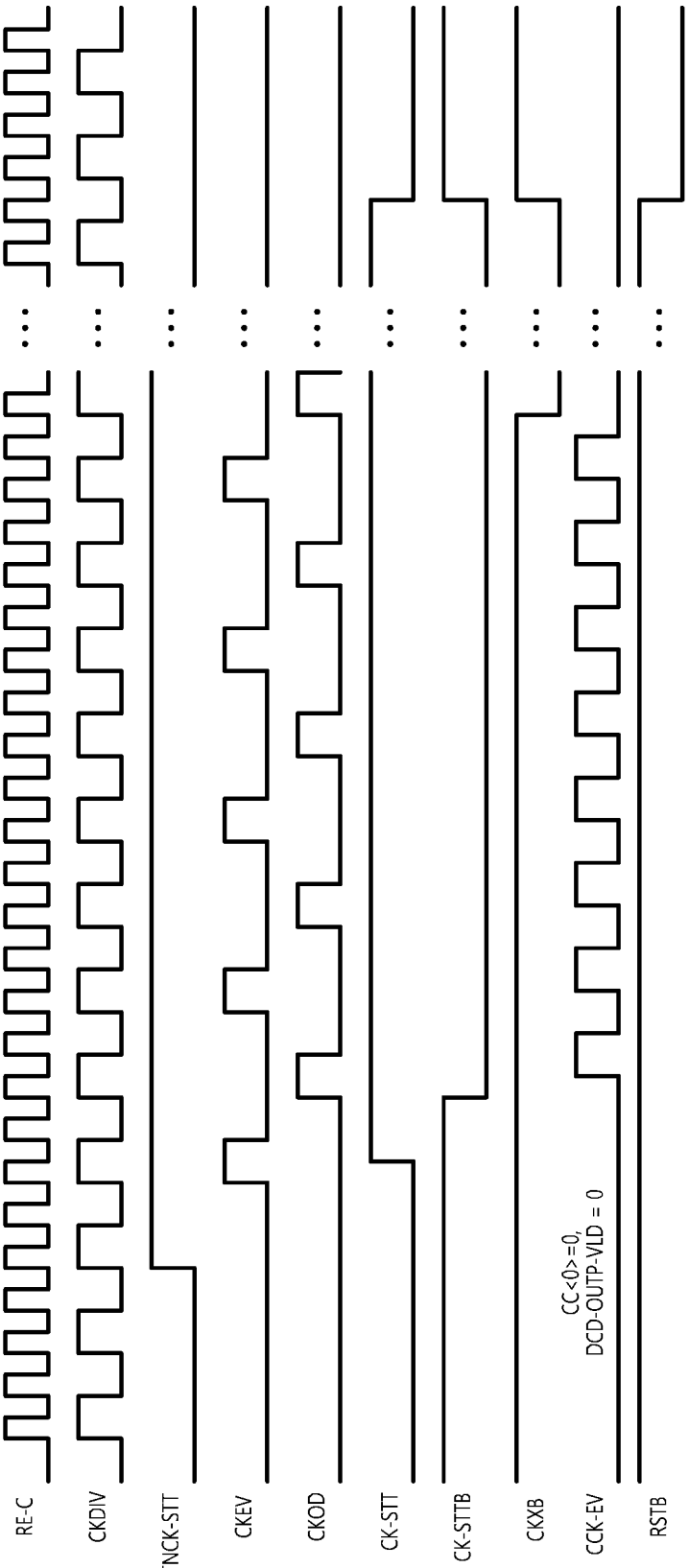

RE-C
CKDIV
TNCK-STT
CKEV
CKOD
CK-STT
CK-STTB
CKXB
CCK-EV
RSTB
CC<0>=0,
DCD-OUTP-VLD = 0

FIG. 10

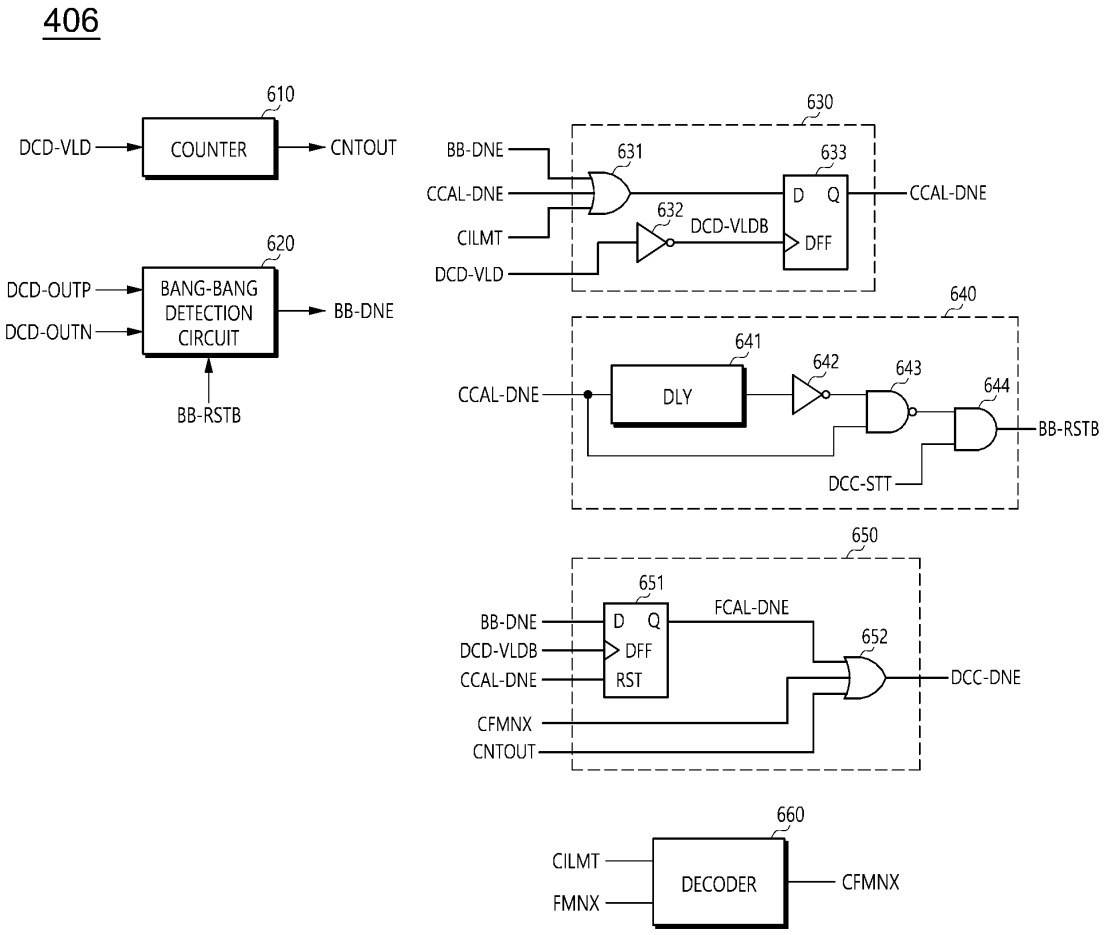

406
610
DCD-VLD
COUNTER
CNTOUT
620
DCD-OUTP
DCD-OUTN
BANG-BANG DETECTION CIRCUIT
BB-DNE
BB-RSTB
630
BB-DNE
631
CCAL-DNE
CILMT
632
DCD-VLD
633
D Q
DCD-VLDB
DFF
CCAL-DNE
640
CCAL-DNE
641
DLY
642
643
644
BB-RSTB
DCC-STT
650
651
BB-DNE
DCD-VLDB
CCAL-DNE
D Q
DFF
RST
FCAL-DNE
652
DCC-DNE
CFMNX
CNTOUT
660
CILMT
FMNX
DECODER
CFMNX

FIG. 11

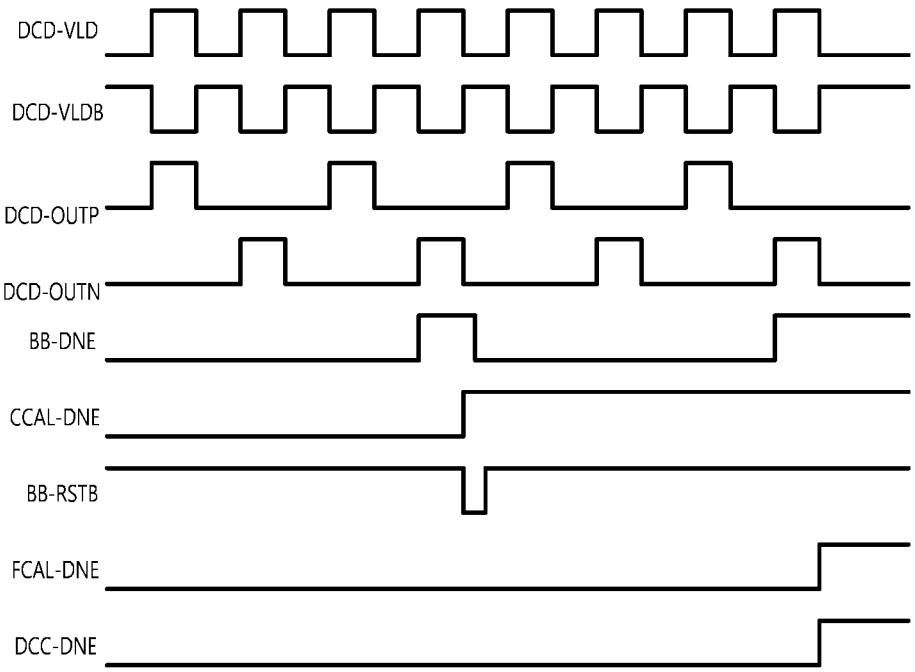

DCD-VLD
DCD-VLDB
DCD-OUTP
DCD-OUTN
BB-DNE
CCAL-DNE
BB-RSTB
FCAL-DNE
DCC-DNE

FIG. 12

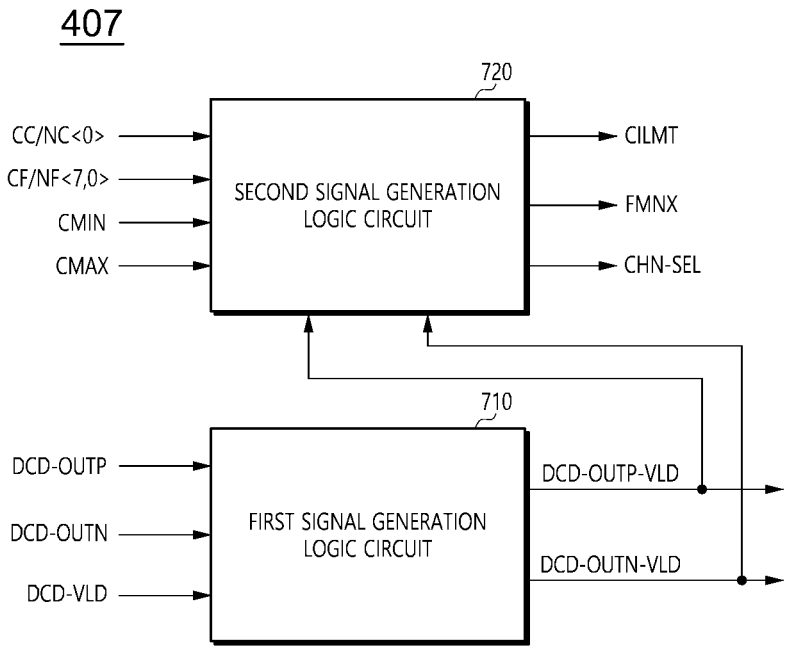

407
720
CC/NC<0>
CF/NF<7,0>
CMIN
CMAX
SECOND SIGNAL GENERATION LOGIC CIRCUIT
CILMT
FMNX
CHN-SEL
710
DCD-OUTP
DCD-OUTN
DCD-VLD
FIRST SIGNAL GENERATION LOGIC CIRCUIT
DCD-OUTP-VLD
DCD-OUTN-VLD

FIG. 13

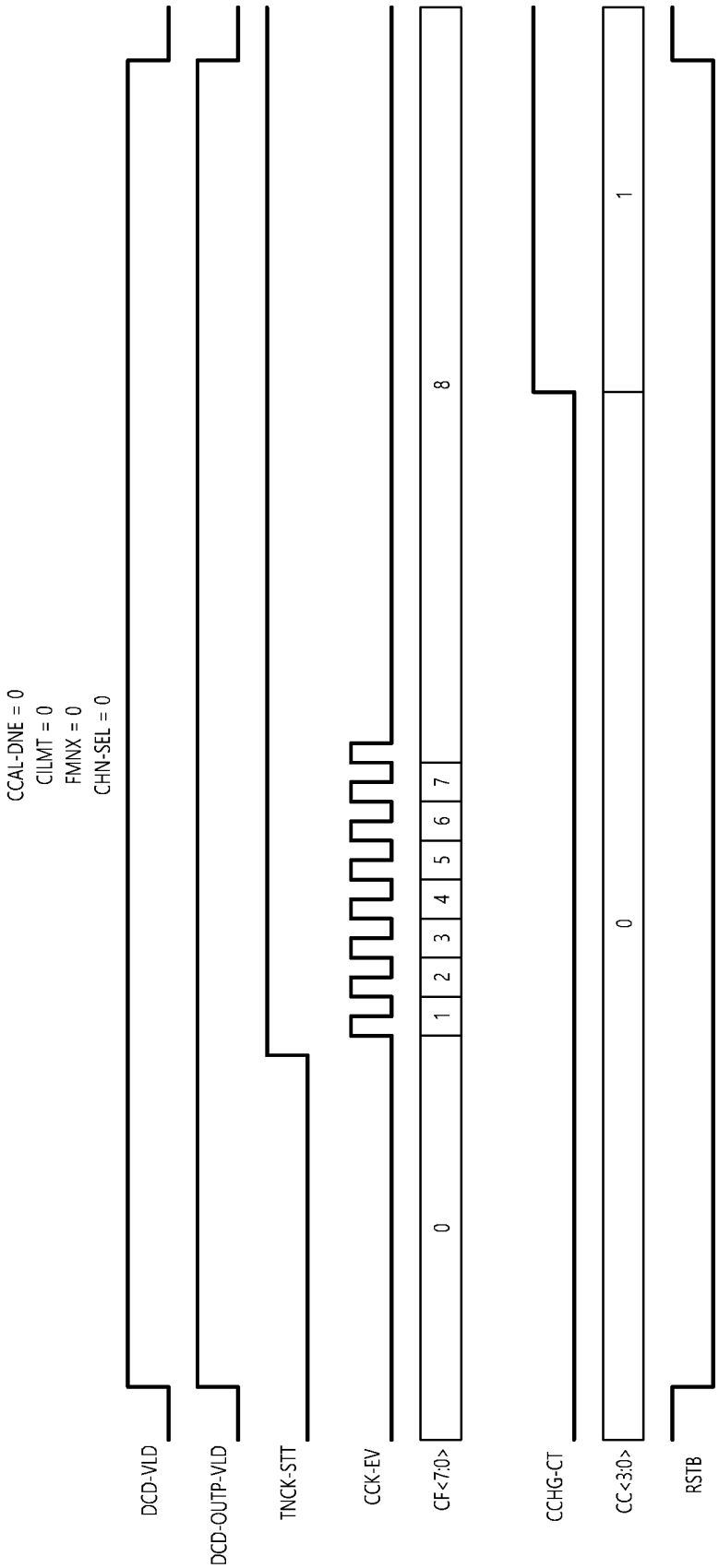

CCAL-DNE = 0
CILMT = 0
FMNX = 0
CHN-SEL = 0
DCD-VLD
DCD-OUTP-VLD
TNCK-STT
CCK-EV
CF<7:0>
0
1
2
3
4
5
6
7
8
CCHG-CT
CC<3:0>
0
1
RSTB

FIG. 14

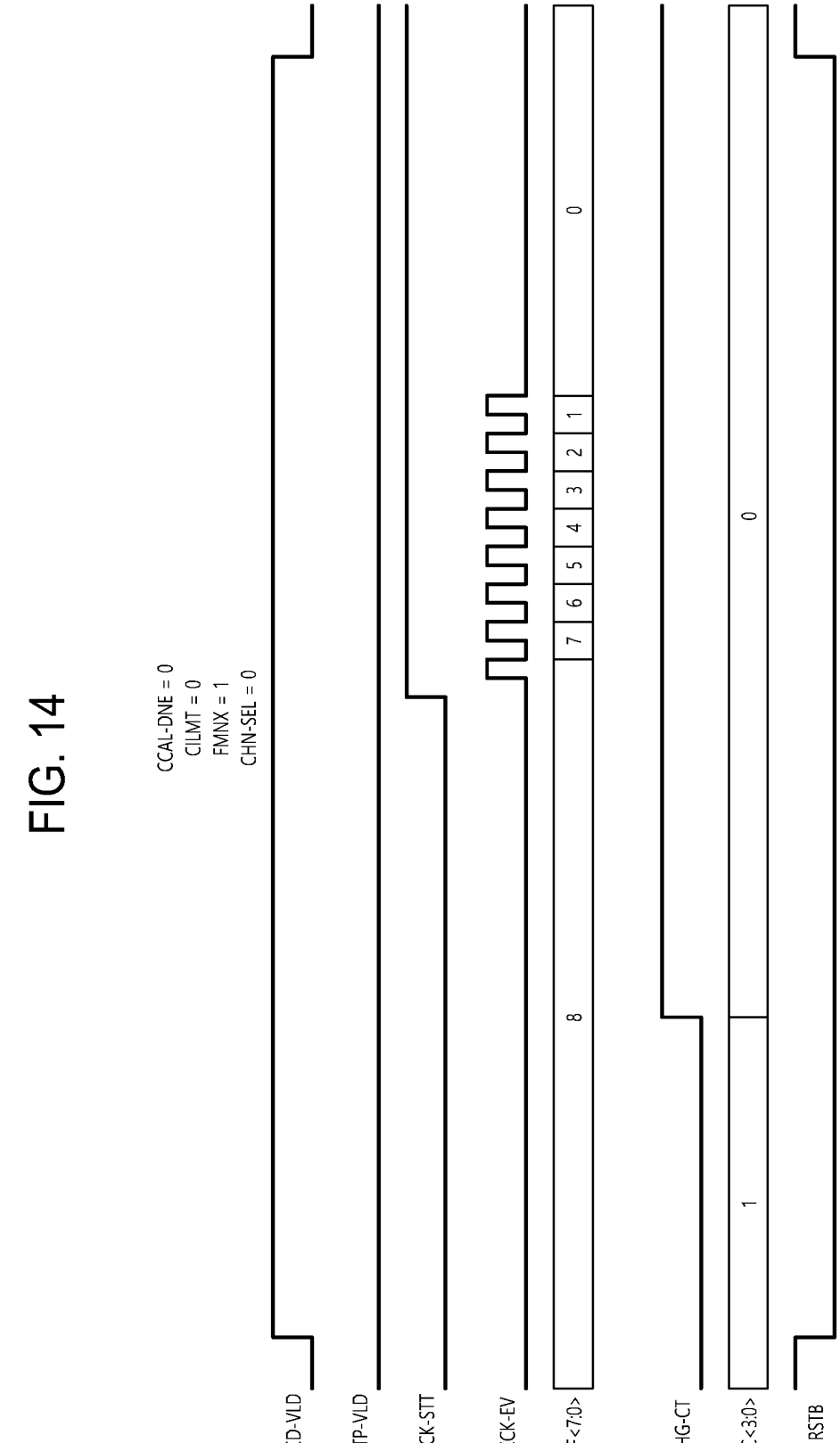

CCAL-DNE = 0
CILMT = 0
FMNX = 1
CHN-SEL = 0
DCD-VLD
DCD-OUTP-VLD
TNCK-STT
CCK-EV
CF<7:0>
8
7
6
5
4
3
2
1
0
CCHG-CT
CC<3:0>
1
0
RSTB

FIG. 15

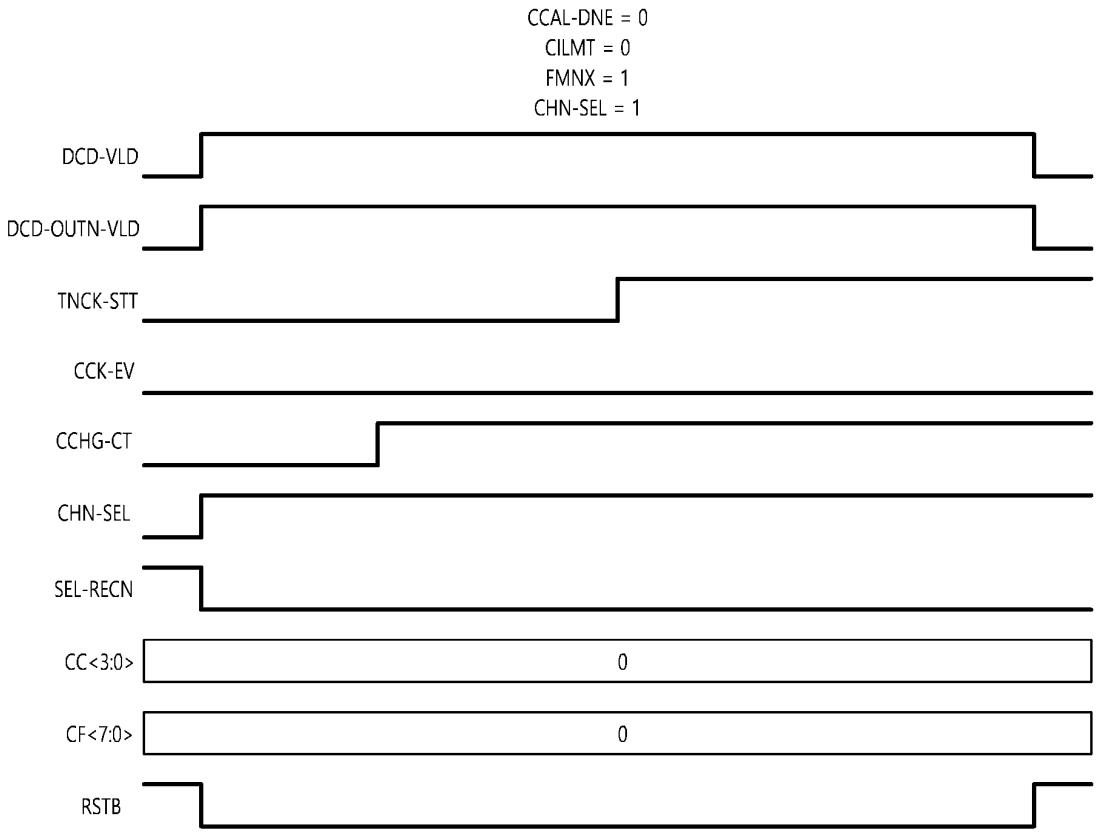

CCAL-DNE = 0
CILMT = 0
FMNX = 1
CHN-SEL = 1
DCD-VLD
DCD-OUTN-VLD
TNCK-STT
CCK-EV
CCHG-CT
CHN-SEL
SEL-RECN
CC<3:0>
0
CF<7:0>
0
RSTB

FIG. 16

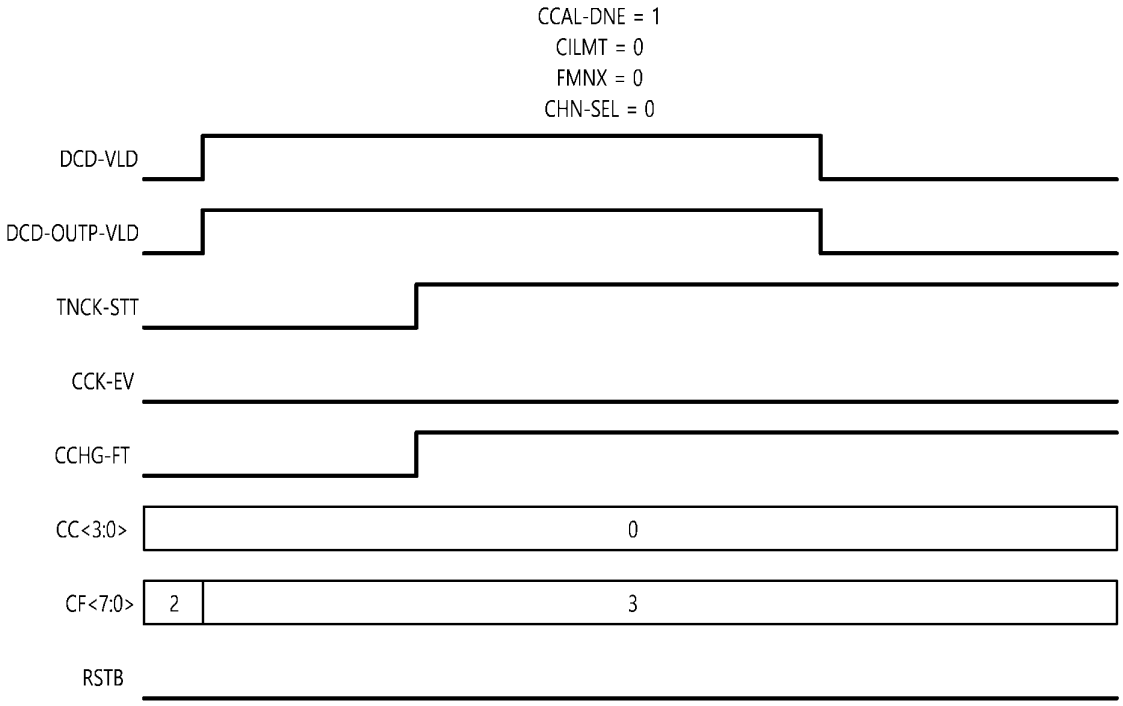

CCAL-DNE = 1
CILMT = 0
FMNX = 0
CHN-SEL = 0
DCD-VLD
DCD-OUTP-VLD
TNCK-STT
CCK-EV
CCHG-FT
CC<3:0>
0
CF<7:0>
2
3
RSTB

FIG. 17

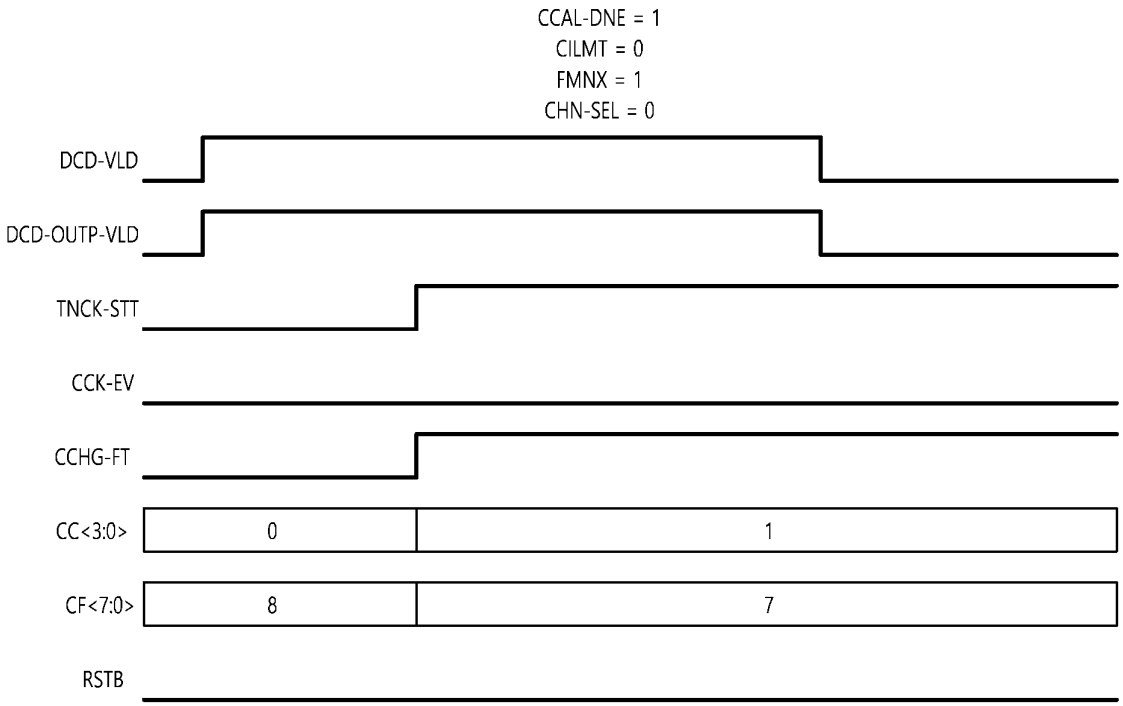

CCAL-DNE = 1
CILMT = 0
FMNX = 1
CHN-SEL = 0
DCD-VLD
DCD-OUTP-VLD
TNCK-STT
CCK-EV
CCHG-FT
CC<3:0>
0
1
CF<7:0>
8
7
RSTB

FIG. 18

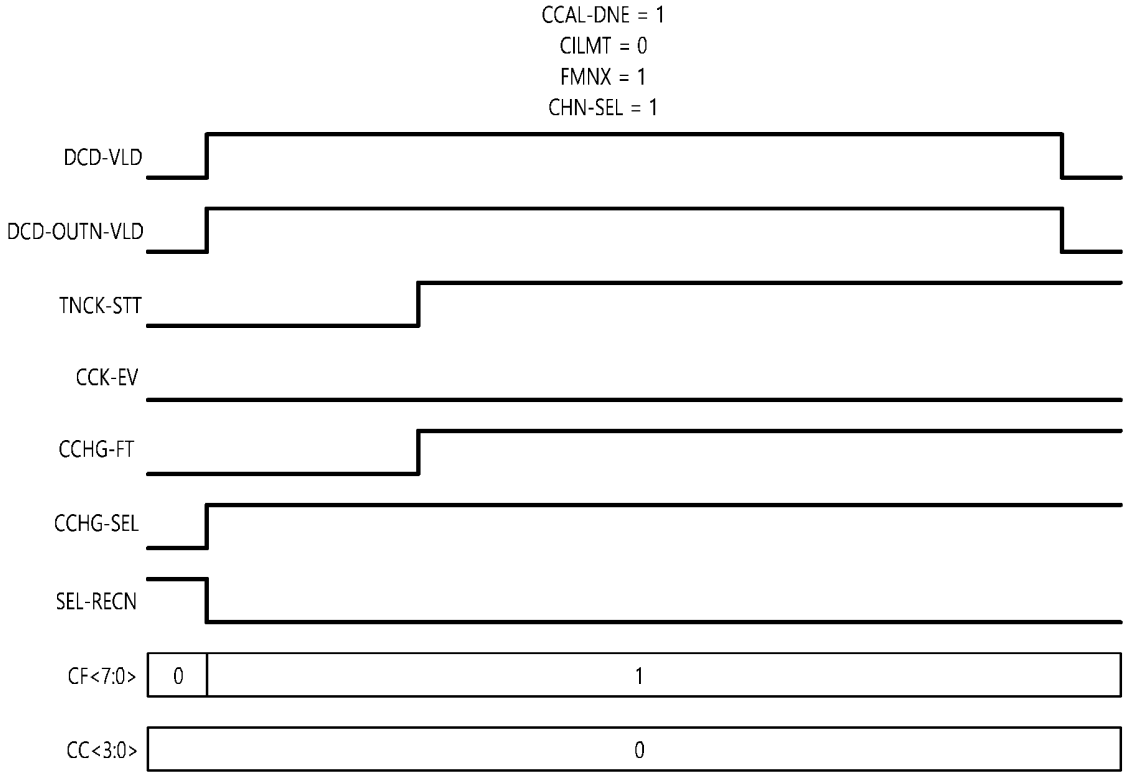
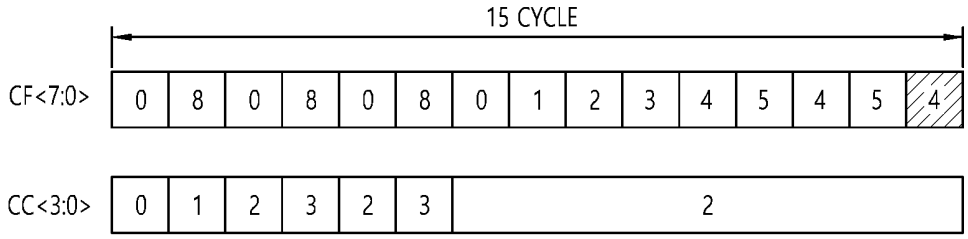

CCAL-DNE = 1
CILMT = 0
FMNX = 1
CHN-SEL = 1
DCD-VLD
DCD-OUTN-VLD
TNCK-STT
CCK-EV
CCHG-FT
CCHG-SEL
SEL-RECN
CF<7:0>
0
1
CC<3:0>
0

FIG. 19


15 CYCLE
CF<7:0>
0 8 0 8 0 8 0 1 2 3 4 5 4 5 4
CC<3:0>
0 1 2 3 2 3 2