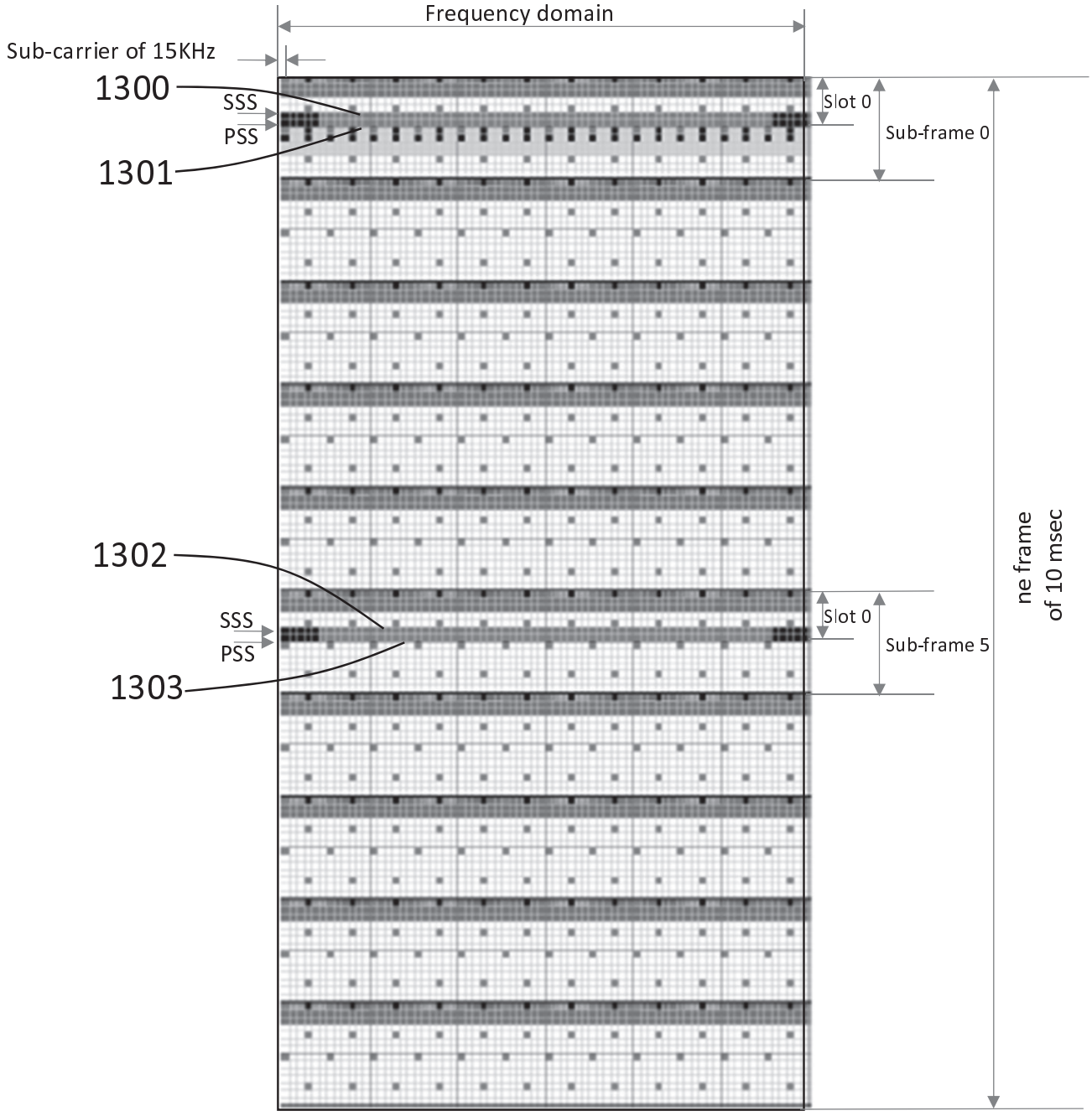


Fig. 4

Prior Art

Fig. 6

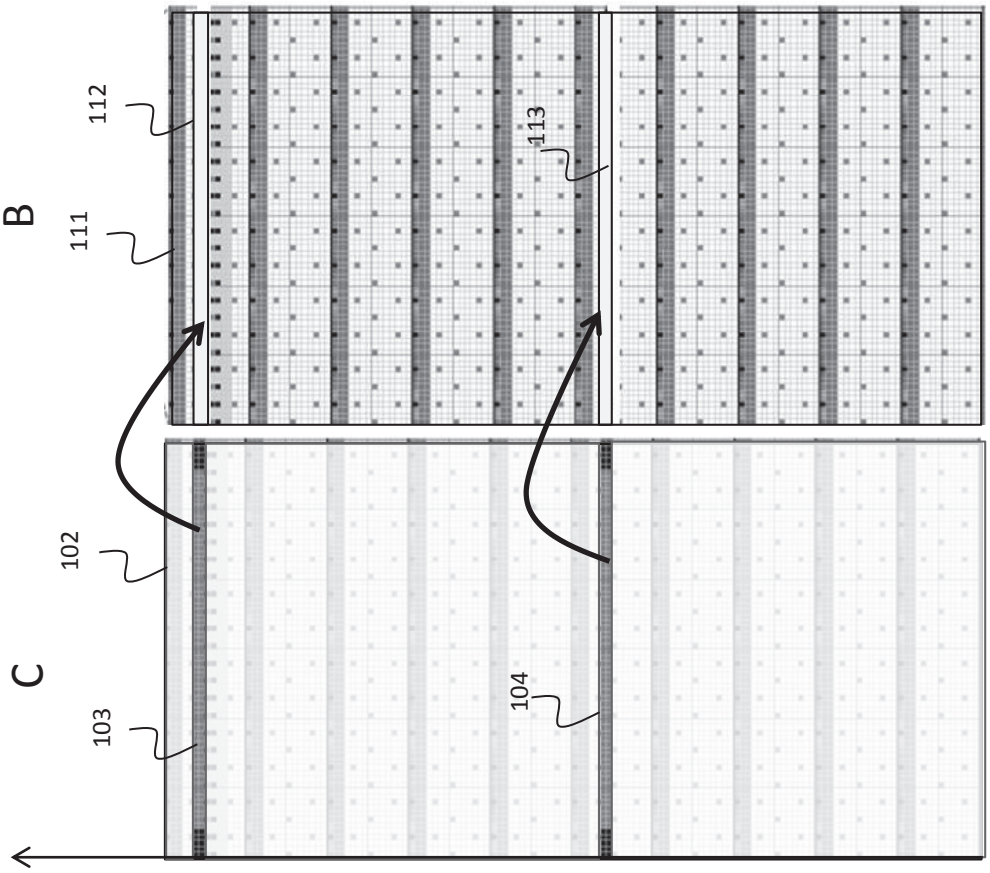


Fig. 5

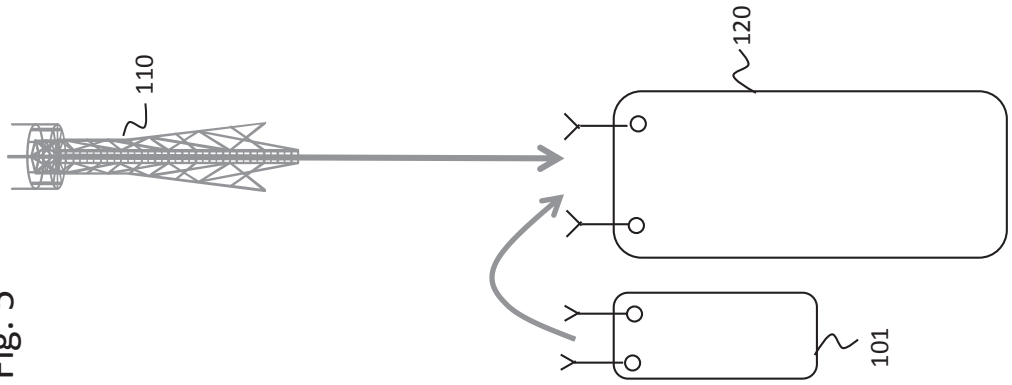


Fig. 8-A

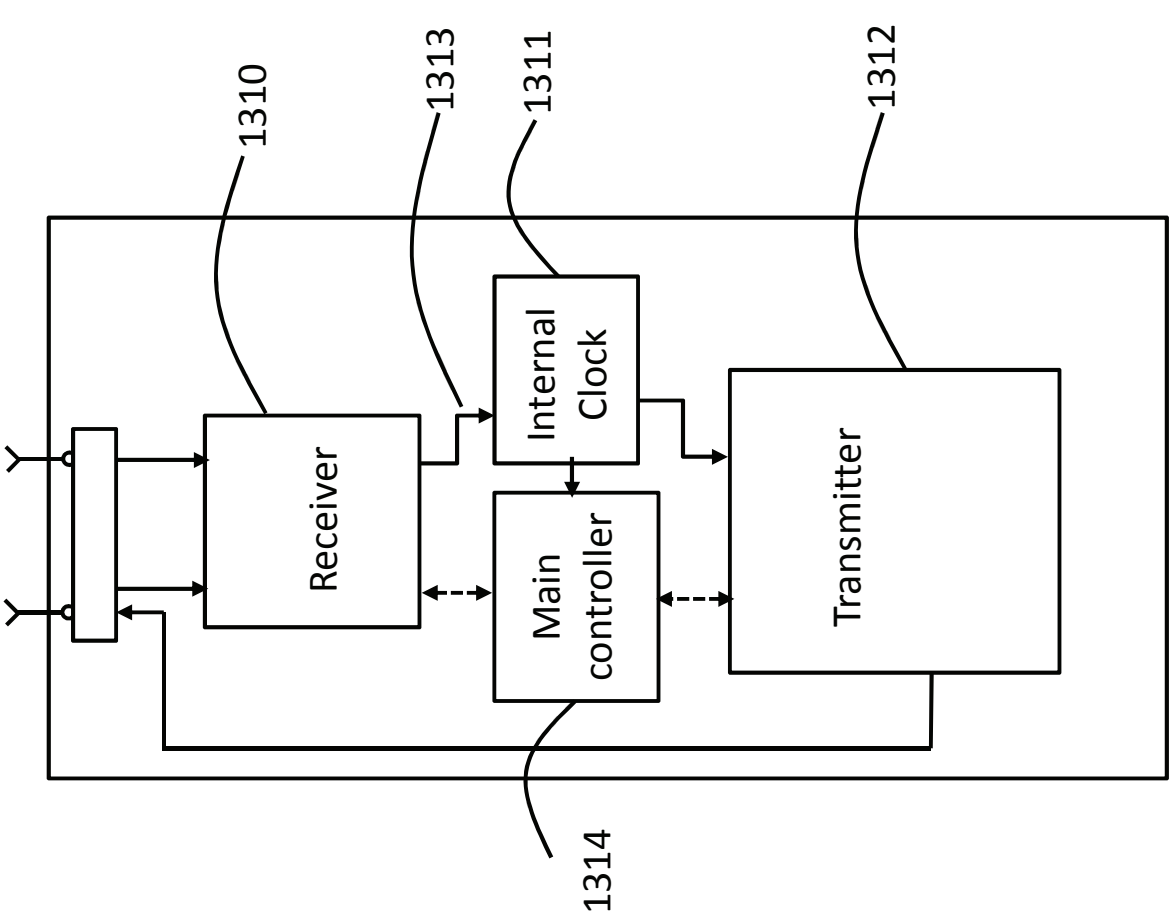

1310
1313
1311
1312
Receiver
Internal Clock
Transmitter
Main controller
1314

Fig. 8-B

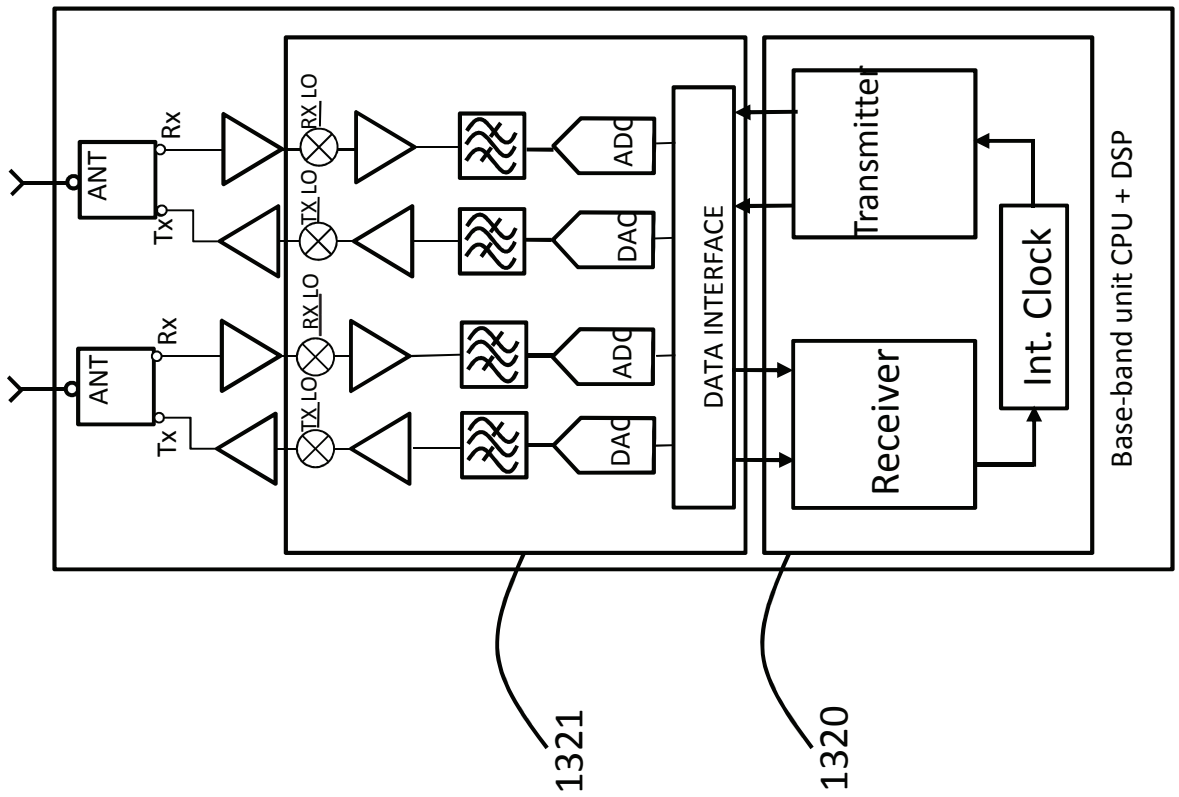

ANT
Rx
Tx
RX LO
TX LO
ADC
DAC
DATA INTERFACE
Transmitter
Receiver
Int. Clock
Base-band unit CPU + DSP
1321
1320

Fig. 10-A

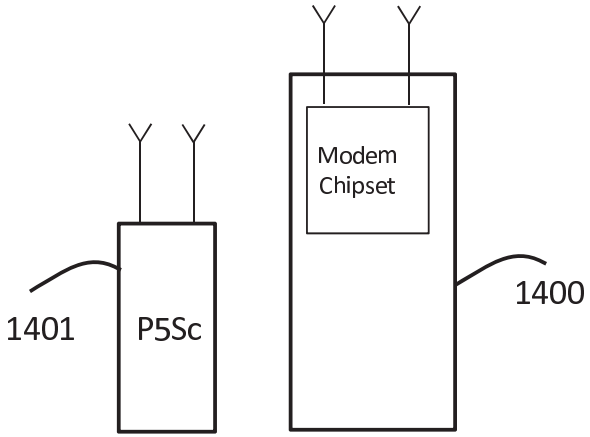


Fig. 10-B

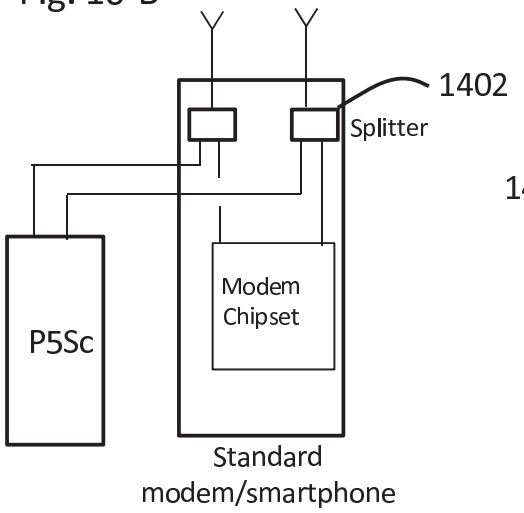


Fig. 10-C

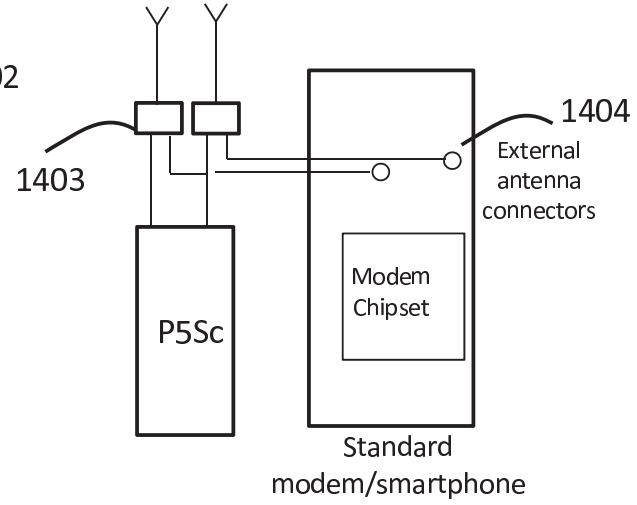


Fig. 11-A

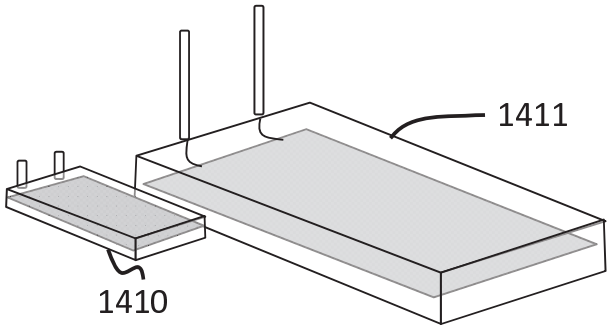


Fig. 11-B

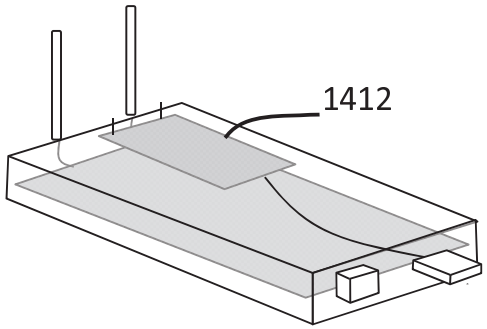


Fig. 11-C

