further shown formed between the terminals 206 and the die pad 204. The dielectric material 208 rigidly couples the terminals 206 and the die pad 204 in place to form a substrate 209.

The terminals 206 are shown having a top 210. The top 210 of the terminals 206 can include a plateau 212 and also include depressions 214 extending from the plateau 212 to a maximum width 216 of the terminals 206. The dielectric material 208 is in direct contact with a peripheral portion 217 at the plateau 212 of the top 210 of the terminals 206 from the plateau 212 to the maximum width 216 of the terminals 206 and fills in the depressions 214.

Below the maximum width 216 of the terminals 206 is a bottom portion 218 extending down from the maximum width 216 of the terminals 206. The bottom portion 218 can include a dent 220 extending down from the maximum width 216 to a base 222 of the bottom portion 218. The base 222 is depicted as planar or flat. The bottom portion 218 is depicted as slightly larger or taller than the top 210 providing increased standoff distance and clearance.

Covering some of the bottom portion 218 is a contact layer 226. The contact layer 226 is defined as a material on the surface of the terminals 206 and form electrical connections with other components. The contact layer 226 can be a solder paste, a layer containing tin or lead, or a conductive high temperature polymer. The contact layer 226 can cover some of the bottom portion 218 of the terminals 206 with a conformal layer with a uniform thickness.

The contact layer 226 is shown covering the bottom portion 218 surface of the terminals 206 with an even and conformal film along the base 222. The contact layer 226 is further depicted covering the underside of the die pad 204.

It has been discovered that the contact layer 226 formed on the base 222 increases solder coverage. Increasing solder coverage with the terminals 206 and the die pad 204 increases board level reliability and performance. The contact layer 226 of the present invention further can be formed by a printing process thereby increasing manufacturing precision without additional costs.

The top 210 of the terminals 206 are shown having the dielectric material 208 formed thereon. The dielectric material 208 can include gaps 228 on the top 210 that expose portions of the plateau 212 from between the dielectric material 208. The gaps 228 are defined as an opening or absence of the dielectric material 208 that exposes portions of the plateau 212 from between the dielectric material 208. The dielectric material 208 can be designed to support the terminals 206 during process and to increase structural rigidity in the integrated

What is claimed is:

1. A method of manufacture of an integrated circuit packaging system comprising:

providing a terminal having a top with a depression;

applying a dielectric material in the depression, the dielectric material having a gap formed therein and exposing a portion of the top therefrom is in direct contact with a peripheral portion at a plateau of the terminal;

forming a trace within the gap and in direct contact with the top, the trace extending laterally over an upper surface of the dielectric material; and

connecting an integrated circuit to the terminal through the trace.

2. The method as claimed in claim 1 further comprising:

providing a die pad; and

applying a contact layer below the die pad; and

wherein:

forming the trace includes forming a perimeter trace around the die pad; and

further comprising:

mounting the integrated circuit to the die pad.

3. The method as claimed in claim 1 further comprising mounting the integrated circuit above the trace extending beyond the integrated circuit.

4. The method as claimed in claim 1 wherein:

forming the trace includes forming multiple traces; and

further comprising:

mounting the integrated circuit above the multiple traces terminating at a non-uniform distance from the integrated circuit.

5. The method as claimed in claim 1 further comprising mounting the integrated circuit above the trace extending below the integrated circuit from the terminal beyond the integrated circuit.

6. A method of manufacture of an integrated circuit packaging system comprising:

providing a terminal having a top with a plateau and a depression extending from the plateau to a maximum width, the terminal further having a bottom portion with a dent extending from the maximum width to a base;

applying a contact layer directly to the base of the terminal;

forming a dielectric material in the depression and in direct contact with the plateau and extending to the maximum width, the dielectric material having a gap formed therein and exposing a portion of the plateau therefrom is in direct contact with a peripheral portion at a plateau of the terminal;

forming a trace within the gap and in direct contact with the plateau, the trace extending laterally over an upper surface of the dielectric material;

connecting an integrated circuit to the terminal through the trace; and

encapsulating the trace and the integrated circuit with an encapsulation.

7. The method as claimed in claim 6 wherein applying the contact layer includes applying the contact layer directly to a portion of the dent of the terminal near the base leaving a portion of the dent near the maximum width exposed.

8. The method as claimed in claim 6 further comprising forming a dimpled surface in the terminal centered in the base.

9. The method as claimed in claim 6 further comprising forming solder balls below the base and attached to the contact layer.

10. The method as claimed in claim 6 wherein connecting the integrated circuit to the terminal includes connecting the integrated circuit with a bond wire or with a solder ball.

~~11. An integrated circuit packaging system comprising:~~

~~a terminal having a top with a depression;~~

~~a dielectric material in the depression, the dielectric material having a gap formed therein and exposing a portion of the top therefrom;~~

~~a trace within the gap and in direct contact with the top, the trace extending laterally over an upper surface of the dielectric material; and~~

~~an integrated circuit connected to the terminal through the trace.~~

~~12. The system as claimed in claim 11 further comprising:~~

~~a die pad adjacent to the terminal;~~

~~a contact layer below the die pad;~~

~~a perimeter trace around the die pad; and~~

~~wherein:~~

~~the integrated circuit is attached to the die pad.~~

13. The system as claimed in claim 11 wherein the trace extends beyond the integrated circuit from below the integrated circuit.

14. The system as claimed in claim 11 further comprising multiple traces terminating at a non-uniform distance from the integrated circuit.

15. The system as claimed in claim 11 wherein the trace extends below the integrated circuit from the terminal beyond the integrated circuit.

16. A system as claimed in claim 11 wherein:

the terminal has a maximum width and has a bottom portion with a dent extending from the maximum width to a base;

the top of the terminal has a plateau and the depression extends from the plateau to the maximum width;

the dielectric material is in direct contact with the plateau and extends to the maximum width;

the gap exposes a portion of the plateau therefrom;

trace is in direct contact with the plateau; and

further comprising:

a contact layer formed directly to the base of the terminal; and

an encapsulation encapsulating the trace and the integrated circuit.

17. The system as claimed in claim 16 wherein the contact layer is formed directly to a portion of the dent of the terminal near the base leaving a portion of the dent near the maximum width exposed.

18. The system as claimed in claim 16 further comprising a dimpled surface formed in the terminal centered in the base.

19. The system as claimed in claim 16 further comprising solder balls below the base and attached to the contact layer.

20. The system as claimed in claim 16 wherein the integrated circuit is connected to the terminal with a bond wire or with a solder ball.