



RASTER DISTORTION AVOIDANCE ARRANGEMENT

The invention relates to a deflection circuit of a video display apparatus.

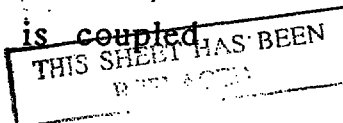
5 So-called "organ pipes" distortion may appear in the left-hand side of a display screen of a cathode ray tube (CRT) as brightness modulated, vertical stripes. This type of distortion may result from horizontal deflection current ringing that produces a beam velocity modulation visible as vertical stripes. The deflection current ringing may be caused by a stray
10 capacitance, associated with windings of a horizontal deflection winding, immediately after a retrace voltage pulse that is developed across the horizontal deflection winding ceases.

The high rate of change of a retrace voltage pulse that is developed across the deflection winding, during the second half
15 of horizontal retrace, produces a capacitive current pulse flowing in the horizontal deflection winding. This capacitive current pulse ends abruptly at the end of horizontal retrace, when the rate of change of the retrace voltage pulse becomes zero and may produce the deflection current ringing.

20 Organ pipes distortions may last, for example, $5\mu\text{s}$ after a beginning time of the trace interval. Typically, the effect of organ pipes distortion is not visible to the user due to the usage of a high degree of overscan. However, it may be desirable to operate modern full square CRTs with only a low degree of
25 overscan.

Color television receivers or display monitors operating at higher scan rates than, for example, $f_H = 15,625$ Hz, may be even more susceptible to organ pipes distortions. The ringing depends upon the horizontal winding stray capacitance and the retrace pulse voltage width and amplitude and not upon
30 the deflection frequency. When a higher deflection frequency is used, the trace interval is shorter. Therefore, the ringing interval is proportionally greater relative to the trace interval. It may be desirable to suppress the deflection current ringing during the
35 beginning of horizontal trace without using a high degree of overscan.

In a circuit embodying an aspect of the invention, a linearity correcting coil or another suitable inductor is coupled





between a deflection switch and the horizontal deflection winding. A current pulse is injected at a junction terminal between the horizontal deflection winding and the linearity correcting coil, during the end of retrace and at the beginning of trace. The
5 injected current is divided between the linearity correcting coil and the horizontal deflection winding. The injected current causes a reduction in the current of the linearity correcting coil that is coupled to the horizontal deflection winding in a manner to compensate for the sudden decrease in the capacitive current in
10 the stray capacitance. In this way, the deflection current ringing is prevented.

In a video display, embodying an aspect of the invention, an inductance is coupled in a current path of a deflection current between a deflection winding and a first
15 switching arrangement. A pulse of current is generated and coupled to the inductance and to the deflection winding via a junction terminal that is in the current path between the inductance and the deflection winding. The pulse of current has both a beginning time and an end time in a vicinity of an instant
20 when a retrace pulse voltage produced in the deflection winding ceases. The pulse of current produces a decrease in a current that flows in the inductance, during a beginning portion of a trace interval.

FIGURE 1 illustrates a horizontal deflection circuit with
25 a ringing suppression arrangement, embodying an aspect of the invention;

FIGURES 2a-2i illustrate waveforms useful for explaining the operation of the circuit of FIGURE 1 when the ringing suppression arrangement of FIGURE 1 is functional; and

30 FIGURES 3a-3g illustrate waveforms that would be obtained in the circuit of FIGURE 1 should the ringing suppression arrangement of FIGURE 1 be removed.

FIGURE 1 illustrates a horizontal deflection circuit 100, embodying an aspect of the invention, operating at a horizontal
35 frequency $f_H = 15,625$ Hz. Deflection circuit 100 includes a flyback transformer T, a deflection switching transistor Q, a damper diode D, a retrace capacitor C_R , an S-shaping capacitor C_S , a linearity coil L_{Lin} with a parallel coupled damping resistor R_D



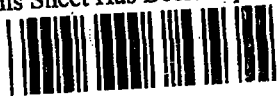
and a horizontal deflection winding L_H . Linearity coil L_{Lin} is coupled between winding L_H and transistor Q.

As shown adjacent to winding L_H , a stray or inter-winding capacitance C_{STRAY} is associated with the windings of winding L_H . Stray capacitance C_{STRAY} is formed between horizontal deflection winding L_H and, for example, a vertical deflection winding, not shown, a yoke ferrite core, not shown, and/or other components in the vicinity. In operation, a ringing suppression network 200, embodying an aspect of the invention, is coupled to a junction terminal 100a, between coil L_{Lin} and winding L_H .

For explanation purposes only, assume that network 200 is disconnected from terminal 100a. In this case, deflection circuit 200 operates in a conventional manner. FIGURES 3a-3g illustrate waveforms useful for the explanation of the way Organ Pipes distortions that are produced when circuit 200 is disconnected. Similar symbols and numerals in FIGURES 1 and 3a-3g indicate similar items or functions.

As a result of the switching operation of transistor Q of FIGURE 1, a retrace voltage $V1$ of FIGURE 3a is developed across deflection transistor Q of FIGURE 1. A retrace voltage $V2$ of FIGURE 3b is developed across winding L_H of FIGURE 1. FIGURE 3c illustrates a deflection current $i1$ that is formed externally to winding L_H and in a current path of winding L_H of FIGURE 1. FIGURE 3d illustrates a waveform of a current $i2$ flowing through stray capacitance C_{STRAY} associated with winding L_H of FIGURE 1. Current $i2$ represents a difference current, measured between current $i1$ and a current $i5$. Current $i5$ flows to ground from an end terminal 100b of winding L_H that is remote from terminal 100a. Current $i2$ may be measured using a current probe for obtaining the current difference between currents $i1$ and $i5$.

During the second half of retrace, current $i1$ is smaller than current $i5$ because of the effect of current $i2$. Current $i2$ affects horizontal scanning because current $i2$ flows through the windings of horizontal deflection winding L_H . Capacitive current $i2$ is dependent on the rate of change of retrace voltage $V2$. Current $i2$ has a positive peak amplitude in the vicinity of an end time, $t1$, of the retrace interval where the high frequency content



of retrace voltages V_1 and V_2 is the largest. When the rate of change of voltage V_2 becomes zero, current i_2 becomes zero.

The fast decrease of current i_2 to zero, at the end of retrace, produces current ringing, as illustrated in FIGURE 3d. Organ Pipes distortions may be formed by current ringing in winding L_H of FIGURE 1 following time t_1 of FIGURE 3d, the end of retrace. The waveforms of FIGURES 3e-3g are shown in the vicinity of time t_1 of FIGURES 3a-3d, but with expanded amplitude and with an expanded time base relative to those of FIGURES 3a-3d. Ringing of current i_2 of FIGURE 3g subtracts from current i_1 of FIGURE 3f and appears superimposed on deflection current i_1 that is coupled to deflection winding L_H of FIGURE 1.

Current i_1 of FIGURE 3f increases at time t_1 by the same amount as current i_2 of FIGURE 3g decreases. The ringing of current i_2 during the $5\mu s$ interval of FIGURE 3g that follow time t_1 is superimposed upon the downramping or trace portion of current i_1 of FIGURE 3f that is coupled to winding L_H of FIGURE 1. The ringing appears also superimposed on retrace voltage V_2 of FIGURE 3e, at the beginning of trace. The ringing is caused by the fast fall time of current i_2 of FIGURE 3g after time t_1 .

In carrying out an inventive feature, ringing suppression network 200 of FIGURE 1, reduces such ringing. Network 200 includes a series arrangement of a resistor R_1 , a capacitor C_1 and a parallel arrangement that includes a resistor R_2 and a switching diode D_1 . Advantageously, linearity coil L_{Lin} is interposed between deflection transistor Q and winding L_H for separating winding L_H from transistor switch Q . Linearity coil L_{Lin} is non-saturated at the beginning of trace and operates as an inductor having an inductance of about 10%-20% of the inductance of winding L_H .

FIGURES 2a-2i illustrate waveforms useful for explaining the operation of the circuit of FIGURE 1 when network 200 is included in the circuit. Similar symbols and numerals in FIGURES 1, 2a-2i and 3a-3g indicate similar items or functions. In FIGURES 2d-2i, the amplitude and the time base are expanded in the vicinity of time t_1 relative to those of FIGURES 2a-2c.

Capacitor C_1 of FIGURE 1 is charged, during retrace, via resistors R_2 and R_1 to a voltage V_3 of minus 20 volts with respect

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to ground, as shown in FIGURE 2b. Retrace voltage V_2 of FIGURE 2a drops to minus 100 volts at the vicinity of time t_1 , the end of retrace, and discharges capacitor C_1 of FIGURE 1 via diode D_1 and resistor R_1 . This injects a pulse of a current i_4 of FIGURE 2c into a junction terminal 100a of FIGURE 1 between winding L_H and linearity coil L_{Lin} . Injected pulse current i_4 is divided between coil L_{Lin} and winding L_H according to the ratio of the inductances of winding L_H and linearity coil L_{Lin} . A greater portion of pulse current i_4 flows through linearity coil L_{Lin} because of its relatively low inductance and subtracts from current i_3 of FIGURE 2g. This causes a decrease of current i_3 in the vicinity of time t_1 . The pulse of current i_4 starts to increase at a fast rate just before time t_1 , it reaches its peak amplitude at time t_1 and then has a slow fall time, as shown in FIGURE 2e.

In accordance with an inventive feature, the suppression of the deflection current ringing is obtained by the decrease of current i_3 of FIGURE 2g, during the aforementioned short interval in the vicinity of time t_1 . The decrease in current i_3 is produced by injected current i_4 of FIGURE 2e. As a result, deflection current i_1 of FIGURE 2f is prevented from increasing after current i_2 of FIGURE 2h abruptly decreases to zero. The smaller portion of current i_4 of FIGURE 2e flows into winding L_H and prevents deflection current i_1 of FIGURE 2f from decreasing prior to time t_1 .

Advantageously, the slow fall time of the pulse of current i_4 of FIGURE 2e, following time t_1 , provides a smooth or gradual transient between currents i_1 and i_3 . Following the short interval at the beginning of trace, when current i_3 is smaller than current i_1 , currents i_1 and i_3 have the same waveform and amplitude, during the remaining trace interval, as shown in FIGURES 2f and 2g, respectively. Advantageously, as a result of the current injection of current i_4 of FIGURE 2e, the ringing that occur in current i_2 of FIGURE 3g no longer occur in current i_2 of FIGURE 2h.

FIGURE 2i illustrates a waveform depicting a difference between currents i_5 and i_3 . The waveform of FIGURE 2i shows that the greater portion of current i_4 of FIGURE 2e in linearity coil L_{Lin} of FIGURE 1 is subtracted from current i_3 of

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FIGURE 2g. Current difference, i_5-i_3 , of FIGURE 2i decreases slowly after time t_1 of FIGURE 2h, providing a smooth transient of voltage V_2 of FIGURE 2d at the end of retrace and the beginning of trace. The peak of current i_4 of FIGURE 2e occurs at the end of retrace, when the rate of change of voltage V_2 of FIGURE 2a is zero. Advantageously, as a result of current i_4 of FIGURE 1, voltage V_2 does not include ringing.

A conventional East-West raster correction circuit may be coupled to end terminal 100b of winding L_H that is remote from linearity coil L_{Lin} , in a conventional manner not shown. In this way, both East-West raster distortion correction and suppression of Organ Pipes ringing may be maintained.

An arrangement similar to that shown in FIGURE 1 may be implemented to provide horizontal deflection for a 34", 16:9 aspect ratio CRT, operating at a horizontal frequency $2f_H$. In this case, winding L_H has an inductance of $350\mu H$, resistor R_1 has a value of 330 Ohm, resistor R_2 has a value of 68 K-Ohm and capacitor C_1 has a value of 470pF.

The values of capacitor C_1 and resistor R_2 are selected in such a way that voltage V_3 of FIGURE 2b is higher, or less negative, than voltage V_2 of FIGURE 2a at time t_1 . The voltage difference, V_3-V_2 , and the values of capacitor C_1 of FIGURE 1 and of resistor R_1 determine the peak amplitude of current i_4 of FIGURE 2e. The fall time of the pulse of current i_4 is determined by resistor R_1 and capacitor C_1 of FIGURE 1.

Stray capacitance C_{STRAY} is dependent on winding L_H . The amplitude of current i_2 strongly depends on the amplitude, pulse-width and the rate of change of voltage V_2 . Therefore, the values of resistors R_1 and R_2 and of capacitor C_1 are selected based on such parameters. Advantageously, because current injection is provided in an AC coupling manner via capacitor C_1 , DC offset current in winding L_H is prevented.

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CLAIMS:

1. A video display deflection apparatus comprising:
a deflection winding (L_H);
a retrace capacitance (CR) coupled to said deflection winding to form a retrace resonant circuit (100);
5 first switching means (Q, D) coupled to said deflection winding for producing a deflection current (i_1, i_5) and a retrace pulse voltage (V_2) therein;
an inductance (L_{LIN}) coupled in a current path of said deflection current between said deflection winding and said first
10 switching means; characterized in that
means ($C1, R1, D1$) for generating a pulse of current (i_4) that is coupled to said inductance and to said deflection winding via a junction terminal (100a), that is in said current path between said inductance and said deflection winding, said pulse of
15 current having both a beginning time and an end time in a vicinity of an instant (t_1) when said retrace pulse voltage ceases, said pulse of current producing a decrease in a current (i_3) that flows in said inductance, during a beginning portion of a trace interval.
- 20 2. An apparatus according to Claim 1 characterized in that said pulse of current (i_4) is AC-coupled to said inductance (L_{LIN}) and to said deflection winding (L_H).
3. An apparatus according to Claim 1 characterized in that said inductance (L_{LIN}) comprises a linearity correction
25 inductance.
4. An apparatus according to Claim 1 characterized in that said pulse of current generating means ($C1, D1, R1$) comprises a first resistor ($R1$) and a second capacitor ($C1$) coupled in series.
5. An apparatus according to Claim 4 characterized by,
30 a diode coupled between said second capacitor and said junction terminal.

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6. An apparatus according to Claim 5 characterized by, a second resistor (R2) coupled in parallel with said diode (D1).

7. A video display deflection apparatus, comprising:
a deflection winding (L_H);

5 a retrace capacitance (CR) coupled to said deflection winding (L_H) to form a retrace resonant circuit (100);

first switching means (D,Q) coupled to said deflection winding (L_H) for generating a resonant retrace pulse voltage (V2) at a first terminal of said deflection winding (100a) and a
10 deflection current (i_5) in said deflection winding, said retrace pulse voltage producing a capacitive current (i_2) in an inter-winding capacitance (C2) of said deflection winding that decreases when said retrace pulse voltage ceases, said decrease in said capacitive current producing an increase in a current (i_1) that
15 flows in said first terminal; characterized in that

means (R1, C1, D1) coupled to said terminal for generating a current pulse (i_4) in a current path that includes said terminal, when said retrace pulse ceases, in a manner to reduce a rate of said increase of said first terminal current such that
20 following a beginning portion of a trace interval, said current pulse ceases.

8. An apparatus according to Claim 7 characterized in that said terminal (100a) is coupled between said deflection winding (L_H) and said first switching means (D,Q).

25 9. An apparatus according to Claim 7 characterized by, a linearity coil (L_{LIN}) coupled between said first switching means (D,Q) and between said deflection winding (L_H) and said current pulse generating means (R1, C1, D1).

10. An apparatus according to Claim 9 characterized
30 in that said current pulse generating means (R1, C1, D1) is coupled between said linearity coil (L_{LIN}) and said deflection winding (L_H).

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11. An apparatus according to Claim 9 characterized in that said current pulse (i_4) causes a current (i_3) that flows in said linearity coil (L_{LW}) to decrease, during said beginning portion of said trace interval.

5 12. An apparatus according to Claim 7 characterized in that said current pulse generating means (R_1 , C_1 , D_1) comprises a third capacitance (C_1) that is coupled to said resonant circuit for applying said retrace pulse voltage (V_2) to said third capacitance to develop a voltage in said third capacitance, during said retrace
10 interval, said third capacitance voltage producing said current pulse (i_4) and second switching means (D_1) for decoupling said third capacitance from said deflection winding, during a portion of said trace interval that follows said beginning portion of said trace interval.

15 13. An apparatus according to Claim 7 characterized in that said current pulse (i_4) causes a parasitic ringing in said deflection current to be suppressed for preventing organ pipes distortions.

20 14. An apparatus according to Claim 7 characterized in that said deflection winding (L_H) comprises a horizontal deflection winding.

 15. A video display deflection apparatus, comprising:
a deflection winding (L_H);
a retrace capacitance (CR) coupled to said deflection
25 winding to form a retrace resonant circuit (100);
first switching means (D, Q) coupled to said deflection winding for producing a deflection current (i_5) and a retrace pulse (V_2) therein;

30 an inductance (L_H) coupled in a current path of said deflection current between said deflection winding and said first switching means; characterized in that

 a series arrangement of a resistor (R_1) and a second capacitor (C_1) for producing from said retrace pulse voltage a



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current (i_4 , during retrace) that charges said second capacitor such that said resistor limits said charging current; and

second switching means (D1) coupled to said second capacitor for generating a pulse of current (i_4 , during beginning of trace) from the charge in said second capacitor in a manner that bypasses said resistor so as to prevent said resistor from limiting said current pulse, said current pulse being coupled to said inductance and to said deflection winding via a junction terminal (100a) that is in said current path between said inductance and said deflection winding.

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