CLAIMS:

1. A method used in forming a memory array comprising strings of memory cells and operative through-array-vias (TAVs), the method comprising:

forming a stack (18) comprising vertically-alternating insulative (20) tiers and conductive tiers (22), the stack comprising a TAV region (21,21A,21B) and an operative memory-cell-string region (23), the TAV region (21,21A,21B) comprising spaced operative TAV areas (27);

forming operative channel-material strings (53) in the stack (18) in the operative memory-cell-string region (23) and forming dummy channel-material strings (35) in the stack (18) in the TAV region (21,21A,21B) laterally outside of and not within the operative TAV areas (27); and

forming operative TAVs (45) in individual of the spaced operative TAV areas (27) in the TAV region (21,21A,21B).

2. The method of claim 1 comprising forming the operative and dummy channel-material strings at the same time.

3. The method of claim 1 comprising forming the operative TAVs after forming the operative and dummy channel-material strings.

4. The method of claim 1 comprising forming the operative and dummy channel-material strings to individually have the same shape relative to one another.

5. The method of claim 1 comprising forming the operative and dummy channel-material strings to individually have the same size and shape relative to one another.

6. The method of claim 1 comprising forming the operative channel-material strings and the dummy channel-material strings to have the same pitch relative to one another.

7. The method of claim 6 comprising forming the operative and dummy channel-material strings to individually have the same size and shape relative to one another.

8. The method of claim 1 comprising forming the operative and dummy channel-material strings to individually be smaller in a horizontal direction than the operative TAVs.

9. The method of claim 1 wherein the operative channel-material strings are within laterally-spaced memory blocks that comprise part of a memory plane; the dummy channel-material strings, the TAV region, and the operative TAVs being within the memory plane.

10. The method of claim 1 wherein the operative channel-material strings are within laterally-spaced memory blocks that comprise part of a memory plane; the dummy channel-material strings, the TAV region, and the operative TAVs being outside of the memory plane.

11. The method of claim 10 wherein the dummy channel-material strings, the TAV region, and the operative TAVs are formed at an edge of a memory plane.

12. The method of claim 10,

wherein the dummy channel-material strings, the TAV region, and the operative TAVs are formed in a landing region of a stair-step region; and

further comprising:

forming an operative stair-step structure into the stack in the stair-step region and a landing in the landing region of the stair-step region.

13. The method of claim 12 wherein the landing is a crest of the operative stair-step structure.

14. The method of claim 1 wherein the operative channel-material strings are within laterally-spaced memory blocks that comprise part of a memory plane; and

further comprising:

forming multiple of said TAV regions that are laterally spaced relative to one another, at least one of said TAV regions being within the memory plane, at least another one of said TAV regions being outside of the memory plane.

15. A method used in forming a memory array comprising strings of memory cells and operative through-array-vias (TAVs), the method comprising:

forming a stack comprising vertically-alternating insulative tiers and conductive tiers, the insulative tiers comprising insulative first material, the conductive tiers comprising a second material of different composition from that of the first material, the stack comprising a TAV region and an operative memory-cell-string region;

forming operative channel-material strings in the stack in the operative memory-cell-string region and forming dummy channel-material strings in the stack in the TAV region;

forming operative TAVs in the TAV region;

forming horizontally-elongated trenches into the stack;

replacing the second material from the conductive tiers with conducting material that is used to form individual conductive lines in the conductive tiers; and

forming elevationally-extending strings of memory cells in the stack; individual of the memory cells comprising channel material of the operative channel-material strings, a gate region that is part of one of the individual conductive lines, and a memory structure laterally between the gate region and the channel material of the operative channel-material strings in the individual conductive tiers.

16. A method used in forming a memory array comprising strings of memory cells and operative through-array-vias (TAVs), the method comprising:

forming a stack comprising vertically-alternating insulative tiers and conductive tiers, the stack comprising an operative memory-cell-string region, the stack comprising a stair-step region comprising a landing region comprising a TAV region;

forming operative channel-material strings in the stack in the operative memory-cell-string region and dummy channel-material strings in the stack in the TAV region of the landing region;

forming operative TAVs in the TAV region of the landing region; and

forming an operative stair-step structure into the stack in the stair-step region and a landing in the landing region of the stair-step region.

17. A memory array comprising:

a vertical stack comprising alternating insulative tiers and conductive tiers, the conductive tiers comprising gate regions of individual memory cells, the gate regions individually comprising part of a conductive line in individual of the conductive tiers; operative channel-material strings extending through the insulative tiers and the conductive tiers;

the Individual memory cells comprising a memory structure laterally between individual of the gate regions and channel material of the operative channel-material strings;

an operative stair-step structure comprising the insulative tiers and the conductive tiers; and

a landing region adjacent steps of the operative stair-step structure, the landing region comprising a landing and operative TAVs extending through the insulative tiers and the conductive tiers, the landing region comprising dummy channel-material strings in the insulative tiers and the conductive tiers.

18. The memory array of claim 17 wherein the operative and dummy channel-material strings individually have the same horizontal shape relative to one another.

19. The memory array of claim 17 wherein the operative and dummy channel-material strings individually have the same size and shape relative to one another.

20. The memory array of claim 17 wherein the operative channel-material strings and the dummy channel-material strings have the same pitch relative to one another.

21. The memory array of claim 20 wherein the operative and dummy channel-material strings individually have the same size and shape relative to one another.

22. The memory array of claim 17 wherein the operative and dummy channel-material strings individually are horizontally smaller than the operative TAVs.

23. The memory array of claim 17 comprising CMOS-under-array circuitry.

24. The memory array of claim 17 comprising NAND.