

Abstract

A memory device includes a memory bank including one or more bank arrays, a PIM circuit configured to perform an operation logic processing operation, and an instruction memory including first to m^{th} instruction queue segments configured in a circular instruction queue to store instructions provided by a host, where instructions stored in the first to m^{th} instruction queue segments are executed in response to an operation request from the host and each new instruction provided by the host is updated over a completely executed instruction in the circular instruction queue.

FIG. 2