

ABSTRACT

A semiconductor memory device includes horizontal patterns disposed on a peripheral circuit structure and spaced apart from each other in a first direction. Memory structures are disposed on the horizontal patterns. The memory structures include source structures and electrode structures. A division structure is disposed between adjacent horizontal patterns in the first direction and is configured to separate the source structures of adjacent memory structures from each other. An etch stop pattern is disposed between the horizontal patterns at a level lower than a level of the source structures. The etch stop pattern is connected to a lower portion of the division structure.

FIG. 5