

What is claimed is:

1. A stacked semiconductor device comprising:

a plurality of semiconductor dies in the stacked semiconductor device stacked in a first direction;

M data paths electrically connecting two of the plurality of semiconductor dies, one data path of the M data paths comprising one or more through-silicon vias, wherein M is a positive integer;

a transmission circuit comprising M serialization units configured to serialize P transmission signals to M serial signals and output the M serial signals to the M data paths, respectively, wherein P is a positive integer greater than M; and

a reception circuit comprising M parallelization units configured to receive the M serial signals from the M data paths and parallelize the M serial signals to P reception signals corresponding to the P transmission signals,

wherein one of the M serialization units comprises:

N transmission gates configured to transfer N transmission signals among the P transmission signals in a round-robin order to each of the M data paths in response to N serialization strobe signals having different phases, respectively.

2. The stacked semiconductor device of claim 1,

wherein N is 3 or more.

3. The stacked semiconductor device of claim 1 or claim 2, wherein one of the M parallelization units comprises:

N flip-flops configured to sample respective ones of the M serial signals in response to N parallelization strobe signals having different phases, respectively, to generate N

reception signals corresponding to the N flip-flops among the P reception signals.

4. The stacked semiconductor device of any one of claims 1 to 3, wherein one of the M parallelization units comprises:

N transmission gates configured to sample a respective one of the M serial signals in response to N parallelization strobe signals having different phases, respectively, to generate corresponding N reception signals among the P reception signals.

5. The stacked semiconductor device of claim 4,
wherein a pulse width of one of the N parallelization strobe signals corresponds to a duration time of one data bit of the M serial signals, and
wherein the pulse width of the one of the N parallelization strobe signals is shorter than the duration time of the one data bit of the M serial signals.

6. The stacked semiconductor device of any one of claims 1 to 5, further comprising:

one or more strobe paths electrically connecting the plurality of semiconductor dies, each of the one or more strobe paths comprising one or more through-silicon vias,

wherein one of the M parallelization units parallelizes a respective one of the M serial signals to corresponding ones of the P reception signals in response to one or more parallelization strobe signals transferred through the one or more strobe paths.

7. The stacked semiconductor device of claim 6, wherein the transmission circuit further comprises:

a strobe generation circuit configured to generate the one or more parallelization

strobe signals based on a source clock signal to output the one or more parallelization strobe signals to the one or more strobe paths.

8. The stacked semiconductor device of claim 7, wherein the strobe generation circuit is further configured to generate one or more serialization strobe signals synchronized with corresponding ones of the one or more parallelization strobe signals based on the source clock signal, and

wherein one of the M serialization units serializes corresponding ones the P transmission signals to a corresponding one of the M serial signals in response to the one or more serialization strobe signals.

9. The stacked semiconductor device of claim 6, wherein the transmission circuit further comprises a strobe generation circuit configured to generate one or more sampling clock signals to output the one or more sampling clock signals to the one or more strobe paths, and

wherein the reception circuit further comprises a pulse generation circuit configured to receive the one or more sampling clock signals from the one or more strobe paths and generate the one or more parallelization strobe signals synchronized with rising edges and/or falling edges of the one or more sampling clock signals.

10. The stacked semiconductor device of claim 6, wherein the transmission circuit further comprises a strobe generation circuit configured to generate one or more strobe differential signal pairs to output the one or more strobe differential signal pairs to the one or more strobe paths, and

wherein the reception circuit further comprises a differential amplification circuit

configured to receive the one or more strobe differential signal pairs from the one or more strobe paths and generate the one or more parallelization strobe signals based on the one or more strobe differential signal pairs.

11. The stacked semiconductor device of any one of claims 1 to 10, wherein one of the M serialization units serializes N transmission signals among the P transmission signals to generate a corresponding one of the M serial signals, and

wherein one of the M parallelization units parallelizes a corresponding one of the M serial signals to generate N reception signals among the P reception signals.

12. The stacked semiconductor device of any one of claims 1 to 11, wherein one of the M serialization units comprises:

a first transmission gate connected between a first input node receiving a first transmission signal among the P transmission signals and an output node connected to one of the M data paths, the first transmission gate configured to be turned on during an activation time of a first serialization strobe signal; and

a second transmission gate connected between a second input node receiving a second transmission signal among the P transmission signals and the output node, the second transmission gate configured to be turned on during an activation time of a second serialization strobe signal having a phase different from a phase of the first serialization strobe signal.

13. The stacked semiconductor device of any one of claims 1 to 12, wherein one of the M parallelization units comprises:

a first flip-flop comprising a data terminal receiving a serial signal among the M

serial signals, a clock terminal receiving a first parallelization strobe signal, and an output terminal generating a first reception signal among the P reception signals; and

a second flip-flop comprising a data terminal receiving the serial signal, a clock terminal receiving a second parallelization strobe signal having a second phase different from a first phase of the first parallelization strobe signal, and an output terminal generating a second reception signal among the P reception signals.

14. The stacked semiconductor device of any one of claims 1 to 13, wherein one of the M parallelization units comprises:

a rising edge triggered flip-flop comprising a data terminal receiving a serial signal among the M serial signals, a clock terminal receiving a parallelization strobe signal, and an output terminal generating a first reception signal among the P reception signals; and

a falling edge triggered flip-flop comprising a data terminal receiving the serial signal, a clock terminal receiving the parallelization strobe signal, and an output terminal generating a second reception signal among the P reception signals.

15. The stacked semiconductor device of any one of claims 1 to 14, wherein one of the M parallelization units comprises:

a first transmission gate connected between an input node receiving a serial signal among the M serial signals and a first output node generating a first reception signal among the P reception signals, the first transmission gate configured to be turned on during an activation time of a first parallelization strobe signal; and

a second transmission gate connected between the input node and a second output node generating a second reception signal among the P reception signals, the second transmission gate configured to be turned on during an activation time of a second

parallelization strobe signal having a second phase different from a first phase of the first parallelization strobe signal.

16. The stacked semiconductor device of any one of claims 1 to 15, wherein the transmission circuit is included in a first semiconductor die among the plurality of semiconductor dies, and the reception circuit is included in a second semiconductor die among the plurality of semiconductor dies.

17. A system comprising:

a base substrate;

a plurality of semiconductor dies stacked on the base substrate in a first direction;

and

a plurality of data paths electrically connecting the plurality of semiconductor dies, one data path of the plurality of data paths comprising one or more through-silicon vias,

wherein the system is configured to serialize a plurality of transmission signals to a plurality of serial signals to output the plurality of serial signals to the plurality of data paths, respectively, in a first semiconductor die among the plurality of semiconductor dies,

wherein the number of the plurality of transmission signals is greater than the number of the plurality of data paths,

wherein the system is configured to parallelize the plurality of serial signals received from the plurality of data paths to a plurality of reception signals corresponding to the plurality of transmission signals in a second semiconductor die among the plurality of semiconductor dies,

wherein the first semiconductor die comprises M serialization units to serialize the plurality of transmission signals, and

wherein one of the M serialization units comprises:

N transmission gates configured to transfer N transmission signals among the P transmission signals in a round-robin order to each of the M data paths in response to N serialization strobe signals having different phases, respectively.

18. The system of claim 17, further comprising:

one or more strobe paths electrically connecting the plurality of semiconductor dies, each of the one or more strobe paths comprising a respective one of the one or more through-silicon vias,

wherein a plurality of parallelization strobe signals used to parallelize the plurality of serial signals to the plurality of reception signals are provided from the first semiconductor die to the second semiconductor die through the one or more strobe paths.

19. A method of transferring signals in a stacked semiconductor device, the method comprising:

stacking a plurality of semiconductor dies in a first direction;

electrically connecting the plurality of semiconductor dies through M data paths, at least one data path of the M data paths comprising a through-silicon via, wherein M is a positive integer;

serializing P transmission signals to M serial signals in a first semiconductor die among the plurality of semiconductor dies to output the M serial signals to the M data paths, respectively, wherein P is a positive integer greater than M; and

parallelizing the M serial signals received from the M data paths to P reception signals corresponding to the P transmission signals in a second semiconductor die among the plurality of semiconductor dies,

wherein the first semiconductor die comprises M serialization units to serialize the plurality of transmission signals, and

wherein one of the M serialization units comprises:

N transmission gates configured to transfer N transmission signals among the P transmission signals in a round-robin order to each of the M data paths in response to N serialization strobe signals having different phases, respectively.

20. The method of claim 19, wherein the through-silicon via comprises a first through-silicon via, the method further comprising:

electrically connecting the plurality of semiconductor dies through one or more strobe paths, at least one of the one or more strobe paths comprising a second through-silicon via; and

providing a plurality of parallelization strobe signals used to parallelize the plurality of M serial signals to the plurality of P reception signals from the first semiconductor die to the second semiconductor die through the one or more strobe paths.