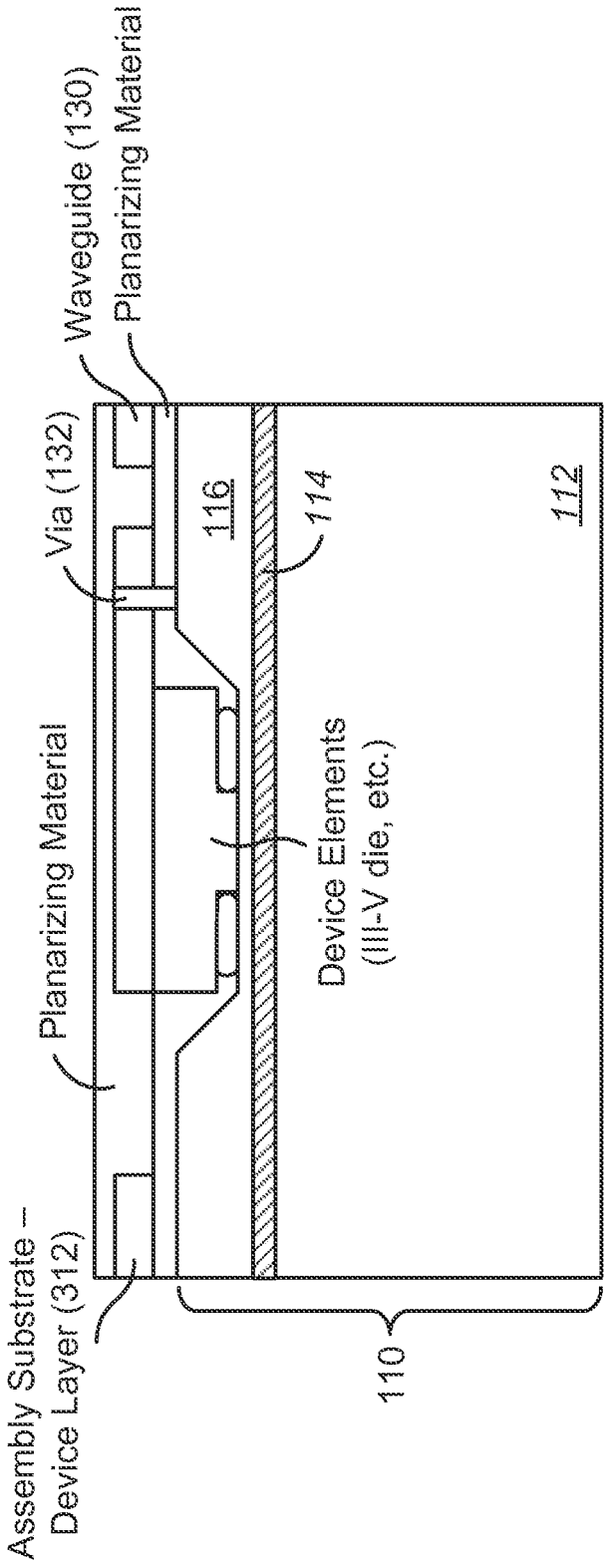

100
Waveguide (130)
Planarizing Material
Via (132)
116
114
112
Planarizing Material
Device Elements
(III-V die, etc.)
Assembly Substrate –
Device Layer (312)
110

FIG. 1

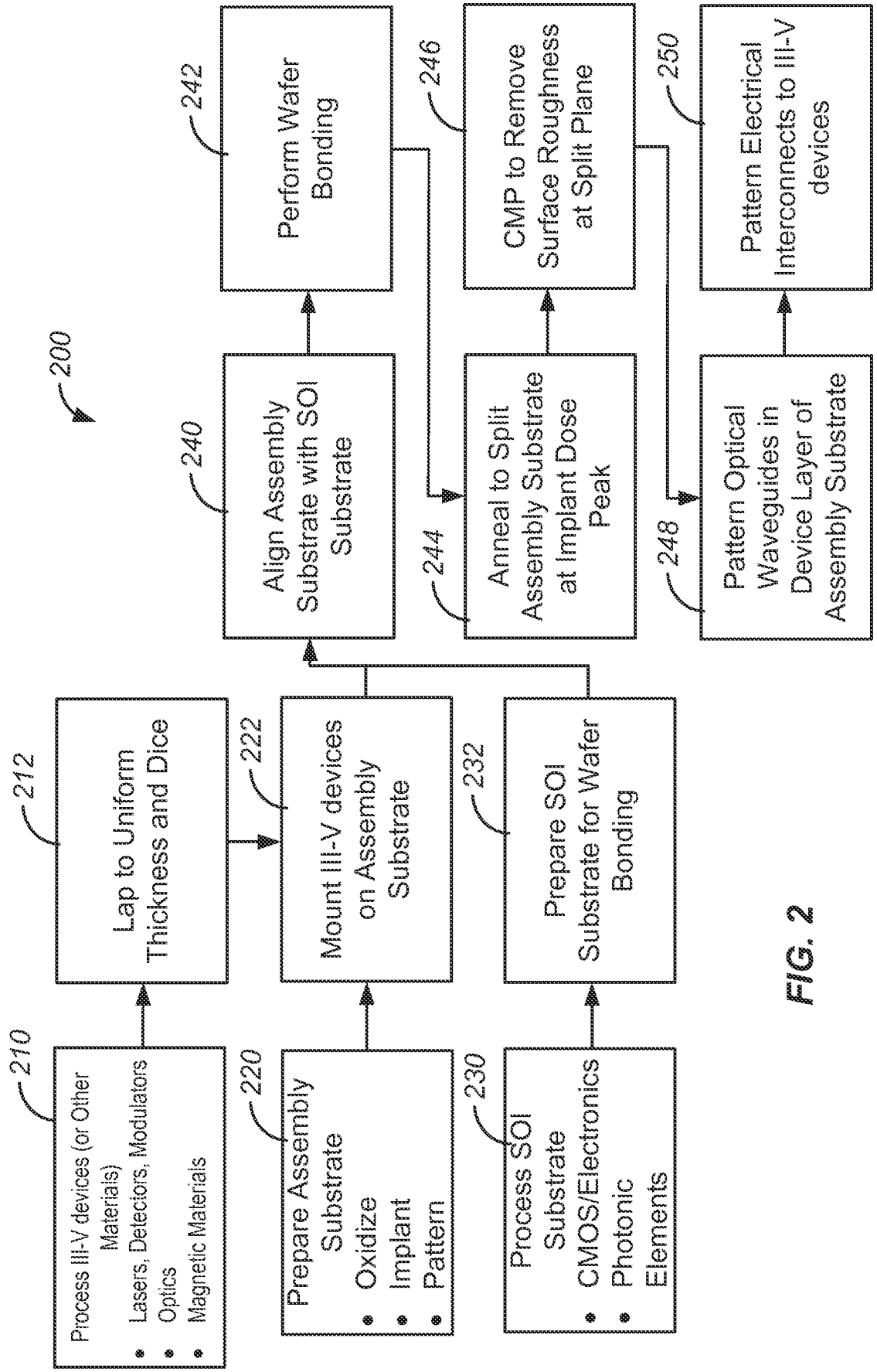

200
210
Process III-V devices (or Other Materials)
Lasers, Detectors, Modulators
Optics
Magnetic Materials
212
Lap to Uniform Thickness and Dice
220
Prepare Assembly Substrate
Oxidize
Implant
Pattern
222
Mount III-V devices on Assembly Substrate
230
Process SOI Substrate
CMOS/Electronics
Photonic Elements
232
Prepare SOI Substrate for Wafer Bonding
240
Align Assembly Substrate with SOI Substrate
242
Perform Wafer Bonding
244
Anneal to Split Assembly Substrate at Implant Dose Peak
246
CMP to Remove Surface Roughness at Split Plane
248
Pattern Optical Waveguides in Device Layer of Assembly Substrate
250
Pattern Electrical Interconnects to III-V devices

FIG. 2

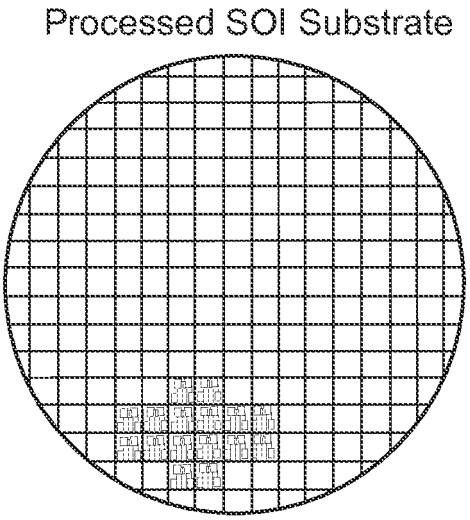


FIG. 3A

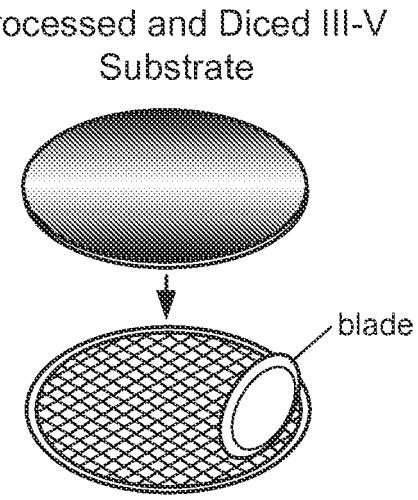


FIG. 3B

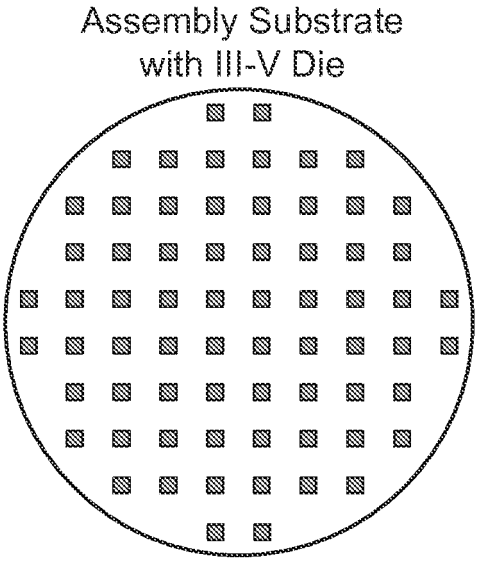


FIG. 3C

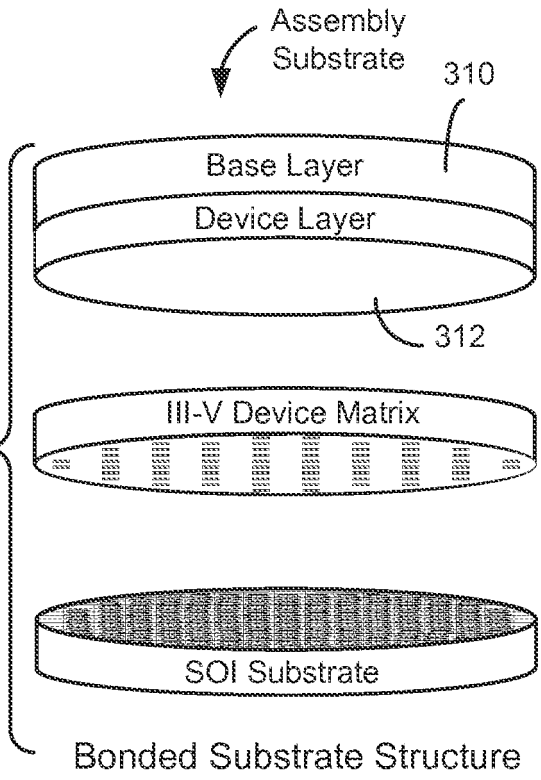


FIG. 3D

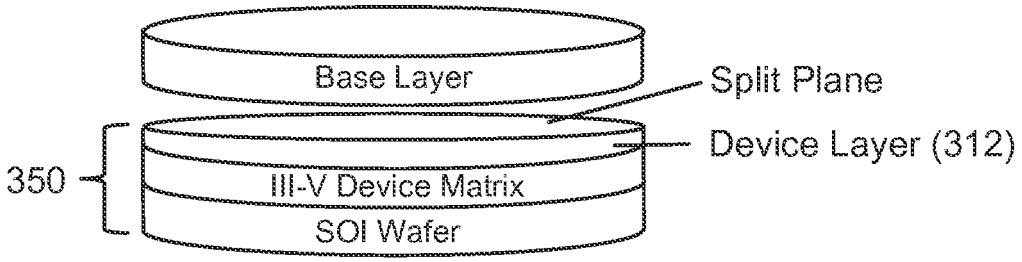


FIG. 3E

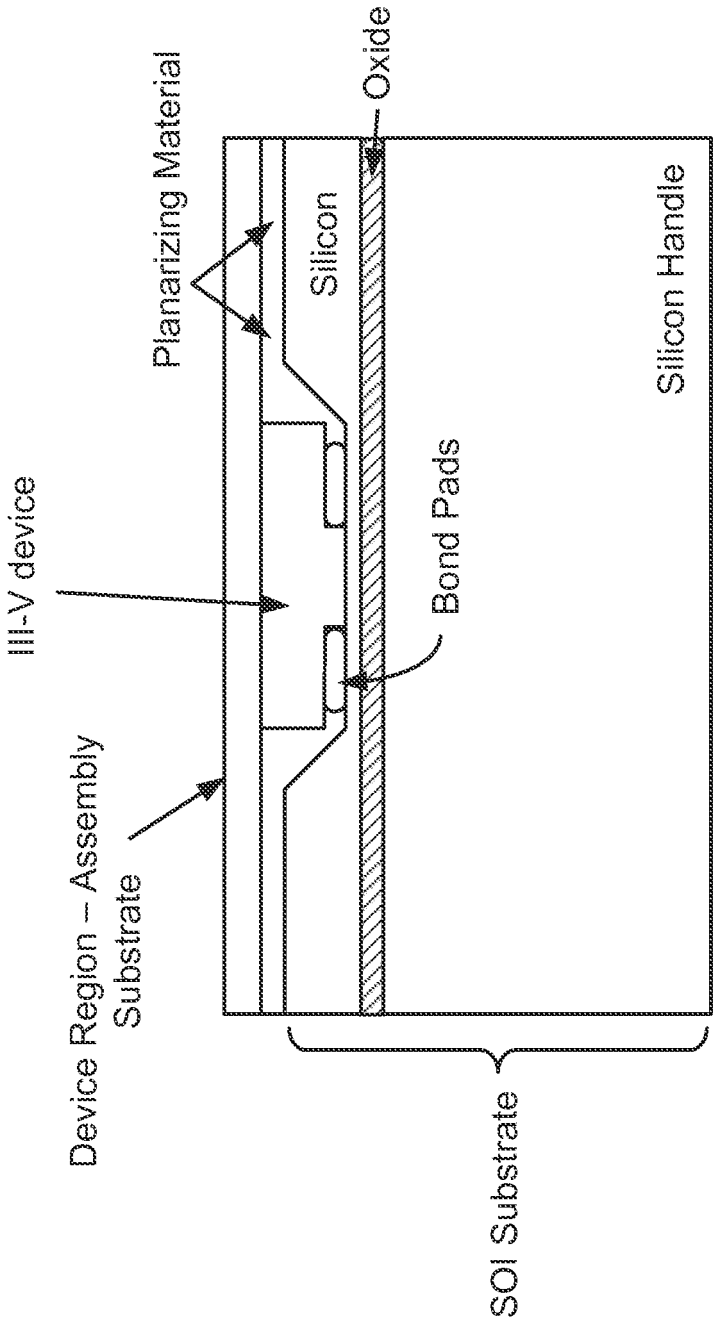

Oxide
Planarizing Material
Silicon
Silicon Handle
III-V device
Bond Pads
Device Region – Assembly Substrate
SOI Substrate

FIG. 4

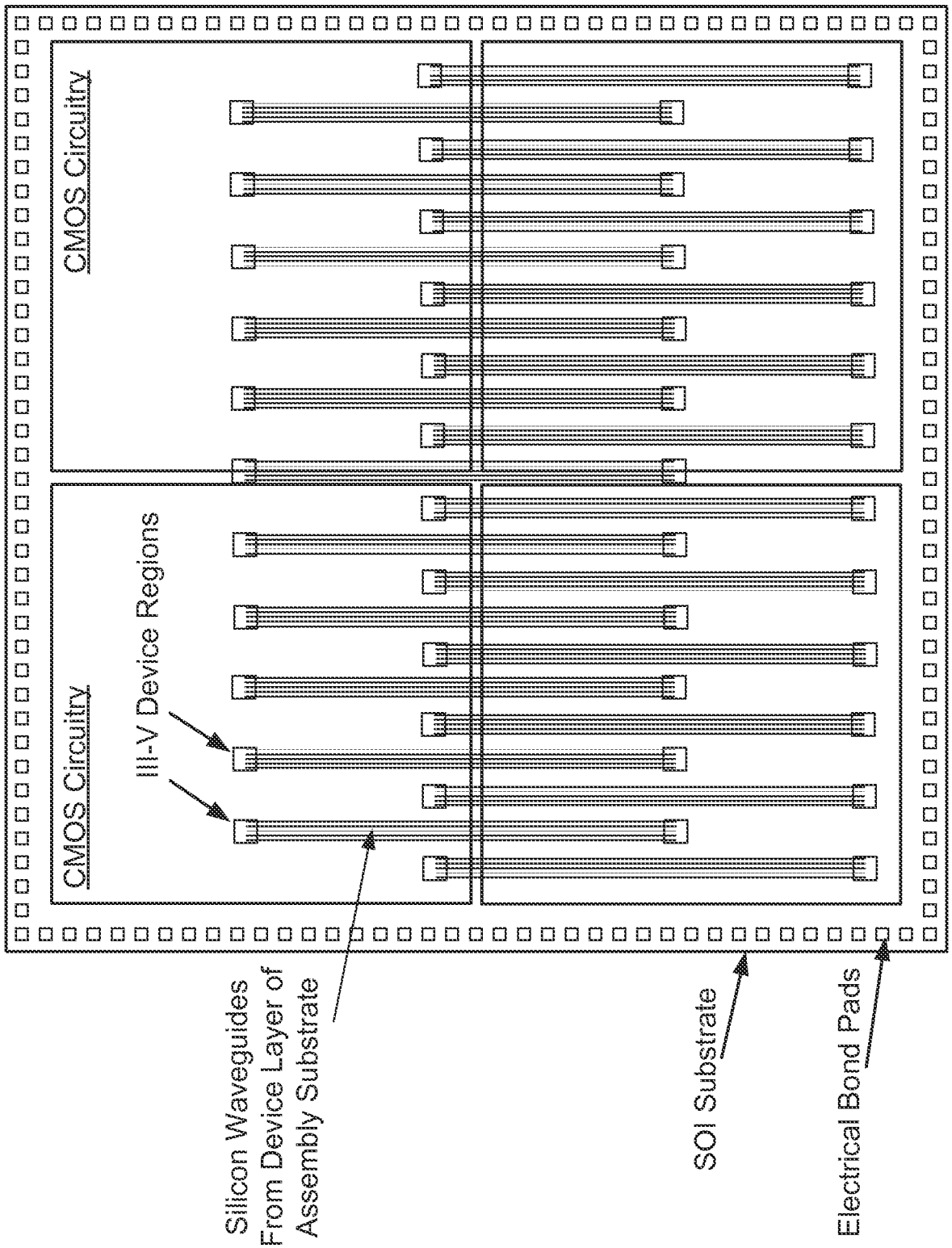

CMOS Circuitry
CMOS Circuitry
III-V Device Regions
Silicon Waveguides From Device Layer of Assembly Substrate
SOI Substrate
Electrical Bond Pads

FIG. 5

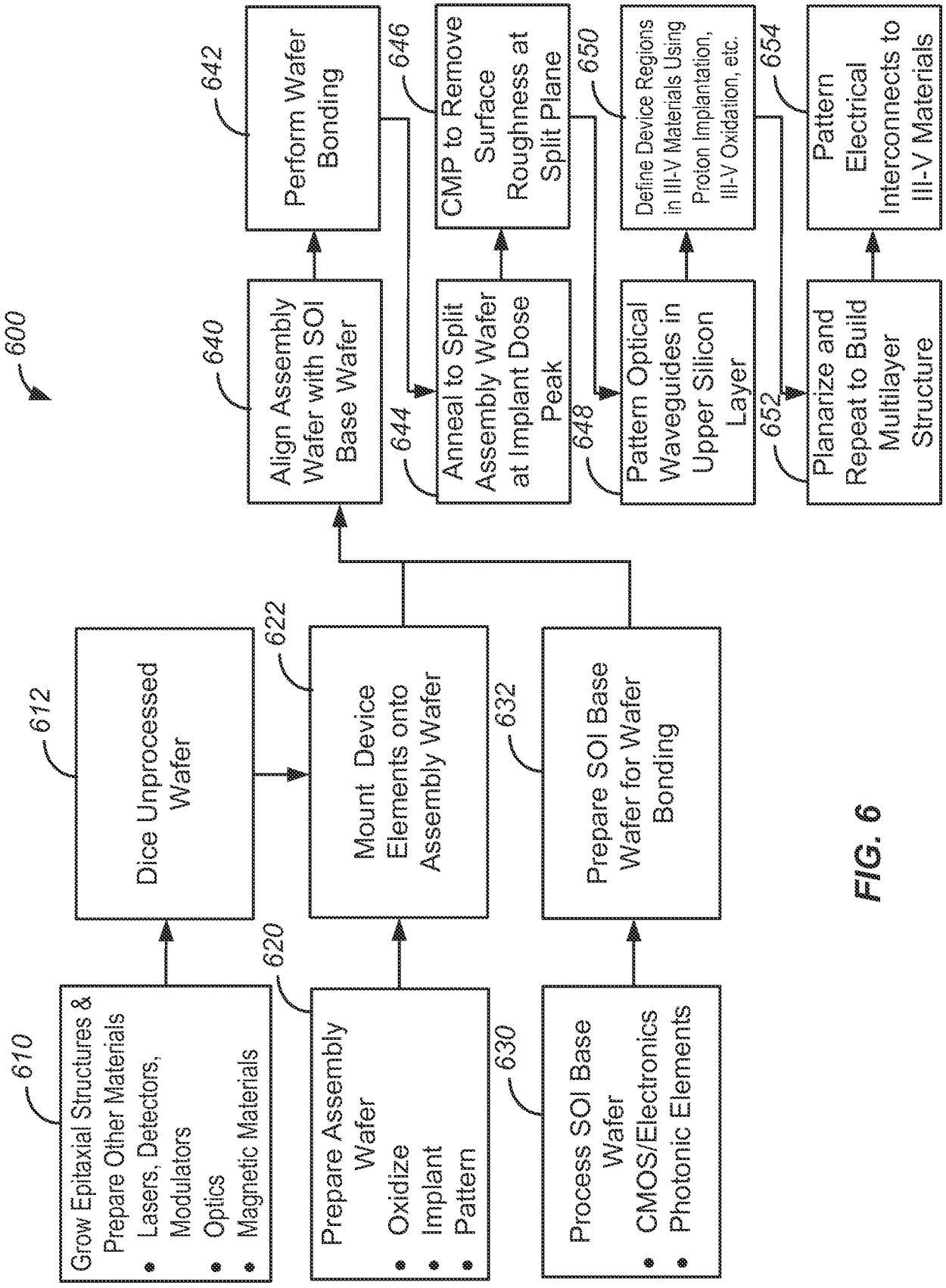

600
610
Grow Epitaxial Structures & Prepare Other Materials
Lasers, Detectors, Modulators
Optics
Magnetic Materials
620
Prepare Assembly Wafer
Oxidize
Implant
Pattern
630
Process SOI Base Wafer
CMOS/Electronics
Photonic Elements
612
Dice Unprocessed Wafer
622
Mount Device Elements onto Assembly Wafer
632
Prepare SOI Base Wafer for Wafer Bonding
640
Align Assembly Wafer with SOI Base Wafer
642
Perform Wafer Bonding
644
Anneal to Split Assembly Wafer at Implant Dose Peak
646
CMP to Remove Surface Roughness at Split Plane
648
Pattern Optical Waveguides in Upper Silicon Layer
650
Define Device Regions in III-V Materials Using Proton Implantation, III-V Oxidation, etc.
652
Planarize and Repeat to Build Multilayer Structure
654
Pattern Electrical Interconnects to III-V Materials

FIG. 6

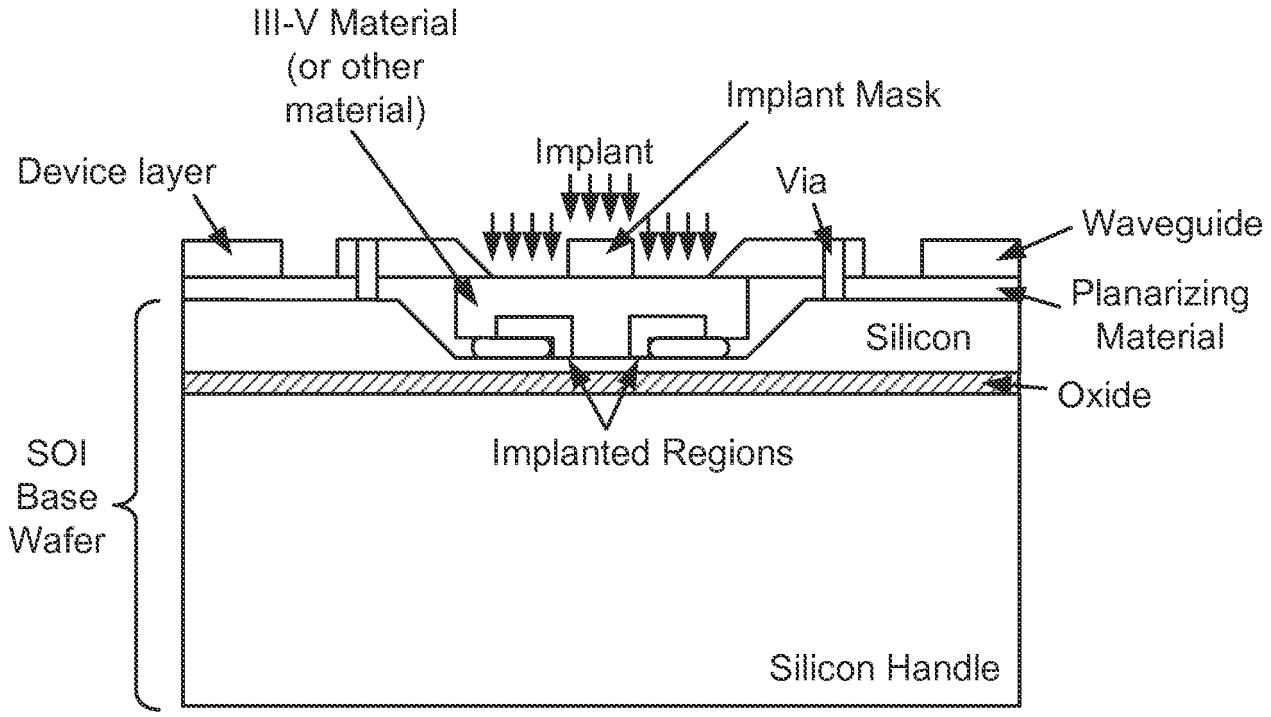

III-V Material
(or other
material)
Implant Mask
Implant
Device layer
Via
Waveguide
Planarizing
Material
Silicon
Oxide
Implanted Regions
SOI
Base
Wafer
Silicon Handle

FIG. 7A

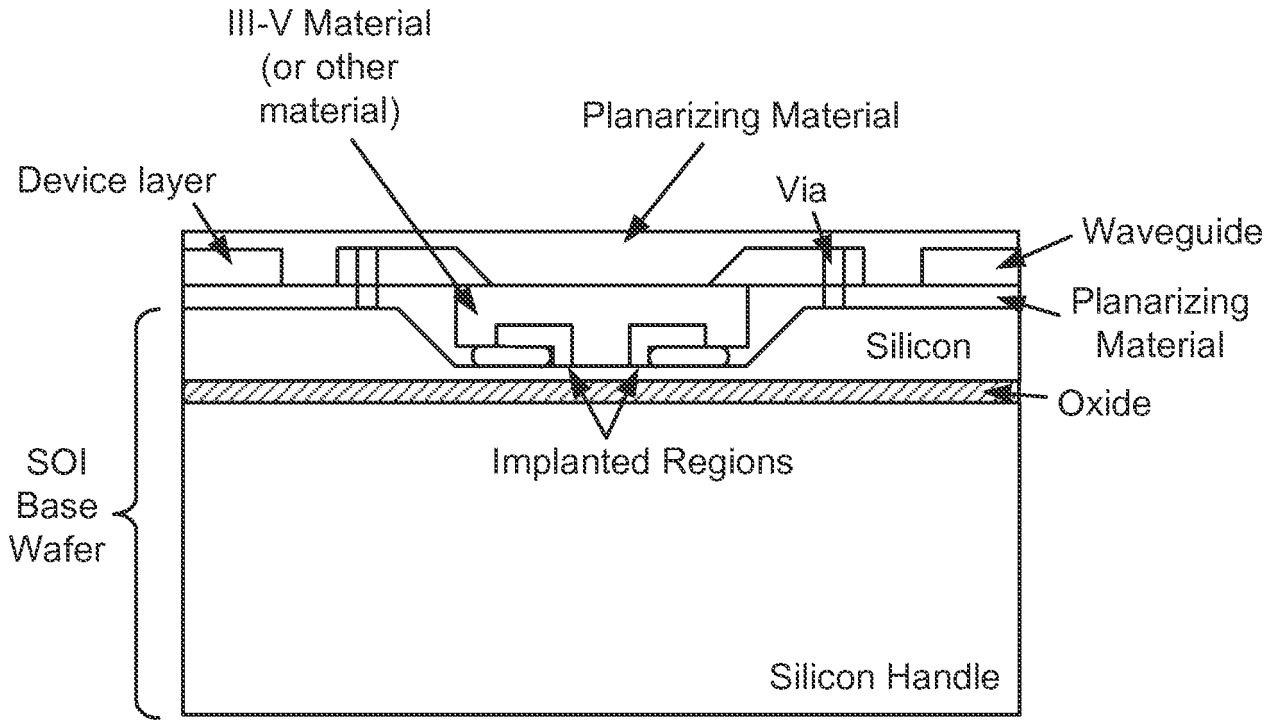

III-V Material
(or other
material)
Planarizing Material
Device layer
Via
Waveguide
Planarizing
Material
Silicon
Oxide
Implanted Regions
SOI
Base
Wafer
Silicon Handle

FIG. 7B

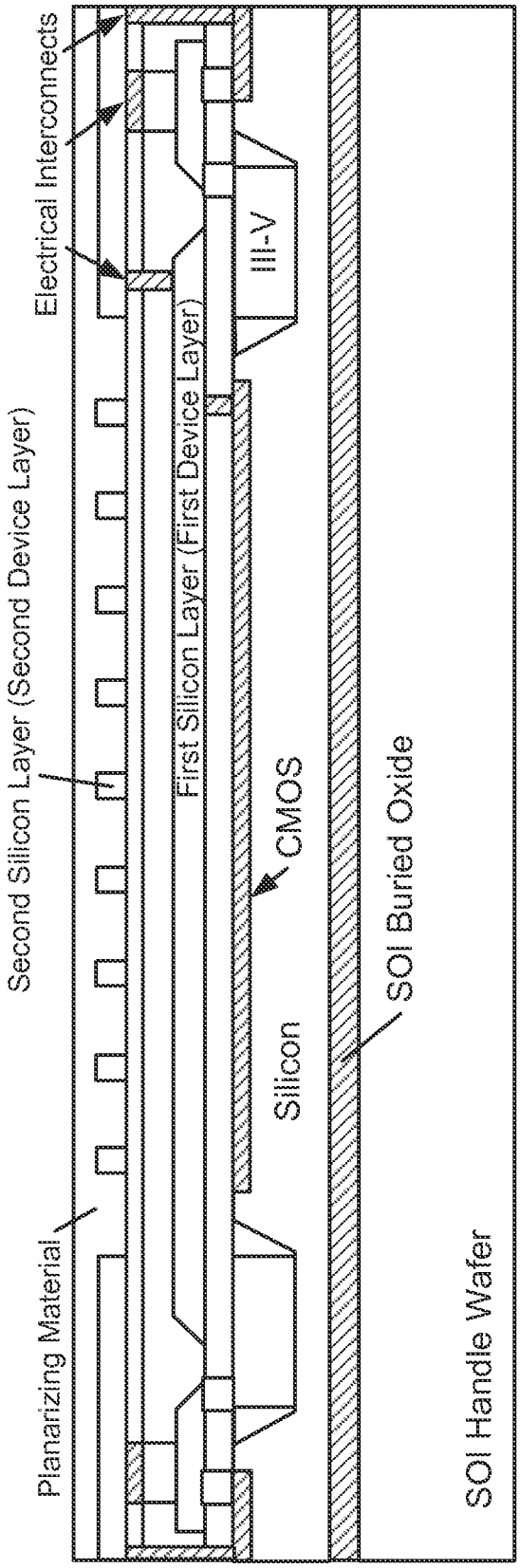

Electrical Interconnects
Second Silicon Layer (Second Device Layer)
First Silicon Layer (First Device Layer)
III-V
CMOS
Silicon
SOI Buried Oxide
Planarizing Material
SOI Handle Wafer

FIG. 7C

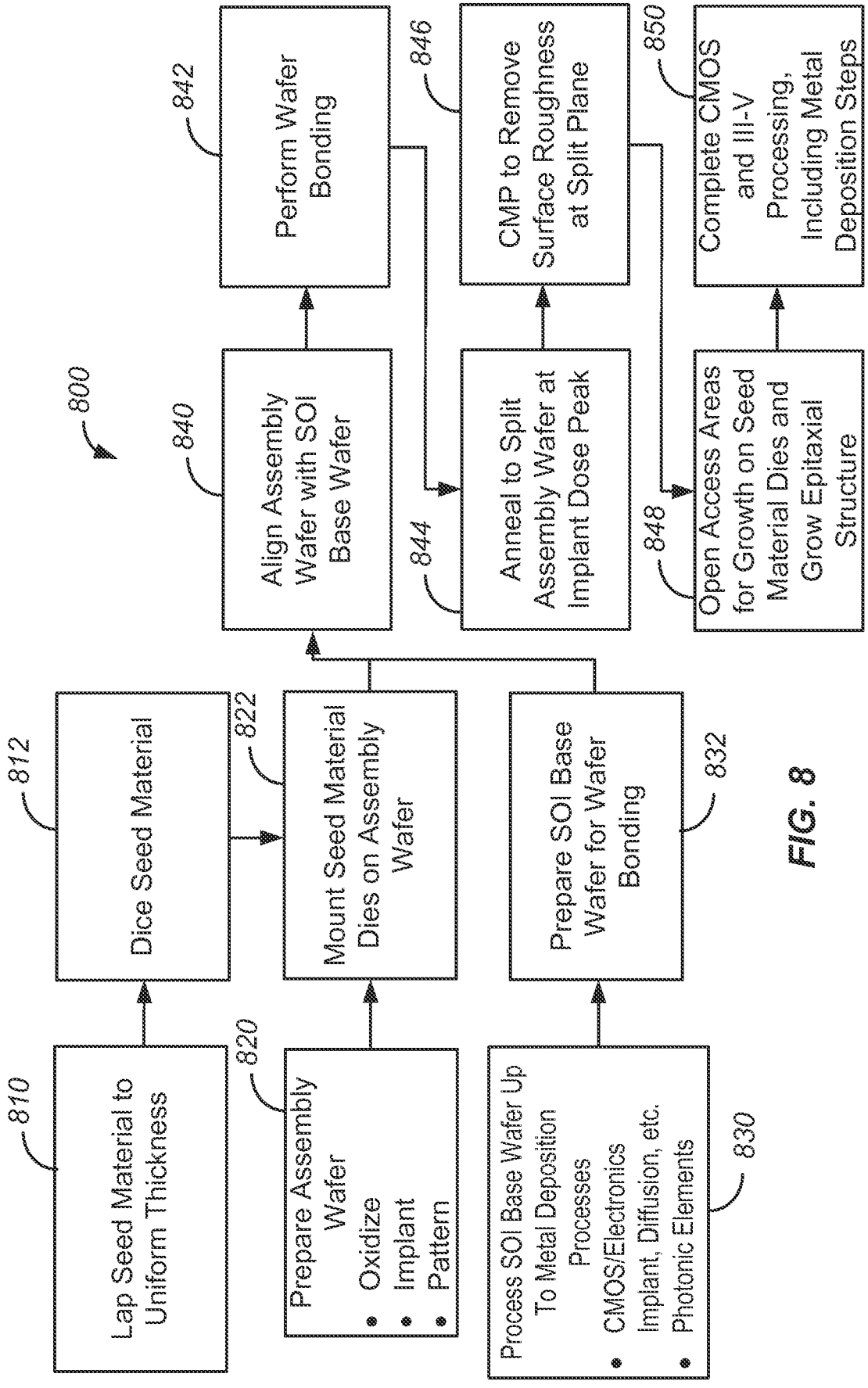

800
810
Lap Seed Material to Uniform Thickness
812
Dice Seed Material
820
Prepare Assembly Wafer
• Oxidize
• Implant
• Pattern
822
Mount Seed Material Dies on Assembly Wafer
830
Process SOI Base Wafer Up To Metal Deposition Processes
• CMOS/Electronics Implant, Diffusion, etc.
• Photonic Elements
832
Prepare SOI Base Wafer for Wafer Bonding
840
Align Assembly Wafer with SOI Base Wafer
842
Perform Wafer Bonding
844
Anneal to Split Assembly Wafer at Implant Dose Peak
846
CMP to Remove Surface Roughness at Split Plane
848
Open Access Areas for Growth on Seed Material Dies and Grow Epitaxial Structure
850
Complete CMOS and III-V Processing, Including Metal Deposition Steps

FIG. 8

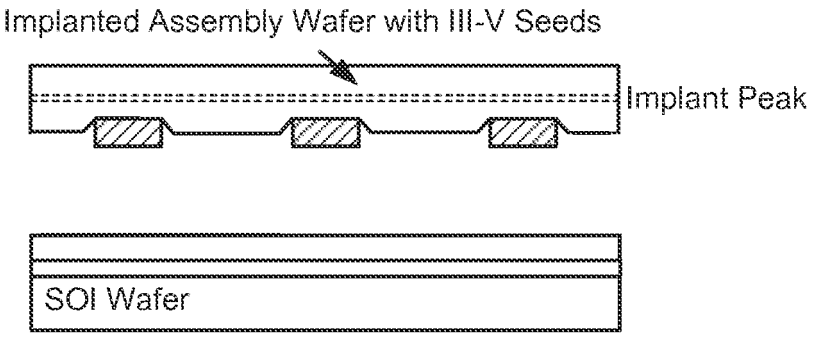


FIG. 9A

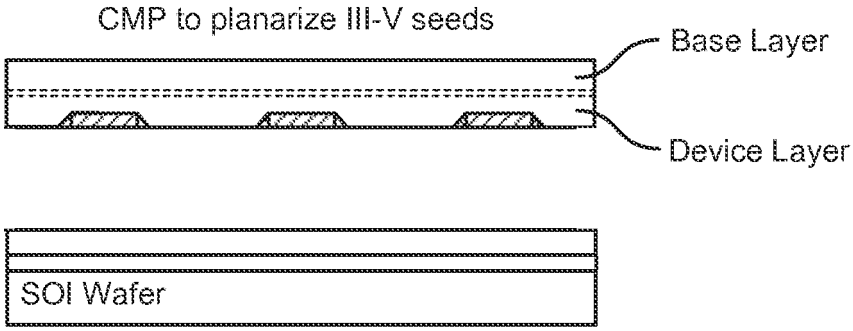


FIG. 9B

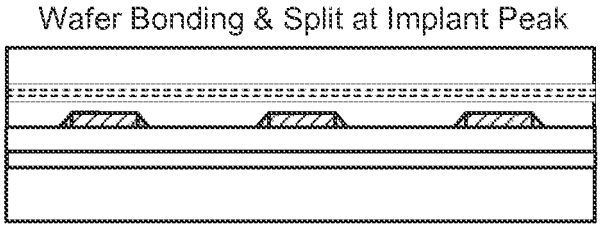


FIG. 9C

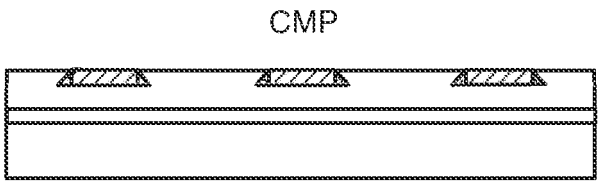


FIG. 9D

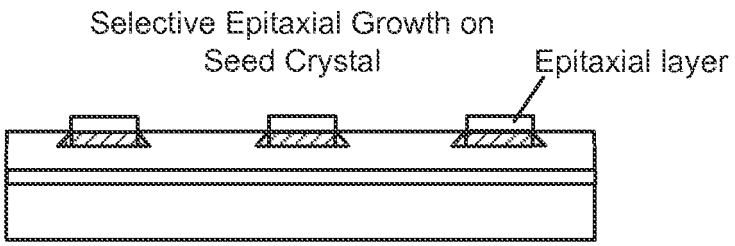


FIG. 9E

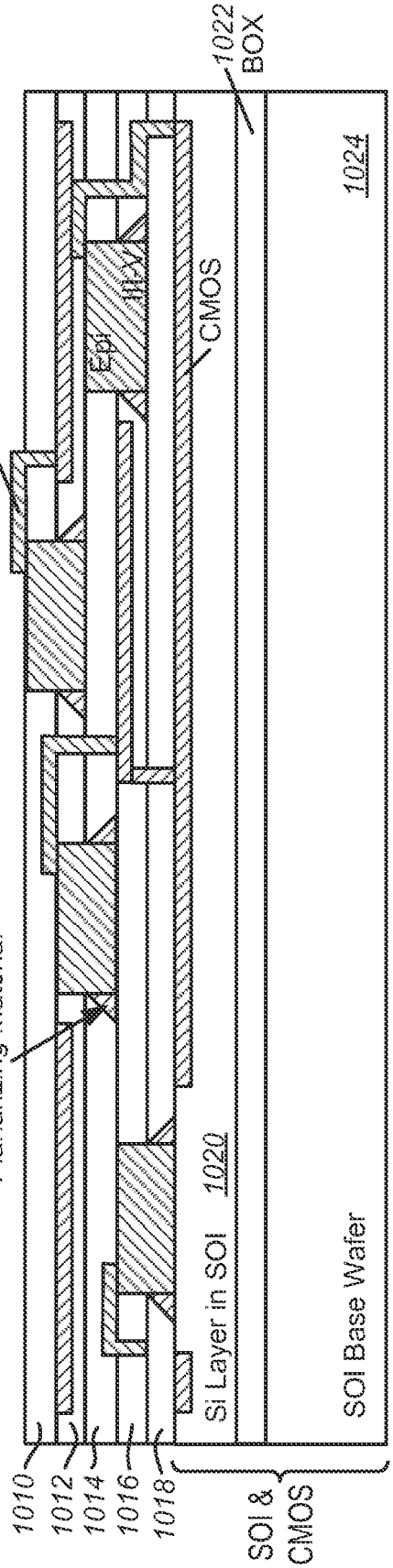

1022
BOX
1024
Electrical Interconnect
Epi
CMOS
Planarizing Material
Si Layer in SOI 1020
SOI Base Wafer
1010
1012
1014
1016
1018
SOI & CMOS

FIG. 10

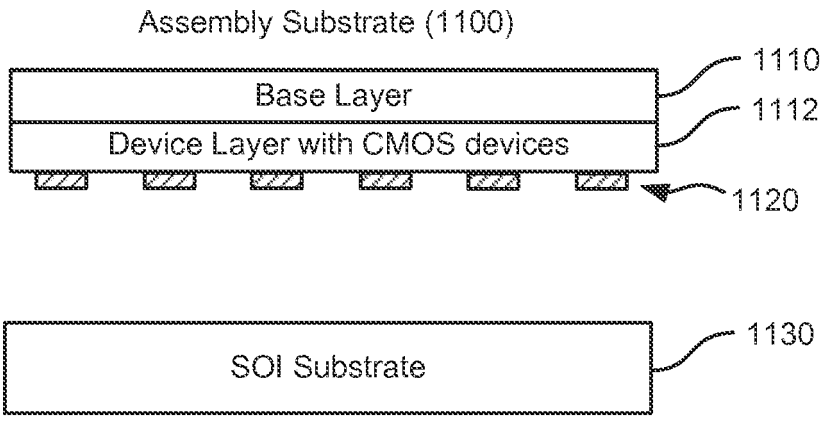


FIG. 11A

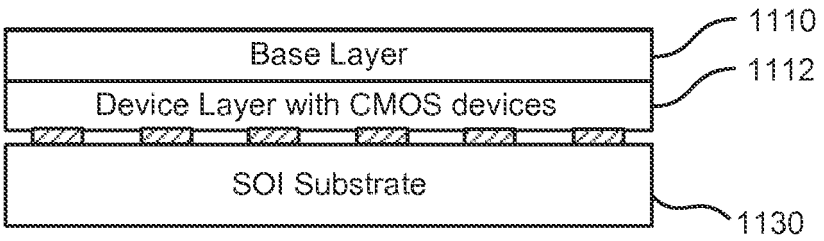


FIG. 11B

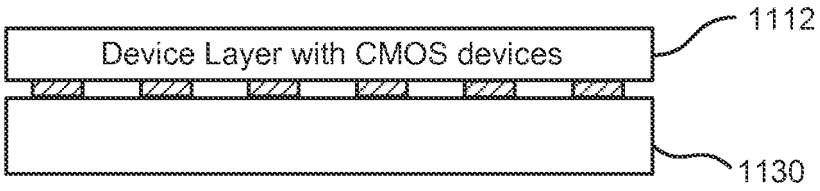


FIG. 11C

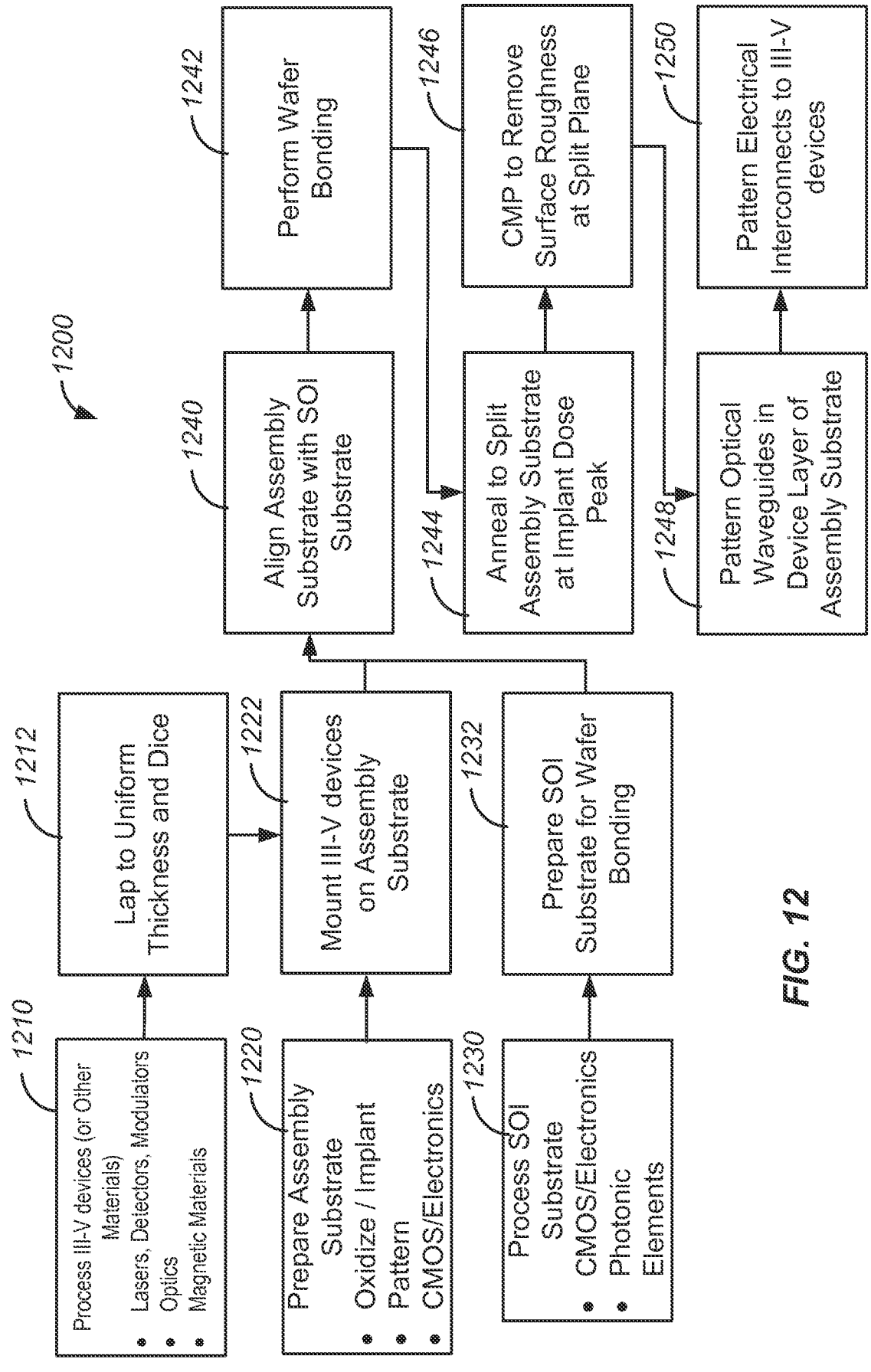

1200
1210
Process III-V devices (or Other Materials)
Lasers, Detectors, Modulators
Optics
Magnetic Materials
1212
Lap to Uniform Thickness and Dice
1220
Prepare Assembly Substrate
Oxidize / Implant
Pattern
CMOS/Electronics
1222
Mount III-V devices on Assembly Substrate
1230
Process SOI Substrate
CMOS/Electronics
Photonic Elements
1232
Prepare SOI Substrate for Wafer Bonding
1240
Align Assembly Substrate with SOI Substrate
1242
Perform Wafer Bonding
1244
Anneal to Split Assembly Substrate at Implant Dose Peak
1246
CMP to Remove Surface Roughness at Split Plane
1248
Pattern Optical Waveguides in Device Layer of Assembly Substrate
1250
Pattern Electrical Interconnects to III-V devices

FIG. 12

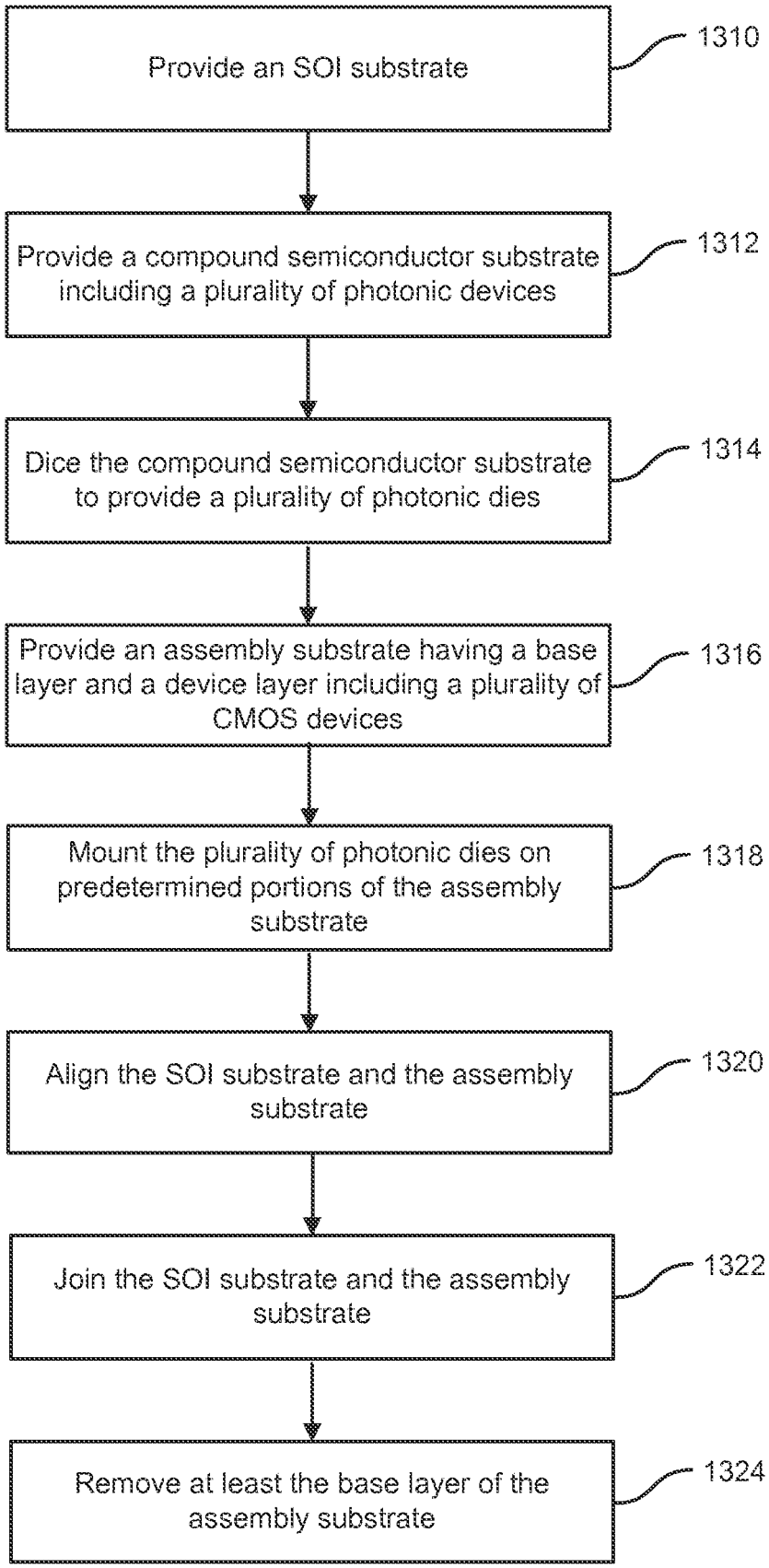

Provide an SOI substrate
1310
Provide a compound semiconductor substrate including a plurality of photonic devices
1312
Dice the compound semiconductor substrate to provide a plurality of photonic dies
1314
Provide an assembly substrate having a base layer and a device layer including a plurality of CMOS devices
1316
Mount the plurality of photonic dies on predetermined portions of the assembly substrate
1318
Align the SOI substrate and the assembly substrate
1320
Join the SOI substrate and the assembly substrate
1322
Remove at least the base layer of the assembly substrate
1324

FIG. 13

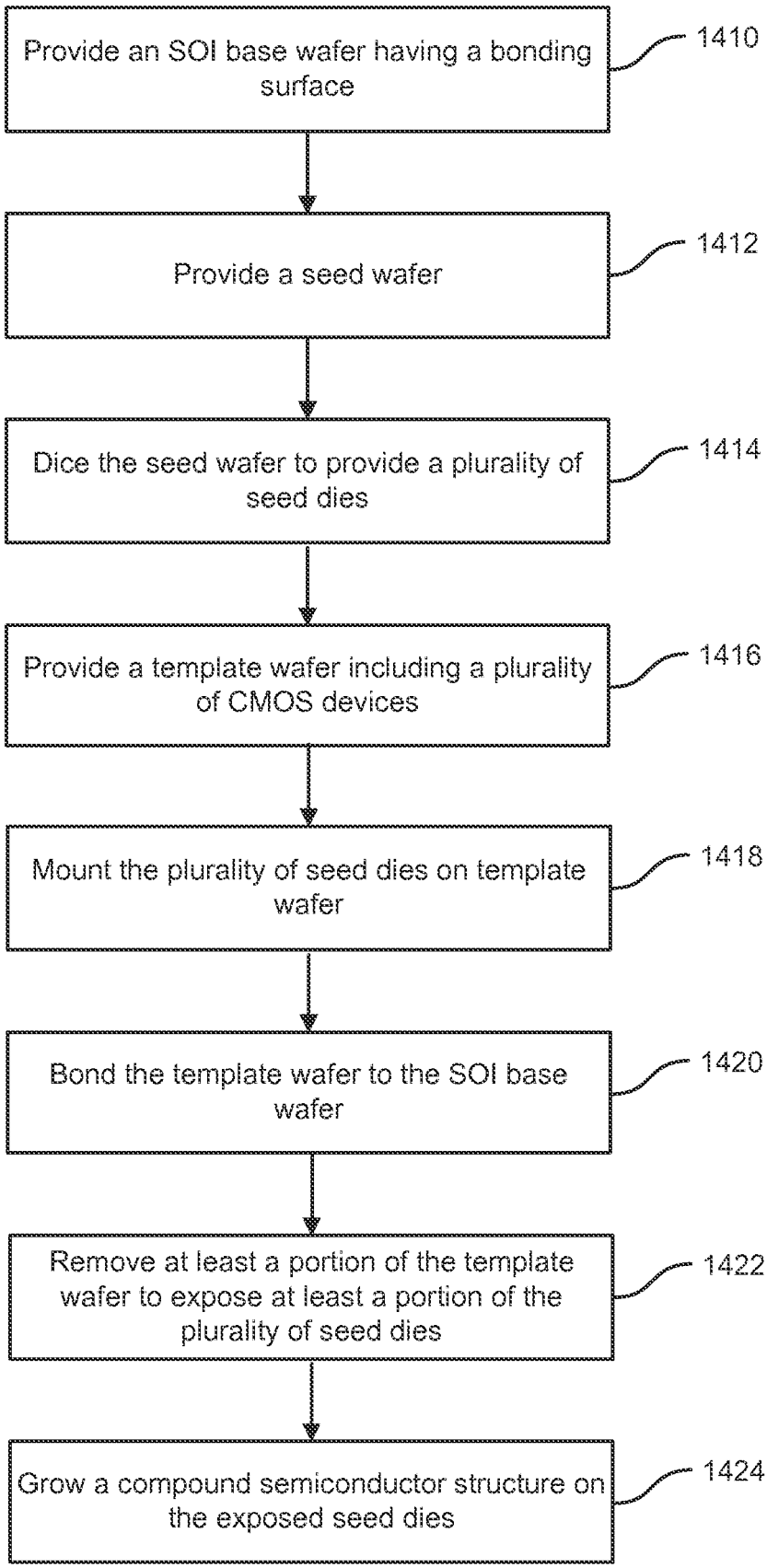

Provide an SOI base wafer having a bonding surface
1410
Provide a seed wafer
1412
Dice the seed wafer to provide a plurality of seed dies
1414
Provide a template wafer including a plurality of CMOS devices
1416
Mount the plurality of seed dies on template wafer
1418
Bond the template wafer to the SOI base wafer
1420
Remove at least a portion of the template wafer to expose at least a portion of the plurality of seed dies
1422
Grow a compound semiconductor structure on the exposed seed dies
1424

FIG. 14