

1 TELEVISION RECEIVER WITH DIGITAL
 SIGNAL PROCESSING HAVING A DIGITAL-TO-
 ANALOG CONVERTER CONTROL CAPABILITY

 This invention relates to television display
5 systems with digital signal processing circuitry that has
 a digital-to-analog control capability.

 In digital television receivers, an analog
baseband video signal is sampled and the samples converted
to representative digital samples by an analog-to-digital
10 converter. The digital samples are processed in a digital
comb filter to produce digital samples representing
separated luminance and chrominance information. The
digital luminance and chrominance information containing
samples are then processed in respective channels of a
15 digital signal processing section. The digital signal
processing section performs functions similar to those
performed by the counterpart analog luminance and
chrominance channels found in conventional television
receivers.

20 Digital-to-analog converters convert the digital
samples produced by the luminance and chrominance channels
to analog signals representing the color image that is to
be displayed. If the analog signals are the Y, I, and Q
signals in an NTSC color system, these analog signals are
25 matrixed to produce the R, G and B signals needed to drive
the cathodes of a color picture tube.

 A feature of the invention is a digital-to-analog
converter arrangement having outputs that may be set
to predetermined voltage levels by a control signal. With
30 such a D/A converter, functions, such as blanking and color
kill, that were previously performed by analog circuitry
can now be expeditiously performed, mainly by the digital
signal processing circuitry, without the need for
additional wiring to circuitry, such as the picture tube
35 drive circuitry, which may be remotely located from the
signal processing section of the television receiver.

In the accompanying drawings:

FIGURE 1 illustrates a television receiver with digital signal processing circuitry that has an analog output signal control capability used for blanking purposes;

FIGURE 2 illustrates a specific embodiment of the digital-to-analog converters in FIGURE 1; and

FIGURE 3 illustrates a portion of the digital signal processing circuitry of FIGURE 1 that includes an analog signal control capability for color kill purposes.

In FIGURE 1 a television signal is received by an antenna 21 and processed by a tuner 22, an intermediate frequency processing circuit 23, and a video detector 24 to produce in a conventional manner a composite video signal at the output of video detector 24. The analog composite video signal is applied to an input of an analog-to-digital (A/D) converter 25. The A/D converter 25 samples the video signal at a rate equal to four times the color subcarrier frequency ($4f_{sc}$), to produce digital samples of the video signal. Each digital sample may comprise, for example, an 8-bit word. The analog video signal will therefore be quantized to one of 256 discrete levels. The $4f_{sc}$ sampling clock signal for A/D converter 25 is developed by a clock generator 27 to enable the A/D converter to sample the analog video signal substantially in phase and frequency synchronism with the color burst signal contained within the video signal.

A sync separator 28 is responsive to the video signal provided by video detector 24 for generating horizontal and vertical sync pulses applied to a deflection unit 33 along signal lines H and V,

1 respectively. Deflection unit 33 generates horizontal and
vertical deflection signals for deflection windings 34 of
a color picture tube 35.

The digitized video signal produced by A/D
5 converter 25 is applied to an input of a digital comb
filter 26 that is clocked at the $4f_{sc}$ rate. Comb filter
26 produces a separated digital luminance signal which is
applied along a data line to a luminance signal processor
32. Luminance processor 32 takes the digitized luminance
10 signal and processes it in accordance with various control
signals inputs, such as a viewer controlled contrast
control not illustrated in FIGURE 1, and produces a
processed luminance signal that is applied to the inputs
of a digital-to-analog (D/A) converter 40c. The luminance
15 signal at the output of D/A converter 40c, now in analog
form, is filtered by a low pass filter 41c to remove the
sampling frequency components, and a processed luminance
signal Y' is applied to an input of a picture tube driver
stage 44.

20 Comb filter 26 also produces a separated digital
chrominance signal which is applied to the input of a
chrominance processor 31. Chrominance processor 31 may
include a chrominance amplifier, not illustrated in
FIGURE 1, that amplifies the chrominance signal in
25 response to viewer controlled color saturation control
signals and a chroma digital peaker, also not illustrated
in FIGURE 1, which modifies the response characteristics
exhibited by the chrominance signal to compensate for any
undesirable response characteristics of the intermediate
30 frequency circuitry 23.

The processed chrominance signals are then
applied to an I-Q demodulator 36. Operation of I-Q
demodulator 36 is synchronized by I and Q clock signals
from clock generator 27 to demodulate the chrominance
35 signal into its baseband digital I and Q color mixture
signal components. The demodulated I signal is applied to
an input of a finite impulse response (FIR) filter 37 and
the demodulated Q signal is applied to the input of a

1 different FIR filter 38. The I filter 37 has a passband
extending from 0 to approximately 1.5 MHz, and the Q
filter has a passband extending from 0 to 0.5 MHz. The I
and Q filters remove high frequency noise that may be
5 contained in the color signals because of the relatively
broad bandwidth of the preceding circuitry of the I and Q
processing channels.

The filtered, digital I and Q signals are
converted to analog signals by D/A converters 40a and 40b,
10 respectively. The analog signals are then filtered by low
pass filters 41a and 41b to remove sampling frequency
components. The resultant I' and Q' signals are applied
to respective input terminals of driver stage 44.

The operation of digital signal processing
15 circuitry thus far described is explained in greater
detail in the U.S. Patent Application Serial No.383,290,
filed May 28, 1982, by H.G.Lewis Jr. (Japanese Patent
Application no. 58-94757 filed May 27 1983).

Driver stage 44 includes an analog color matrix
20 39 of conventional design to which the analog I', Q', and
Y' signals are applied through respective buffers 42a-42c
to develop the conventional RGB signals representing red,
green and blue picture information. The RGB signals are
amplified by driver amplifiers 43 and coupled to the
25 various cathode electrodes of an image display device,
such as a picture tube 35, to produce a display of the
color picture information contained in the composite
video signal.

Each of the digital-to-analog converters 40a,
30 40b, 40c is capable of having its output signal level
established at a predetermined level
upon receipt of a control signal. Such a capability
permits, for example, horizontal and vertical blanking of
the screen of color picture tube 35 using digital
35 techniques rather than the conventional technique of an
analog input signal to the driver stage 44.

As illustrated in FIGURE 1, sync separator 28
develops a composite sync signal that is applied to a

1 blanking pulse generator 29 which develops along a signal
line BL blanking pulses of duration equal to the
horizontal and vertical blanking intervals.

The blanking pulses on signal line BL are
5 applied through respective pulse delay circuits 30a, 30b,
30c to the reset input terminals of respective D/A
converters 40a, 40b, 40c. Upon receipt of the
negative-going edge of the blanking pulses at their reset
terminals, D/A converters 40a, 40b and 40c, establish
10 their output voltages at predetermined levels for the
duration of the pulse. For example, if the output range
of the D/A converter is between 0 volts and -1 volt,
resetting the D/A converter will result in the output
voltage being maintained at, for example, the 0 volt
15 level.

With the output levels of the three D/A
converters 40a, 40b and 40c during the horizontal and
vertical blanking intervals being maintained at 0 volts,
the analog voltages I', Q', and Y' are also set to the 0
20 volt level. Buffer stages 42a, 42b, 42c are designed so
that a 0 volt input to each, when appropriately level
shifted and inverted, produces voltages on signal lines R,
G and B that cut off the driver amplifiers in driver
amplifier circuit 43 to produce cutoff of the cathode
25 electrodes in color picture tube 35. The cutoff of the
cathode electrodes produces a blank screen for the
duration of the horizontal or vertical blanking

Providing for blanking in the manner just
indicated is advantageous in that it may be desirable to
30 provide a blanking capability near the end of the digital
signal processing chain rather than near the beginning,
such as at a point near the operation of A/D converter 25.
If blanking information is introduced into the luminance
and chrominance digital signals early in the processing
35 chain, processing circuitry further along may erroneously
change these digital signal to ones that are incapable of
producing correct blanking levels for the Y', Q', and I'
analog signals.

1 Delay circuits 30a-30c are provided to enable
the blanking signal levels to be developed substantially
simultaneously on the I', Q' and Y' output lines. Because
the luminance and color mixing information I, Q and Y are
5 processed in different data channels, the processing
delays introduced by the different channels will differ
for the I, Q and Y information. Furthermore, because the
bandwidth for the I', Q' and Y' signals differ from about
4.5 MHz for the Y' signal to about 0.5 MHz for the Q'
10 signal, the group delays introduced by low pass filters
41a-41c differ. The delay circuits 30a-30c are designed
to take all these delays into account so as to initiate
the blanking portion of the I', Q' and Y' output signals
at substantially the same time.

15 An example of a D/A converter with reset
capability suitable for the D/A converters
40a-40c is the 10-input bit D/A converter manufactured
by TRW Corporation, Redondo Beach, California, model TDC
1016J. In the TTL input mode of operation, this D/A
20 converter may be used so that pin 11 is the functional
equivalent of the reset input terminal of FIGURE 1.

 Alternatively, the D/A converter 400 illustrated
in FIGURE 2 may be used as any one of the D/A converters
40a-40c of FIGURE 1. D/A converter 400 is an 8-bit
25 converter, since the digital signal processing circuit of
FIGURE 1 requires the quantization of composite video
signal to no more than 256 levels. To keep the signal to
noise ratio high, D/A converter 400 is run in the zero
hold mode by using eight data type flip-flops 50. Each of
30 the input bits 2^0 - 2^7 of the corresponding digital output
sample is applied to a respective D input terminal of a
respective one of D-type flip-flops 50. The 8-bit data is
strobed into the D flip-flops upon receipt of a clock
pulse from clock generator 27 of FIGURE 1 along a CLOCK
35 signal line that is coupled to each of the clock input
terminals of flip-flops 50. The Q output terminals of the
flip-flops 50, representative of the received data, are
coupled to a respective one of eight switched current

1 sources 51. The outputs of switched current sources 51
are coupled to a summing network 52, such as a
conventional R2R ladder, to produce an analog output
voltage whose value is a function of the digitized signal
5 level represented by the 8-bits 2^0-2^7 .

The negative-going horizontal and vertical
blanking pulses after suitable delay are applied along a
RESET line of FIGURE 2 to the reset input terminals R of
the D flip-flops 50 to produce a logical 0 output state at
10 each of the Q output terminals. A logical 0 at each of
the Q output terminals produces at the output of the
ladder network 52 a substantially zero analog output
voltage. The zero analog output voltage for D/A converter
400 results in zero I', Q', Y' voltages at the outputs of
15 low pass filters 41a-41c.

Other types of D flip-flops may be used in D/A
converter 400 of FIGURE 2. For example, D flip-flops
having output enable terminals rather than reset terminals
may be used. The blanking pulses are then applied to the
20 output enable terminals to keep the Q outputs low during
the blanking pulse interval.

FIGURE 3 illustrates a portion of the circuitry of
FIGURE 1 of use when a color kill capability is provided
when using a digital-to-analog converter having a reset
25 capability. Elements of FIGURES 1 and 3 identified the
same, function in a similar manner. In FIGURE 3 the
blanking signal line BL is directly connected to the delay
circuit 30c that is interposed between blanking generator
29 and the reset input terminal R of the luminance channel
D/A converter 40c. Blanking line BL is also directly
30 connected to an input terminal of an AND gate 45. At the
other input terminal of AND gate 45 there is applied a
color kill signal K obtained from conventional analog
circuitry or from the color kill circuitry of the digital
35 signal processing portion of the television receiver. In
a digital signal processing system, the color kill signal
K may be derived in the chrominance processor 31 of FIGURE

1 in the manner described in application number
8307377 filed 17 March 1983 entitled DIGITAL
TELEVISION RECEIVER AUTOMATIC CHROMA CONTROL SYSTEM.
Color kill signal K remains in its low state as long
5 as it is desired to display only luminance information.

The output terminal of AND gate 45 is connected
through pulse delay circuits 30a and 30b to the respective
~~input terminals of delay circuits 40a and 40b that are in~~
~~turn coupled to the~~ reset terminals R of the I D/A
10 converter 40a and the Q D/A converter 40b. Thus, upon the
occurrence of the negative-going color kill signal K the
output of AND gate 45 goes low resulting in the resetting
of D/A converters 40a and 40b resulting in a zero output
voltage level for the I' and Q' signals. Only the
15 luminance information is applied to driver stage 44 to
produce a black and white picture display.

1 CLAIMS

1. A television display apparatus having a digital signal processing system for producing an analog output signal from digital information signals to obtain a drive
5 for an image display device, said digital signal processing system comprising: means for supplying digital samples containing image information including a luminance processor for generating a plurality of luminance information representative digital samples and a color
10 processor for generating a plurality of color information representative digital samples; a digital-to-analog converter arrangement responsive to said digital samples for producing at least one analog output signal containing color information of said image information and
15 another analog output signal containing luminance information of said image information; means responsive to said analog output signals for developing said drive to generate a display of said image; and a color kill circuit, comprising:

20 means for developing a color kill control signal and coupling it to said digital-to-analog converter arrangement for establishing said color analog output signal at a predetermined level that results in the removal of color information from said display.

25 2. Apparatus as claimed in claim 1 wherein said image information is contained in picture intervals occurring between second intervals within which said display is to be blanked, and wherein said apparatus further includes means for developing a blanking control
30 signal and coupling it to said digital-to-analog converter arrangement for establishing said analog output signals at levels that result in the production of a blank display.

3. Apparatus as claimed in claim 1 or 2 wherein
35 said digital-to-analog converter arrangement includes a plurality of _____



1 latches each latch having applied to an input terminal
thereof a corresponding bit from an associated digital
sample, a summing network coupled to output terminals
of said plurality of latches for developing an analog
5 output signal, the magnitude of which is represented
in binary form by said associated digital sample, and
a signal line, coupled to a terminal of each of said
plurality of latches, responsive to a said control signal
for producing a predetermined logical state at each of
10 said output terminals independent of the state of said
digital sample at the time of said control signal.

4. Apparatus as claimed in any preceding claim
wherein said color processor develops first and second
bit groups representative of first and second color
15 mixing information respectively, said digital-to-analog
converter arrangement developing two color analog
output signals representative of said first and second
color mixing information respectively, said color kill
control signal, when developed, resulting in said two
20 color analog output signals being placed in those states
that will result in a display containing only luminance
information.

5. Apparatus as claim in claim 4 wherein said
digital-to-analog converter arrangement develops said
25 other analog output signal representative only of said
luminance information and is responsive to a blanking
control signal for placing the three analog output
signals in those states that will result in a blank
display.

30 6. Television display apparatus substantially as
hereinbefore described with reference to FIGURE 3 of
the accompanying drawings..

