Claims:

1. A method for processing a substrate, comprising:

depositing a sacrificial structure layer on the substrate, wherein the substrate is a doped or undoped silicon wafer or a sapphire;

depositing a photoresist on the sacrificial structure layer;

patterning the photoresist to produce a crude photoresist profile on the sacrificial structure layer;

trimming the photoresist with a plasma to produce a refined photoresist profile covering a first portion of the sacrificial structure layer while a second portion of the sacrificial structure layer is exposed, wherein the refined photoresist profile has a line width roughness of about 10 Å to about 20 Å and a line edge roughness about 10 Å to about 20 Å;

etching the second portion of the sacrificial structure layer to form patterned features disposed on the substrate;

depositing a dielectric layer on upper surfaces and side surfaces of the patterned features and on and in contact with an upper surface of the substrate, wherein trimming the photoresist and depositing the dielectric layer occur in the same processing chamber;

anisotropically etching a portion of the dielectric layer, comprising:

removing the dielectric layer on the upper surfaces of the patterned features;

removing the dielectric layer on the upper surface of the substrate; and

leaving at least a portion of the dielectric material on the side surfaces, wherein the portion of the dielectric material on the side surfaces forms sidewall spacers disposed on the upper surface of the substrate; and

removing the patterned features while leaving the sidewall spacers disposed across and in contact with the upper surface of the substrate.

2. The method of claim 1, wherein the refined photoresist profile contains sidewall surfaces with smoother or less wavy surfaces than sidewall surfaces of the crude photoresist profile.

3. The method of claim 1, wherein trimming the photoresist further comprises modulating a critical dimension for the patterned features or the subsequently deposited dielectric layer.

4. The method of claim 1, wherein the dielectric layer comprises silicon oxide, silicon oxynitride, or silicon nitride.

5. The method of claim 4, wherein the–dielectric layer is doped with carbon or hydrogen.

6. The method of claim 1, wherein the processing chamber is a plasma-enhanced chemical vapor deposition chamber.

7. The method of claim 1, wherein the plasma is a capacitively coupled plasma (CCP) or an inductively coupled plasma (ICP), and wherein the dielectric layer is a carbon-based material comprising amorphous carbon.

8. The method of claim 1, wherein the plasma is generated with a frequency in a range from about 100 kHz to about 2.4 GHz and a power in a range from about 10 watt to about 1,000 watt.

9. The method of claim 1, wherein the plasma is generated in a processing chamber having a pressure in a range from about 10 mTorr to about 50 Torr.

10. The method of claim 1, wherein trimming the photoresist further comprises exposing the photoresist to a process gas comprising hydrogen (H_2), ammonia, nitrous oxide, oxygen (O_2), a hydrocarbon, nitrogen trifluoride, chlorine (Cl_2), nitrogen (N_2), carbon dioxide, carbon monoxide, water, ions thereof, plasmas thereof, or any combination thereof.

11. The method of claim 1, further comprising removing the photoresist from the patterned features before depositing the dielectric layer on the patterned features.

12. A method for processing a substrate, comprising:

depositing a sacrificial structure layer on the substrate, wherein the substrate is a doped or undoped silicon wafer or a sapphire;

depositing a photoresist on the sacrificial structure layer;

patterning the photoresist to produce a crude photoresist profile on the sacrificial structure layer;

trimming the photoresist with a plasma to produce a refined photoresist profile covering a first portion of the sacrificial structure layer while a second portion of the sacrificial structure layer is exposed, wherein the refined photoresist profile contains sidewall surfaces with smoother or less wavy surfaces than sidewall surfaces of the crude photoresist profile;

etching the second portion of the sacrificial structure layer to form patterned features disposed on the substrate;

depositing a dielectric layer on upper surfaces and side surfaces of the patterned features and on and in contact with an upper surface of the substrate, wherein trimming the photoresist and depositing the dielectric layer occur in the same processing chamber;

anisotropically etching a portion of the dielectric layer, comprising:

removing the dielectric layer on the upper surfaces of the patterned features;

removing the dielectric layer on the upper surface of the substrate; and

leaving at least a portion of the dielectric material on the side surfaces, wherein the portion of the dielectric material on the side surfaces forms sidewall spacers disposed on the upper surface of the substrate; and

removing the patterned features while leaving the sidewall spacers disposed across and in contact with the upper surface of the substrate.

13. The method of claim 12, wherein the refined photoresist profile has a line width roughness of about 10 Å to about 20 Å.

14. The method of claim 12, wherein trimming the photoresist further comprises modulating a critical dimension for the subsequently deposited dielectric layer.

15. The method of claim 12, wherein the processing chamber is a plasma-enhanced chemical vapor deposition chamber.

16. The method of claim 12, wherein the plasma is a capacitively coupled plasma (CCP) or an inductively coupled plasma (ICP).

17. The method of claim 12, wherein the plasma is generated with a frequency in a range from about 100 kHz to about 2.4 GHz and a power in a range from about 10 watt to about 1,000 watt.

18. The method of claim 12, wherein the plasma is generated in a processing chamber having a pressure in a range from about 10 mTorr to about 50 Torr.

19. The method of claim 12, wherein trimming the photoresist further comprises exposing the photoresist to a process gas comprising hydrogen (H_2), ammonia, nitrous oxide, oxygen (O_2), a hydrocarbon, nitrogen trifluoride, chlorine (Cl_2), nitrogen (N_2), carbon dioxide, carbon monoxide, water, ions thereof, plasmas thereof, or any combination thereof.

20. A method for processing a substrate, comprising:

depositing a sacrificial structure layer on the substrate, wherein the substrate is a doped or undoped silicon wafer or a sapphire;

depositing a photoresist on the sacrificial structure layer;

patterning the photoresist to produce a crude photoresist profile on the sacrificial structure layer;

trimming the photoresist with a plasma to produce a refined photoresist profile covering a first portion of the sacrificial structure layer while a second portion of the sacrificial structure layer is exposed, wherein the refined photoresist profile has a line width roughness of about 10 Å to about 20 Å and a line edge roughness of about 10 Å to about 20 Å;

etching the second portion of the sacrificial structure layer to form patterned features disposed on the substrate;

removing the photoresist from the patterned features;

depositing a dielectric layer on upper surfaces and side surfaces of the patterned features and on and in contact with an upper surface of the substrate, wherein the dielectric layer comprises silicon oxide, silicon oxynitride, or silicon nitride, and wherein the dielectric layer is doped with carbon or hydrogen;

anisotropically etching a portion of the dielectric layer, comprising:

removing the dielectric layer on the upper surfaces of the patterned features;

removing the dielectric layer on the upper surface of the substrate; and

leaving at least a portion of the dielectric material on the side surfaces, wherein the portion of the dielectric material on the side surfaces forms sidewall spacers disposed on the upper surface of the substrate; and

removing the patterned features while leaving the sidewall spacers disposed across and in contact with the upper surface of the substrate.