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(54) Title: METHOD FOR REDUCING THE RANGE IN RESISTIVITIES OF SEMICONDUCTOR CRYSTALLINE SHEETS GROWN IN A MULTI-LANE FURNACE

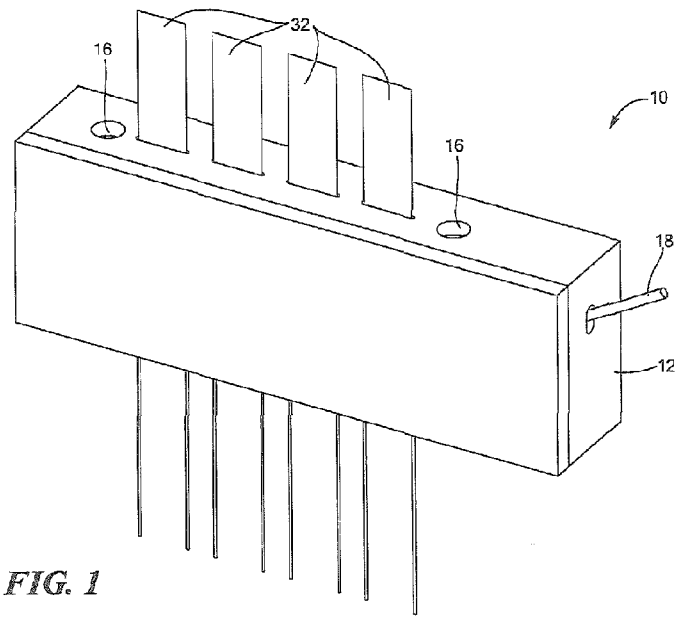


FIG. 1

(57) Abstract: A method for reducing the range in resistivities of semiconductor crystalline sheets produced in a multi-lane growth furnace. A furnace for growing crystalline sheets is provided that includes a crucible with a material introduction region and a crystal growth region including a plurality of crystal sheet growth lanes. The crucible is configured to produce a generally one directional flow of material from the material introduction region toward the crystal sheet growth lane farthest from the material introduction region. Silicon doped with both a p-type dopant and an n-type dopant in greater than trace amounts is introduced into the material introduction region. The doped silicon forms a molten substance in the crucible called a melt. Crystalline sheets are formed from the melt at each growth lane in the crystal growth region. Co-doping the silicon feedstock can reduce the variation in resistivities among the crystalline sheets formed in each lane.

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