CLAIMS

1. A method of plating a metal on an electronic substrate, wherein the electronic substrate comprises one or more features, wherein the one or more features comprise one of one or more through-holes and/or one or more blind micro-vias in the electronic substrate, the method comprising the steps of:

a) preparing the electronic substrate to receive metal plating thereon;

b) bringing the electronic substrate and at least one counter electrode into contact with an electroplating solution comprising a source of metal ions of the metal to be plated;

c) electrically polarizing first and second sides of the electronic substrate to initiate metal plating thereon, wherein the electroplating solution plates the one or more through-holes and/or the one or more blind micro-vias using a plating cycle until metallization is complete;

wherein the plating cycle comprising the steps of, in order:

1) pulse plating for a first time period on a first side and a second side of the electronic substrate to cause metal to preferentially plate in the center of the one or more through-holes, wherein the metal merges together in the center of the one or more through-holes to form two opposing blind vias; and
2) direct plating for a second time period to fill the two opposing blind vias formed by pulse plating;

wherein the pulse plating step comprises applying an electrical current to electrodeposit metal from the electroplating solution to the first side and second side of the electronic substrate, wherein the electrical current is applied as a pulse plating cycle comprising a repeatable sequence, wherein the repeatable sequence comprises a set of pulse plating periods, each set of pulse plating periods including, in any order:

(i) at least a first forward pulse period;

(ii) at least a first reverse pulse period;

(iii) at least a second forward pulse period; and

(iv) optionally, at least one rest period,

wherein pulse breaks are interposed between at least one of the pulse plating periods in the set of pulse plating periods, preferably wherein pulse breaks are interposed between at least some of the pulse plating periods in the set of pulse plating periods, most preferably wherein pulse breaks are interposed between each of the pulse plating periods in the set of pulse plating periods.

2. The method according to claim 1, wherein the electroplating solution is an acid copper plating bath comprising a source of copper ions.

3. The method according to claim 1 or claim 2, wherein the same electroplating solution is used for the pulse plating step and the direct plating step.

4. The method according to claim 3, wherein the pulse plating step and the direct plating steps are performed in separate tanks.

5. The method according to claim 1 or claim 2, wherein the electroplating solutions used in the pulse plating step and the direct plating step are different from each other.

6. The method according to any of claims 1 to 5, wherein the metallized electroplated metal deposit completely fills the one or more through-holes and/or the one or more blind micro-vias and deposits a conformal metal deposit on the electronic substrate.

7. The method according to claim 2, wherein the acid copper electroplating bath is maintained at a temperature of between about 15 and about 45°C.

8. The method according to any of claims 1 to 5, further comprising the step of direct current plating using forward current for a time period prior to step 1), wherein direct current plating for the first time period deposits a flash copper layer on the surfaces of the one or through-holes and/or one or more blind micro-vias.

9. The method according to any of claims 1 to 5, wherein the electronic substrate is contacted with the metal electroplating solution by immersing the electronic substrate in the electroplating solution.

10. The method according to claim 1, wherein each set of pulse plating periods consists of, in any order:

a) a first forward pulse of a first forward duration and first forward intensity;

b) a second forward pulse of a second forward duration and second forward intensity;

c) a third forward pulse, the third forward pulse having at least substantially the same duration and/or intensity as the first forward pulse, preferably having the same duration and intensity as the first forward pulse;

d) a first reverse pulse of a first reverse duration and first reverse intensity;

e) a fourth forward pulse, the fourth forward pulse having at least substantially the same duration and/or intensity as the first forward pulse,

f) a fifth forward pulse, the fifth forward pulse having a different forward duration and/or a different forward intensity from at least one of the first forward pulse and the second forward pulse; and

g) a sixth forward pulse, the sixth forward pulse having at least substantially the same duration and/or intensity as the first forward pulse; and

wherein a pulse break is interposed after one or more of steps a) to g), preferably wherein a pulse break is interposed after each of steps a) to g).

11. The method according to any of claims 1 to 5 and 10, wherein the pulse plating cycle comprising the repeatable sequence applied to the first side of the electronic substrate is the same as the pulse plating cycle comprising the repeatable sequence applied to the second side of the electronic substrate.

12. The method according to any of claims 1 to 5 and 10, wherein the pulse plating cycle comprising the repeatable sequence applied to the first side of the electronic substrate is different from the pulse plating cycle comprising the repeatable sequence applied to the second side of the electronic substrate.

13. The method according to any of claims 1-5 and 10-12, wherein pulse breaks in the first set of pulse plating periods applied to the first side of the electronic substrate are synchronous with the pulse breaks in the second set of pulse plating periods applied to the second side of the electronic substrate.

14. The method according to any of claims 1-5 and 10-13, wherein one or more forward pulses having the same duration and intensity as first forward pulse on the first side of the electronic substrate and the second side of the substrate line up with each other, even if the set repeatable sequence comprising the set of pulse plating periods applied to the first side of the substrate is different from the repeatable sequence comprising the set of pulse plating periods applied to the second side of the electronic substrate.

15. The method according to any of claims 1 to 5 and 10-14, wherein each repeatable sequence comprising the set of pulse plating periods has a duration of between about 0.5 and about 5 seconds.

16. The method according to claim 15, wherein each repeatable sequence has a duration of 1 second.

17. The method according to any of claims 1 to 15 and 10-16, wherein the repeatable sequence comprises a plurality of two or more repeatable sequences arranged in a repeating series.

18. The method according to claim 10, wherein the pulse plating cycle is an asynchronous plating cycle, wherein the repeatable sequence applied to the first side of the electronic substrate is the same as the repeatable sequence applied to the second side of the electronic substrate, except in reverse order.

19. The method according to claim 1 or 10, further comprising a longer duration rest period included in the repeatable sequence comprising the set of pulse plating periods, wherein the longer duration rest period on one side of the electronic substrate coincides with a forward pulse on the opposite side of the electronic substrate, wherein the longer duration rest period and the forward pulse have at least substantially the same duration.

20. The method according to claim 14, wherein after the asynschronous plating cycle is performed for a period of time, a second pulse plating cycle with synchronous waveforms on the first side and the second side of the electronic substrate is applied,

wherein the asynchronous plating cycle preferentially plates the copper in the center of the one or more through-holes such that the copper merges together in the center of the one or more through-holes to form two opposing blind vias and the second pulse plating cycle shapes

the thus formed two opposing blind vias to allow for more uniform plating of the one or more through-holes.

21. The method according to claim 20, wherein the second pulse plating cycle uses a reverse/forward ratio of between about 1:1 to 4:1 and wherein the duration of forward pulses is in the range of about 10 to 150 ms and the duration of the reverse pulses is in the range of about 0.5 to 10 ms.

22. The method according to any of claims 1-5 and 10-21, wherein the duration of each first forward pulse period and second forward pulse period is independently in the range of about 80 to 250 ms, the duration of each reverse pulse period is in the range of about 50 to about 150 ms, and the duration of each pulse break is in the range of about 1 to about 50 ms.

23. An electronic substrate comprising one or more features metallized by the process of any of claims 1-5 and 10-21.

24. A printed circuit board, wherein the printed circuit board comprises:

a metallized panel in which one or more through-holes are formed;

wherein the printed circuit board comprises a conductive seed layer thereon to initiate electroplating of copper;

wherein one or more through-hole comprises:

a) a first copper plating layer in the center of the one or more through-holes, wherein the copper mergers together in the center of the one or more through-hole to form two opposing blind vias;
b) optionally, a second copper plating layer deposited over the first copper plating layer, wherein the optional second copper plating layer shapes the blind vias formed by the first copper plating layer; and
c) a copper filling layer, wherein the copper filling layer is deposited over the first copper plating layer and the optional second copper plating layer to fill the one or more through-holes;

wherein the one or more through-holes are completely filled with copper, without any voids, dimples or other defects.

25. The printed circuit board according to claim 24, wherein all of layers a) to c) are present.

26. The printed circuit board according to claim 24 or claim 25, wherein the first copper layer, optional second copper layer, and copper filling layer are applied using the same acid copper plating electrolyte.

27. The printed circuit board according to claim 24 or claim 25, wherein the first copper layer and the copper filling layer are applied using different acid copper plating electrolytes.