SILICON WAFER AND METHOD OF MANUFACTURING THE SAME

DESCRIPTION

TECHNICAL FIELD

[0001]

The present invention relates to a silicon wafer and a method of manufacturing the same which can suppress occurrences of slip dislocation and warpage in the field of a semiconductor wafer manufacturing technique, in particular, in a device manufacturing process.

BACKGROUND ART

[0002]

A silicon wafer used as a substrate of a semiconductor device or the like is manufactured by slicing a silicon single-crystal ingot and performing a heat treatment, mirror-like finishing, and the like. As a method of manufacturing a silicon single-crystal ingot, for example, a Czochralski method (to be referred to as a CZ method hereinafter) is given. The CZ method occupies a large part of manufacturing of a silicon single-crystal ingot because a large-diameter single-crystal ingot can be easily obtained and defect can be relatively easily controlled.

[0003]

In a silicon single crystal (to be referred to as "CZ-Si" hereinafter) pulled up by the CZ method, a crystal defect called a grown-in defect is present. The CZ-Si

includes oxygen between lattices in an oversaturated state. However, the oversaturated oxygen causes a microscopic defect called a Bulk Micro Defect (to be referred to as a "BMD" hereinafter) by a heat treatment (annealing) performed later.

[0004]

In order to form a semiconductor device in a silicon wafer, a crystal defect is required not to be present in a semiconductor device forming region. When a crystal defect is present on a surface for forming a circuit, the defective portion causes a circuit breakdown or the like. On the other hand, an appropriate number of BMDs are required to be present in the silicon wafer. This is because the BMDs function to getter a metal impurity or the like which causes a semiconductor device malfunction.

[0005]

In order to satisfy the above request, a method which performs high-temperature annealing to the silicon wafer to induce the BMD in the silicon wafer to form an Intrinsic Gettering layer (to be referred to as an "IG layer" hereinafter), eliminates a grown-in defect being present on the surface of the silicon wafer, and forms a Denuded Zone (to be referred to as a "DZ layer" hereinafter) layer having an extremely small number of crystal defects is used.

[0006]

As a concrete example, a method (Patent Document 1) which performs high-temperature annealing to a nitrogen-

containing substrate to reduce grown-in defects on the surface and forms BMDs having nitrogen as cores in the substrate, is proposed.

[0007]

However, the DZ layer formed on the upper and lower surfaces of the silicon wafer by the high-temperature annealing process has an oxygen concentration which is extremely low because of outward diffusion of oxygen during heat treatment. As a result, prohibitive power of dislocation defect extension on the upper and lower surfaces of the wafer is extreamly low. For this reason, due to micro-scratches on the upper and lower surfaces caused in the annealing step, dislocation defects (to be referred to as "slip" hereinafter) easily extends in a bulk. The extension of the slip dislocation undesirably decreases the strength of the silicon wafer. For example, when a wafer is annealed while being supported by a heat treatment port or the like, a slip dislocation frequently extends from a supported portion on a peripheral portion on the lower surface of the wafer. The slip dislocation may extend from a silicon wafer edge.

[0008]

When the strength of the silicon wafer is deteriorated, the wafer may be damaged during the manufacturing steps, or the wafer may be broken down. However, the DZ layer is indispensable to manufacturing of a semiconductor device.

A silicon wafer having a DZ layer and an excellent strength characteristic is desired.

[0009]

In the conventional technique described in the Patent Document 1, deterioration of strength of a silicon wafer is not considered. A silicon wafer formed by the above method cannot avoid extension of slip dislocation.

[0010]

On the other hand, in order to prevent occurrence of the slip dislocation, a method which generate BMDs at a high concentration is also proposed.

[0011]

More specifically, a silicon wafer manufacturing method in which a rapid heat raising/falling temperature heat treatment is performed to a substrate cut out of a silicon single-crystal ingot in an atmosphere of a gas mixture of a nitrogen gas or an inert gas or an ammonia gas and an inert gas at a temperature of 500°C or more to 1200°C or less for 1 minute or more to 600 minutes or less to form oxygen deposition cores each having a size of 20 nm or less in a BMD layer at a concentration of $1 \times 10^{10}/cm^3$ or more is proposed (Patent Document 2). A silicon wafer manufacturing method in which a heat treatment is performed to a silicon wafer having an oxygen concentration of 1.2×10^{18} atoms/cm^3 to 1.4×10^{18} atoms/cm^3 and a carbon concentration of 0.5×10^{16} atoms/cm^3 to 2×10^{17} atoms/cm^3 in a non-oxidizing atmosphere under the conditions: a

temperature of 1100°C to 1250°C; 1 hour to 5 hours; and a temperature raising rate of 0.1 to 1°C/minute in a temperature range of 1100°C to 1250°C to form BMDs each having a size of 150 nm or less at a concentration of 5 x $10^9/cm^3$ or more is proposed(Patent Document 3). A silicon wafer in which a heat treatment is repeated several times to generate BMDs at a high concentration (1 x $10^{10}/cm^3$ to 1 x $10^{12}/cm^3$) is proposed (Patent Document 4). Furthermore, a silicon wafer in which BMDs each of which is located at a position having a depth of 50 μm from a surface and has a size of 10 nm or more to 50 nm or less are formed at a concentration of 5 x $10^{11}/cm^3$ to suppress slip and warpage is also proposed (Patent Document 5).

[Patent Document 1] Japanese Unexamined Patent Application Publication No. 10-98047

[Patent Document 2] Japanese Unexamined Patent Application Publication No. 2006-40980

[Patent Document 3] Japanese Unexamined Patent Application Publication No. 2006-269896

[Patent Document 4] Japanese Unexamined Patent Application Publication No. 08-213403

[Patent Document 5] Japanese Unexamined Patent Application Publication No. 2008-160069

DISCLOSURE OF THE INVENTION

[Problem to be Solved by the Invention]

[0012]

However, in recent years, when a silicon wafer increases in diameter, and when an integration density of semiconductor device patterns increases, in addition to occurrence of slip dislocation, warpage occurring in a wafer becomes problematic.

[0013]

As heat treatment furnaces, a batch type heat treatment furnace and an RTA are known. Slip is brought from a contact between the lower surface of a silicon wafer edge and a silicon wafer holding portion or a silicon wafer edge portion. The brought slip extends in [110] direction, and, depending on circumstances, the silicon wafer may be damaged or broken down. Warpage is a phenomenon in which a silicon wafer is deformed by thermal distortion in a heat treatment. A warpage of a silicon wafer before a heat treatment to give desired characteristics is performed is suppressed to 10 μm or less. However, the heat treatment is performed, a level difference between a peak and a trough reaches several ten micromillimeters. A semiconductor device pattern cannot be exposed on a wafer surface correctly to cause a decrease in yield of semiconductor devices.

[0014]

The problem of the warpage is conspicuous when a wafer diameter is 200 mm or more. In particular, a problem caused by a warpage in a batch type heat treatment cannot be solved without giving attention to a BMD concentration

and a size of a surface layer. As described above, even though BMDs are merely regulated to be formed at a position having a depth of 50 μm or more and to have small sizes, the problem cannot be avoided.

[0015]

A problem to be solved by the invention is to provide a method of manufacturing a silicon wafer which has a DZ layer having an appropriate area and controls a BMD concentration which can suppress occurrences of slip dislocation and warpage in device manufacturing processes.

[Means for Solving the Problem]

[0016]

The present inventors perform faithful research to solve the problem. As a result, the present inventors obtained the following knowledge to get the present invention. That is, of BMDs immediately under a DZ layer, BMDs each having a size of 200 μm or more are controlled at a concentration of $2 \times 10^9/cm^3$ or less in a bulk having a depth of 50 μm or more, and BMDs each having a size of 10 nm or more to 50 nm or less are controlled to a density of $1 \times 10^{12}/cm^3$ or more, so that occurrences of slip and warpage caused by a batch type heat treatment furnace in device manufacturing processes can be suppressed.

[0017]

In a batch type heat treatment, a temperature difference between a wafer peripheral portion and wafer central portion increases. As a result, stress which

deforms the wafer into a convex shape or a concave shape acts. The stress acting at this time is zero at a center of thickness and increases toward a portion near the surface of the wafer. On the other hand, as a cause of warpage, dislocation occurring from a BMD is given. When the size of the BMD is large, dislocation easily occurs. Therefore, when a BMD having a large size is present near a surface of a wafer having large stress, dislocation occurs from the BMD, and the wafer is easily warped. The present inventors found that control of a concentration and a size of BMDs being present at a relatively deep position (position having a depth of 50 μm or more) in a wafer was not important to improvement of a warpage characteristic, rather than control of a concentration and a size of BMD near a surface layer (position having a depth of 20 μm or less) was very effective to improve the warpage characteristic. Any one of the conventional techniques described in conventional documents 1 to 5 does not refer to control of a concentration and a size of BMDs located at a position shallower than a surface by 20 μm or less. For this reason, in the conventional techniques, a wafer warpage characteristic in a batch type heat treatment cannot be improved.

[0018]

More specifically, the present invention relates to a silicon wafer which deposits BMDs at a high concentration in a bulk to suppress slip dislocation and decreases sizes

of BMDs near a surface layer where maximum heat stress is generated in a batch type heat treatment to suppress warpage and a method of manufacturing the silicon wafer. The present invention includes the following aspect(s) / embodiment(s).

[0019]

(1) A silicon wafer having a nitrogen concentration which is 5 x 10^{14} atoms/cm^3 or more to 1 x 10^{16} atoms/cm^3 or less, having a carbon concentration which is 1 x 10^{15} atoms/cm^3 or more to 8.1 x 10^{15} atoms/cm^3 or less, and having BMDs each having an octahedon shape,

characterized in that BMDs each of which is located at a position shallower than the silicon wafer surface by a depth of less than 20 μm and has a diagonal length of 200 nm or more has a concentration of not more than 2 x $10^9/cm^3$, and BMDs each of which is located at a position having a depth of more than 50 μm and has a diagonal length of 10 nm or more to 50 nm or less has a concentration of 1 x $10^{12}/cm^3$ or more.

[0020]

(2) A method of manufacturing the silicon wafer described in the (1), characterized in that

a nitrogen concentration of a substrate is 5 x 10^{14} atoms/cm^3 or more to 1 x 10^{16} atoms/cm^3 or less, a carbon concentration is 1 x 10^{15} atoms/cm^3 or more to 3 x 10^{16} atoms/cm^3 or less,

a heat treatment including:

(A) a low-temperature heat treatment step of performing a heat treatment in a temperature range of 650°C or more to 750°C or less for a required time of 30 minutes or more to 5 hours or less;

(B) furthermore, a heat treatment which raises a temperature in a temperature range of up to 850°C at a temperature raising rate of 0.5°C/minute or more to 2°C/minute or less;

(C) a temperature falling and extracting step of decreasing a temperature of a furnace at a temperature falling rate of 1°C/minute or more to 10°C/minute or less and extracting the substrate out of the furnace at 600°C or more to 750°C or less to cool the substrate to a room temperature, and

(D) a high-temperature heat treatment of setting the temperature of the furnace to 600°C or more to 750°C or less after the temperature falling and extracting step, inserting the substrate into the furnace, raising the temperature of the furnace in a temperature range of less than 1100°C at a temperature raising rate of 5°C/minute or more to 10°C/minute or less, raising the temperature in a temperature range of 1100°C or more to 1250°C or less at a temperature raising rate of 1°C/minute or more to 2°C/minute or less, holding the temperature at 1000°C or more to 1250°C or less to make a diffusion length of inter-lattice oxygen 50 μm or more is performed.

[0021]

(3) A method of manufacturing the silicon wafer described in the (1), characterized in that

a nitrogen concentration of a substrate is 5×10^{14} atoms/cm^3 or more to 1×10^{16} atoms/cm^3 or less, a carbon

concentration is 1 x 10^{15} atoms/cm^3 or more to 3 x 10^{16} atoms/cm^3 or less,

a heat treatment including:

(A) a low-temperature heat treatment step of performing a heat treatment in a temperature range of 650°C or more to 750°C or less for a required time of 30 minutes or more to 5 hours or less;

(B) furthermore, a heat treatment which raises a temperature in a temperature range of up to 850°C at a temperature raising rate of 0.5°C/minute or more to 2°C/minute or less; and

(C) furthermore, a high-temperature heat treatment in which a heat raising process up to less than 1100°C is performed at a temperature raising rate of 5°C/minute or more to 10°C/minute or less and in a temperature range of 1100°C or more to 1250°C or less at a temperature raising rate of 1°C/minute or more to 2°C/minute or less, and the temperature is held at 1000°C or more to 1250°C or less to make a diffusion length of interstitial oxygen 50 μm or more is performed.

[0022]

In this case, according to embodiments of the present invention, a BMD having an octahedron shape means a BMD having a shape surrounded by a plurality of {111} planes and other planes. In general, the shapes includes a shape surrounded by eight {111} planes and a shape surrounded by {111} planes and

{100} planes. Planes other than {111} plane and {100} plane may appear.

[0023]

The shapes of BMDs being present in a wafer also include a plate-like shape other than the octahedron. A plate-like BMD is a BMD having a shape surrounded by two {100} planes which are relatively large and other planes. An inside of the BMD may have a tree-like shape. Discrimination between the octahedron shape and the plate-like shape is performed as follows. Of sizes in a [100] direction and a [010] direction when viewed in a [001] direction, a long size is defined as A, and a short size is defined B. In this case, a shape having a ratio of A/B (to be referred to as an "oblateness" hereinafter) of 1.5 or less is defined as an octahedron, and a shape having a ratio of A/B of larger than 1.5 is defined as a plate-like shape. Since BMD shapes in the silicon wafer fluctuate, determination whether the shape of a BMD being present in a wafer is an octahedron shape or a plate-like shape may be performed as follows. That is, the A/B ratios of a plurality of BMDs at different positions in a wafer are measured, an average of the A/B ratios (to be referred to as an "average oblateness" hereinafter) is calculated, and it is determined whether the value exceeds 1.5. When this value exceeds 1.5, states of distortion acting on crystal lattices around the BMDs are different from each other. For this reason, an optimum BMD size distribution to

suppress occurrences of slip and warpage is different from that in the spirit and scope of the invention.

[0024]

In embodiments of the present invention, a diagonal length of an octahedron BMD means a longer one A of lengths in the [100] direction and the [010] direction.

[Effect of the Invention]

[0025]

In a silicon wafer according to the present invention which is a silicon wafer having BMDs each having an octahedron shape, BMDs each having a diagonal length of 200 nm or more of BMDs located at a position having a depth of 20 μm from a surface of the silicon wafer have a concentration of $2 \times 10^{9}/cm^{3}$ or less, and BMDs each having a diagonal length of 10 nm or more to 50 nm or less of BMDs located at a position having a depth of 50 μm or more have a concentration of $1 \times 10^{12}/cm^{3}$ or more. For this reason, occurrences of slip and warpage in device manufacturing processes are extremely minimized, the silicon wafer can be prevented from being deteriorated in strength while having a DZ layer, and large-scale (typically, 200 mm) high-quality devices can be manufactured.

[0026]

In the silicon wafer according to the present invention, in comparison with a mirror wafer being free from BMDs therein, slip dislocation and warpage do not

easily occur, and a high gettering capability can be obtained.

BEST MODE TO CARRYING OUT THE INVENTION

[0027]

The present invention will be described below in detail with reference to embodiments.

[0028]

(Silicon Wafer)

A silicon wafer according to the present invention is characterized in that occurrences of both slip and warpage in device manufacturing processes can be extremely minimized.

[0029]

In this case, dimensions (diameter and thickness) of a wafer in which the present invention is realized and the presence/absence of dope of various elements are not limited to specific ones. These characteristic features can be appropriately selected depending on the type of a required semiconductor silicon wafer.

[0030]

A semiconductor device manufacturing by using the silicon wafer according to the present invention is not limited to a specific one. The present invention can be applied to manufacturing of various semiconductor devices. More specifically, a silicon wafer according to the present invention can be widely applied to manufacturing of an epitaxial wafer having a surface on which an epitaxial

layer is formed, a silicon on insulator (SOI) wafer, an SIMOX wafer to which an SIMOX (Separation By Implanted Oxygen) process is performed, and an SiGe wafer having a surface on which an SiGe layer is formed.

[0031]

As the characteristic features of the silicon wafer according to the present invention, the silicon wafer has BMDs each having an octahedron shape, BMDs each having a diagonal length of 200 nm or more of BMDs located at a position having a depth of 20 μm from a surface of the silicon wafer have a concentration of $2 \times 10^9/cm^3$ or less, and BMDs each having a diagonal length of 10 nm or more to 50 nm or less of BMDs located at a position having a depth of 50 μm or more have a concentration of $1 \times 10^{12}/cm^3$ or more. This is a knowledge which is explained below by the present inventors.

[0032]

More specifically, in the silicon wafer having BMDs each has an octahedron shape, BMDs located at a position having a depth of 20 μm from a surface influence a warpage characteristic. Furthermore, BMDs each having a diagonal length of 10 nm or more to 50 nm or less and located at a position having a depth of 50 μm or more influence a slip suppressing characteristic. In general device manufacturing processes, occurrences of warpage and slip can be extremely minimized. In this manner, even though slip occurs from a wafer support portion in the device

manufacturing processes, the slip can be prevented from penetrating a silicon wafer surface. Even though slip occurs from a wafer edge portion, the slip can be prevented from reaching a semiconductor device forming region, and the slip can be prevented from adversely affect the device.

[0033]

When diagonal lengths of BMDs located at a position having a depth of 50 μm or more are smaller than 10 nm, or when a concentration of BMDs is smaller than $1 \times 10^{12}/cm^3$, the BMDs do not easily serve as sufficient barriers to slip propagation. Although the density and diagonal lengths of BMDs which can serve as barriers to slip propagation do not have upper limits, for the reason (will be described later), in a range which can be realized by an actual silicon wafer, the upper limit of the diagonal length of the BMD is 50 nm. More specifically, when BMDs are present at a high concentration, almost all solid solution oxygen is precipitated as BMDs. On the other hand, the number of oxygen atoms precipitated as BMDs does not exceed the number of oxygen atoms solved in CZ-Si, and a solid solution oxygen concentration is 1×10^{18} atoms/cm^3 at most. Therefore, when the BMDs are present at a high concentration, the concentration of the oxygen atoms precipitated as BMDs may be constant at about 1×10^{18} atoms/cm^3. In this state, when the BMD concentration increases, diagonal lengths decrease. More specifically, the diagonal lengths of BMDs which are present at a certain

concentration or more have an upper limit, and the BMDs having a concentration of 1 x $10^{12}/cm^3$ cannot be realized by BMDs each having a diagonal length of larger than 50 nm. Therefore, the ranges of the concentration and the diagonal length of BMDs which can suppress slip propagation are 1 x $10^{12}/cm^3$ or more and 10 nm or more to 50 nm or less, respectively.

[0034]

For this purpose, an interstitial oxygen concentration is preferably 5 x 10^{17} atoms/cm^3 or less. On the other hand, the lower limit of the interstitial oxygen concentration may be about 2 x 10^{17} atoms/cm^3. The interstitial oxygen concentration cannot be easily further decreased because a very-long-time heat treatment must be performed at a low temperature.

[0035]

The BMD size distribution and the interstitial oxygen concentration described above are desirably realized over an entire surface of a wafer. However, depending on applications, the distribution and the concentration may be realized in some region. For example, when only a typical slip brought from an edge portion of the wafer is prevented, in a region distanced from a wafer center by 80% or more of a wafer radius, the BMD size distribution and the interstitial oxygen concentration may be able to be realized. This is because a slip brought from the edge portion of the wafer frequently occurs in the region

distanced from the wafer center by 80% or more of the wafer radius. In order to prevent only warpage of a typical wafer, the BMD size distribution and the interstitial oxygen concentration may be able to be realized in the inside region having 80% or less of the wafer radius. This is because high-concentration dislocation inside a typical wafer which causes warpage frequently occurs in a region having 80% or less of the wafer radius.

[0036]

The silicon wafer according to the present invention is excellent in that slip and warpage occurring in device manufacturing processes are small. More specifically, a silicon wafer according to the present invention, in particular, a silicon wafer in which BMDs are controlled as described above and an interstitial oxygen concentration is reduced is characterized in that a length of a slip occurring in the following heat treatment is very small (typically, the length of the slip is 10 mm or less, and an amount of warpage obtained after the heat treatment is 10 μm or less).

[0037]

More specifically, as a test to evaluate slip and resistance to occurrence of warpage in device manufacturing processes, a heat treatment which holds a furnace temperature at 900°C, inserts a wafer into the furnace, and holds the temperature at 1100°C for 30 minutes.

[0038]

In the heat treatment, in a temperature range in which slip and warpage easily occur, thermal stress is practically maximum. For this reason, when dislocation is prevented from occurring at a temperature raising/falling rate in the temperature range, it can be said that the silicon wafer according to the present invention is a silicon wafer in which slip and warpage minimally occur in almost all the device manufacturing processes.

[0039]

In order to measure the shapes and diagonal lengths of the BMDs and the number of BMDs described above, a known measuring method can be generally used. More specifically, a method performed by a transmission electron microscope (to be referred to as a "TEM" and an infrared interference and a method of Optical Precipitate Profiler (to be referred to as an "OPP" hereinafter) are given.

[0040]

Methods of measuring and evaluating slip dislocation and an amount of warpage of a wafer are not limited. The slip dislocation and the amount of warpage can be generally measured by a known method. More specifically, an X-ray topograph is used to measure slip dislocation. An amount of warpage can be observed and evaluated by using FT-90A available from NIDAK corporation.

[0041]

Furthermore, in order to measure an interstitial oxygen concentration, a Fourier transformation infrared absorption spectroscopy (FTIR) can be used.

[0042]

(Method of Manufacturing Silicon Wafer)

The silicon wafer according to the present invention has the characteristic features described above. Therefore, methods to manufacture silicon wafers having the characteristic features are arbitrarily used. More specifically, single crystal growing conditions (crystal pulling rate, crystal cooling rate, crucible rotation, gas flow, and the like) and heat treatment conditions (heat treatment temperature, time, temperature raising/falling, and the like) are appropriately controlled to make it possible to manufacture a silicon wafer having the above characteristic features.

[0043]

In the present invention, in particular, a heat treatment for a substrate is preferably performed in steps.

[0044]

In this case, the substrate means a silicon wafer to which a heat treatment is not performed, and also means a substrate which is cut out of a single crystal ingot and to which steps such as chamfering other than the heat treatment are performed.

[0045]

A limitation of the size (diameter, thickness, and the like) and a limitation of the presence/absence of dope of various elements are not especially set, the size and the presence/absence of dope can be appropriately selected depending on the type and performance of a required silicon wafer.

[0046]

An interstitial oxygen concentration included in a substrate may be an oxygen concentration of contained in a silicon in silicon single crystal growth performed by a CZ method under normal conditions. When the substrate is manufactured by the heat treatment described below, preferably, the concentration falls within a range of 8.0 x 10^{17} atoms/cm^3 or more to 9.5 x 10^{17} atoms/cm^3 or less. When the oxygen concentration falls out of the range, BMDs are not formed at a high concentration, and BMDs each having a large size undesirably has a high-concentration.

[0047]

In the present invention, divided heat treatments, more preferably, includes (A) a low-temperature heat treatment which performs a heat treatment in a temperature range of 650°C or more to 750°C or less for a required time of 30 minutes or more to 5 hours or less, (B) furthermore, a heat treatment which raises a temperature up to 850°C at a temperature raising rate of 0.5°C/minute or more to 2°C/minute or less, (C) a temperature falling and extracting step decreasing a temperature of a furnace at a

temperature falling rate of 1°C/minute or more to 10°C/minute or less after the heat raising step and extract the substrate out of the furnace when the temperature of the furnace is 600°C or more to 750°C or less to cool the substrate to a room temperature, and (D) a high-temperature heat treatment which sets the temperature of the furnace to 600°C or more to 750°C or less after the temperature falling and extracting step, inserts the wafer into the furnace, raising the temperature of the furnace in a temperature range of up to 1100°C at a temperature raising rate of 5°C/minute or more to 10°C/minute or less, raises the temperature in a temperature range of 1100°C or more to 1250°C or less at a temperature raising rate of 1°C/minute or more to 2°C/minute less, and holds the temperature at 1000°C or more to 1250°C or less to make a diffusion length of interstitial oxygen 50 μm or more.

[0048]

A batch heat treatment in the present invention, more preferably, includes (A) a low-temperature heat treatment which performs a heat treatment in a temperature range of 650°C or more to 750°C or less for a time of 30 minutes or more to 5 hours or less, (B) furthermore, a heat treatment which raises a temperature up to 800°C at a temperature raising rate of 0.5°C/minute or more to 2°C/minute or less, and (C) furthermore, a high-temperature heat treatment which raises a temperature in a temperature range up to less than 1100°C at a temperature raising rate of

5°C/minute or more to 10°C/minute or less and raises a temperature in a temperature range of 1100°C or more to 1250°C or less at a temperature raising rate of 1°C/minute or more to 2°C/minute or less, and holds a constant temperature at 1000°C or more to 1250°C or less to make a diffusion length of inter-lattice oxygen 50 μm or more is performed.

[0049]

In the step (A), since oxygen is not sufficiently diffused when a temperature of a heat treatment is lower then 650°C, it is not preferable that BMD formation does not sufficiently occur. On the other hand, when the temperature exceeds 750°C, the heat treatment rarely influences optimization of BMDs, and waste undesirably increases. Time for the heat treatment is shorter than 30 minutes, time required for BMD core formation is not sufficient. When the time exceeds 5 hours, productivity extremely decreases undesirably.

[0050]

Furthermore, in the step (B), when a temperature raising rate in the heat raising step is lower than 0.5°C/minutes, a stable temperature increasing rate cannot be secured. When the temperature raising rate exceeds 2°C/minute, deposited BMDs are not undesirably eliminated.

[0051]

Furthermore, the high-temperature heat treatment step (D) is to outwardly diffuse interstitial oxygen to form a

DZ layer. In this step, when a holding temperature is lower than 1000°C, it is not preferable in terms of production decrease that a long time is required to outwardly diffuse interstitial oxygen. When the holding temperature exceeds 1250°C, the quality of member in an annealing furnace is extremely deteriorated undesirably. When a diagonal length of the interstitial oxygen is a numerical value calculated on the basis of a temperature and a time in the step. More specifically, the numerical value can be calculated by the following equation (i).

[0052]

Diffusion length (μm) of inter-lattice oxygen = $2 \times 10^4 \times (D \times \text{time (second)})^{0.5}$

where

$D\ (cm^2/second) = 0.17 \times \exp(-2.53 \div 8.62 \times 10^{-5} \div \text{temperature (K)})$

In this manner, a heat treatment which obtains a diffusion length 50 μm or more is preferable to form a large-sized DZ layer having a width of 5 μm or more.

[0053]

An extracting step is added to the heat treatment when two heat treatment furnaces are used and when a low-temperature heat treatment and a high-temperature heat treatment are performed in different furnaces, respectively. When the respective heat treatments are advantageously performed in the different furnaces to improve the productivity, the temperature raising and extracting step

is preferably added to divide the heat treatments into a low-temperature heat treatment and a high-temperature heat treatment.

[0054]

A temperature raising rate in the temperature raising and extracting step is preferably 1°C/minute or more to 10°C/minute or less which can be realized by a general furnace. A temperature of the furnace when a substrate is extracted from the furnace is undesirably lower than 600°C because the life of a heater in the furnace is shortened. The temperature undesirably exceeds 750°C because members of the furnace are deteriorated.

[0055]

A temperature of a furnace when a wafer is inserted in the high-temperature heat treatment is undesirably lower than 600°C and undesirably higher than 750°C for the same reason as the temperature falling step. A temperature raising rate up to 1100°C is preferably 5°C/minute or more to 10°C/minute or less which can be realized by a general furnace, and a temperature raising rate in a temperature range of 1100°C or more to 1250°C or less is preferably 1°C/minute or more to 2°C/minute or less. A temperature and a range of a diffusion length of oxygen in a heat treatment at 1000°C or more are as described above. A temperature raising speed and a pulling temperature after the high-temperature heat treatment is performed are not limited to specific ones.

[0056]

An apparatus used in the series of heat treatments described above are not limited to specific one, and a conventional known apparatus is preferably used. More specifically, a normal batch type vertical furnace, a batch type vertical furnace with an oxygen purge function, and the like are given.

[0057]

In the manufacturing method according to the present invention, the substrate preferably contains nitrogen. This is because the substrate contains nitrogen to suppress warpage to a lower level (typically, 15 μm or less). In this manner, the warpage is further suppressed, so that a higher-performance device can be manufactured.

[0058]

A concentration of nitrogen added for this purpose is preferably 5×10^{14} atoms/cm^3 or more to 1×10^{16} atoms/cm^3 or less. When the concentration exceeds the range, polycrystallization undesirably occurs because an yield may be decreased.

[0059]

In the manufacturing method according to the present invention, the substrate preferably contains carbon. This is because the substrate contains carbon to advantageously form BMDs even though the low-temperature heat treatment is performed at a low temperature for a comparatively short period of time.

[0060]

A concentration of carbon added for this purpose is preferably 1 x 10^{15} atoms/cm^3 or more to 3 x 10^{16} atoms/cm^3 or less. When carbon is added at a concentration higher than the above range, a production yield disadvantageously decreases in crystal manufacturing. Furthermore, when concentration is lower than the range, the BMD concentration of a bulk is difficult to be 1 x 10^{12}/cm^3 or more. Furthermore, the carbon concentration is more preferably 1 x 10^{16} atoms/cm^3 or less.

[0061]

Methods of adding nitrogen and carbon to a substrate are not limited to specific methods, and a conventional known method is preferably used. More specifically, as a method of adding nitrogen, substrate with nitride film is added to a single-crystal pulling melt to make it possible to adjust a nitrogen concentration of the obtained substrate. And as a method of adding carbon powder is added to a single-crystal pulling melt to make it possible to adjust a carbon concentration of an obtained substrate.

[0062]

Methods of measuring concentrations of nitrogen, carbon, and oxygen contained in a substrate are not limited to specific methods, and the concentrations can be preferably measured by conventional known methods. More specifically, in measurement of a nitrogen concentration, the nitrogen concentration a secondary ion mass analyzing

apparatus (SIMS) can be used. The oxygen concentration and the carbon concentration are measured by an infrared absorption method, and can be calculated as converted coefficients by a value of Japan Electronics and Information Technology Industries Association (JEITA).

[Examples]

[0063]

The present invention will be described below in detail by examples. However, the present invention is not limited to the examples.

[0064]

(Method of Manufacturing Annealed Wafer)

Single-crystal ingots were manufactured under various conditions (wafer diameter, conductivity type, oxygen, nitrogen, carbon concentration), and the same portions of straight body parts of the single-crystal ingots were cut by using a wire saw. The portions obtained by performing mirror processing having a thickness of 725 μm or more to 750 μm or less were used as substrates. Annealed wafers were manufactured from the substrates by the following method.

[0065]

Divided Heat Treatment

An obtained substrate was put in a batch type first vertical heat treatment furnace, a low-temperature heat treatment was performed to the substrate. The substrate was put in a second vertical heat treatment furnace, and a

high-temperature heat treatment was performed in an argon gas atmosphere. A diffusion length of interstitial oxygen in the high-temperature heat treatment was obtained by integrating the equation (i) according to a temperature pattern of the high-temperature heat treatment. Heat treatment conditions of the examples and comparative examples will be described below.

[0066]

Batch Heat Treatment

An obtained substrate was put in a batch type vertical heat treatment furnace, a low-temperature heat treatment and a high-temperature heat treatment were performed in an argon gas atmosphere in the same furnace. A diffusion length of interstitial oxygen in the high-temperature heat treatment was obtained by integrating the equation (i) according to a temperature pattern of the high-temperature heat treatment. Heat treatment conditions of the examples and the comparative examples will be described below.

[0067]

Examples of Heat Treatment

Examples 1 to 3: at 700°C for 4 hours, temperature was raised to 800°C at 1°C/minute, at 800°C for 0 hour, temperature was decreased at 3°C/minute, substrate was extracted at 700°C and cooled to a room temperature, substrate was inserted at 700°C, temperature raised/decreased at lower than 1100°C at 5°C/minute,

temperature was raised/decreased at 1100°C or more at 1°C/minute, at 1200°C for 0 hour

Example 4: at 700°C for 4 hours, temperature was raised to 750°C at 0.5°C/minute, at 750°C for 0 hour, temperature was decreased at 3°C/minute, substrate was extracted at 700°C and cooled to room temperature, substrate was inserted at 700°C, temperature raised/decreased at lower than 1100°C at 5°C/minute, temperature was raised/decreased at 1100°C or more at 1°C/minute, at 1200°C for 0 hour

Example 5: at 700°C for 4 hours, temperature was raised to 800°C at 0.5°C/minute, temperature was raised/decreased to 1100°C at a 8°C/minute, temperature raised/decreased at 1100°C or more at 1°C/minute, at 1200°C for 5 hour

Comparative Examples 1 to 4: at 700°C for 4 hours, temperature was raised to 800°C at 1°C/minute, at 800°C for 0 hour, temperature was decreased at 3°C/minute, substrate was extracted at 700°C and cooled to a room temperature, substrate was inserted at 700°C, temperature raised/decreased at lower than 1100°C at 5°C/minute, temperature was raised/decreased at 1100°C or more at 1°C/minute, at 1200°C for 1 hour

Comparative Example 5: at 700°C for 4 hours, substrate was extracted at 700°C and cooled to a room temperature, substrate was inserted at 700°C, temperature raised/decreased at lower than 1100°C at 5°C/minute,

temperature was raised/decreased at 1100°C or more at 1°C/minute, at 1200°C for 1 hour

Comparative Example 6: at 700°C for 4 hours, temperature was raised to 800°C at 0.5°C/minute, at 800°C for 0 hour, temperature was decreased at 3°C/minute, substrate was extracted at 700°C and cooled to a room temperature, substrate was inserted at 700°C, temperature raised/decreased at lower than 1100°C at 5°C/minute, temperature was raised/decreased at 1100°C or more at 1°C/minute, at 1200°C for 1 hour

[0068]

Manufacturing conditions of the manufactured wafers (Examples 1 to 5 and Comparative Examples 1 to 6)(wafer diameter, conductivity type, concentrations (nitrogen, oxygen, and carbon) in a substrate, and diffusion lengths of interstitial oxygen in each heat treatment) are listed in Table 1. In this table, a P-type is boron dope, and N-type is phosphorous dope. Adjustment and measurement of concentrations of inclusions (oxygen and the like) are performed according to a normal known method.

[0069]

[Table 1]

No.	Wafer Diameter (mm)	Conductivity Type	Nitrogen (atoms/cm^3)	Oxygen (atoms/cm^3)	Carbon (atoms/cm^3)	Diffusion Length of Inter-lattice Oxygen in High-temperature Heat Treatment (μm)
Example 1	200	P	1.3E+15	9.2E+17	1.5E+15	52
Example 2	200	P	1.4E+15	9.0E+17	3.5E+15	52
Example 3	200	N	1.9E+15	9.3E+17	2.6E+15	52
Example 4	200	P	1.6E+15	9.2E+17	4.7E+15	52
Example 5	200	P	2.4E+15	8.8E+17	8.1E+15	52
Comparative example 1	200	P	1.3E+15	9.2E+17	1.5E+15	23
Comparative example 2	200	N	1.9E+15	9.3E+17	2.6E+15	23
Comparative example 3	200	P	3.3E+15	8.6E+17	1.0E+16	23
Comparative example 4	200	P	1.4E+15	9.0E+17	3.5E+15	23
Comparative example 5	200	P	1.4E+15	8.7E+17	3.3E+15	23
Comparative example 6	200	P	3.2E+15	8.6E+17	1.3E+16	23

Manufacturing Conditions of Manufactured Wafers, and Concentrations in Substrates

[0070]

(Measurement and Evaluation of Annealed Wafer)

Each annealed wafer obtained under the manufacturing conditions was measured and evaluated in the following (1), (2), (3), and (4). TEM samples of samples used in measurements of (1) and (2) was obtained as follows. That is, the wafers were polished by a precision polisher to predetermined depths (50 μm, 100 μm, and 300 μm), and the samples were obtained from a center portion of the wafer and a portion distanced from an edge by 10 mm. An OPP was set such that a focus is set to predetermined depths (5 μm and 15 μm from a surface layer) of the wafers and predetermined positions (center, and 10 mm from edge).

[0071]

(1) Determination of BMD Shape: the same measurement sample was measured twice while changing a scan direction of an OPP into <110> direction and <100> direction, and (A BMD oblateness was determined) a ratio of signal intensities obtained by both the measurements. More specifically, a relationship between the ratio of the signal intensities and the BMD oblateness was examined in advance, and a oblateness was calculated from the ratio of the signal intensities. Measurement was also performed by a TEM. At this time, the oblateness was measured and calculated from a microscopic image viewed from [001] direction. From these results, BMD shape determination was performed. At least 10 BMDs in each of the samples were measured, and all obtained oblatenesses were averaged to calculate an average oblateness. It was determined whether the average oblatenesses exceeded 1.5.

[0072]

(2) BMD Size and Concentration: Sizes and concentrations were obtained by measuring a portion having a depth of less than 20 μm from a surface layer by using an OPP and measuring a portion having a depth of 50 μm or more by using a TEM. From observation results of the BMDs obtained by the following methods 1) and 2), concentrations of BMDs each having a predetermined size were calculated. As the concentration of BMDs each having the predetermined size, an average value at three portions at a predetermined depth was used.

[0073]

1) Measurement by OPP: By using an OPP available from AXENT Technologies, a signal intensity obtained by performing signal processing electrically to a phase difference of transmitting lasers caused by BMDs was measured. As measurement range in a direction of depth, a range in a depth of ±5 μm from the setting was used. More specifically, when a focus was set at a position in a depth of 5 μm from a surface, a range from a depth of 0 μm to 10 μm was measured. When the focus was set at a position in a depth of 15 μm from the surface, a range from a depth 10 μm to 20 μm was measured. In size correction of BMDs was performed as follows. That is, BMDs each having known sizes were measured by an OPP, and a correction curve of the signal intensities and BMD sizes was formed. The correction curve will be described below.

[0074]

BMD diagonal length (nm) having an octahedron shape = $153 \times (\text{OPP signal})^{0.43}$

By using the correction curve, BMD sizes were calculated from signal intensities. In calculation of the sizes, a ghost signal removing process (K. Nakai Review of Scientific Instruments, vol. 69 (1998) pp. 3283) was performed. A detection sensitivity was set to a sensitivity at which a BMD having a diagonal length of 80 nm or more could be measured.

[0075]

2) Measurement by TEM: from a microscopic image obtained by measurement, a concentration of BMDs each having a predetermined size was calculated. The concentration was calculated from the number of BMDs observed in a field of view and a volume of a sample corresponding to an observed region.

[0076]

(3) Nitrogen Concentration of Annealed Wafer

A sample was extracted from an annealed wafer and polished by 20 μm to remove a nitrogen outward diffusion layer on the surface. Thereafter, a nitrogen concentration was measured.

[0077]

Slip Length of Annealed Wafer and Warpage Resistance Evaluation

A heat treatment (to be referred to as a "pseudo device process heat treatment" hereinafter) described in the following (4) was performed to an annealed wafer. Warpages of the annealed wafer before the pseudo device process heat treatment and after the pseudo device process heat treatment were measured by FT-90A available from NIDEK corporation to calculate an increase in warpage = warpage after heat treatment - warpage before heat treatment. An annealed wafer after the pseudo device process heat treatment was observed by an X-ray topograph, and a maximum length of lengths of observed slips was defined as a typical value.

(4) Heat Treatment using Batch Type Heat Treatment Furnace (I): Holds a furnace temperature at 900°C, and a wafer is inserted into the furnace

(II): Holds a temperature at 900°C for 30 minutes in an oxygen gas atmosphere, and then extract the wafer at 900°c

[0078]

(Measurement Results and Evaluation Results of Annealed Wafers)

In Table 2, as examples and comparative examples, with respect to annealed wafers manufactured under the manufacturing conditions shown in Table 1, measured concentrations of BMDs each having a predetermined size and slips and amounts of warpage occurring in the pseudo device process heat treatment are listed. The wafer manufactured under any of the conditions has a BMD average oblateness was 1.5 or less.

[0079]

[Table 2]

No.	Wafer Diameter (mm)	Conductivity Type	Nitrogen (atoms/cm^3)	Oxygen (atoms/cm^3)	Carbon (atoms/cm^3)	Diffusion length of Inter-lattice Oxygen in High-temperature Heat treatment (μm)	BMD Concentration		Slip (mm)	Amount of Warpage (μm)
							1 Surface Layer (1/cm^3) 200nm≤	2 Inside Bulk (1/cm^3) 10mm≤ 50nm≥		
Example 1	200	P	1.3E+15	9.2E+17	1.5E+15	52	1.1E+09	2.0E+12	7.8	1.3
Example 2	200	P	1.4E+15	9.0E+17	3.5E+15	52	2.0E+09	3.2E+12	4.7	0.0
Example 3	200	N	1.9E+15	9.3E+17	2.6E+15	52	1.9E+09	2.2E+12	8.7	1.5
Example 4	200	P	1.6E+15	9.2E+17	4.7E+15	52	1.6E+09	3.0E+12	8.2	1.7
Example 5	200	P	2.4E+15	8.8E+17	8.1E+15	52	1.8E+09	3.0E+12	0.9	6.4
Comparative example 1	200	P	1.3E+15	9.2E+17	1.5E+15	23	5.2E+09	2.0E+12	5.5	14.6
Comparative example 2	200	N	1.9E+15	9.3E+17	2.6E+15	23	7.9E+09	2.4E+12	5.8	39.6
Comparative example 3	200	P	3.3E+15	8.6E+17	1.0E+16	23	9.1E+09	2.4E+12	7.0	99.1
Comparative example 4	200	P	1.4E+15	9.0E+17	3.5E+15	23	6.2E+09	3.0E+12	2.9	33.3
Comparative example 5	200	P	1.4E+15	8.7E+17	3.3E+15	23	8.4E+08	4.8E+11	12.5	6.0
Comparative example 6	200	P	3.2E+15	8.6E+17	1.3E+16	23	7.1E+09	7.6E+11	11.0	72.2

[0080]

In this case, a "surface layer" of a BMD concentration in Table 2 is a concentration of BMDs each having a size of 200 nm or more, and an "inside bulk" of the BMD concentration means a concentration of BMDs each having a size of 10 nm or more to 50 nm or less. A value of a concentration of the "surface layer" is a sum of concentrations measured at a depth of 5 μm and a depth of 15 μm.

According to these results, the followings were obtained.

(i) A surface layer of a BMD concentration is 2 x $10^9/cm^3$ or less, an inside bulk of the BMD concentration is 1 x $10^{12}/cm^3$ or more. For this reason, a slip length is 10 mm or less, and an amount of warpage is suppressed to 10 μm or less.

(ii) A nitrogen concentration of an annealed wafer added with nitrogen was not different from a nitrogen concentration measured in a substrate.

(iii) Slips and warpages of a P-type and an N-type were not different from each other.

(iv) The same effects were obtained in the divided heat treatments and the batch heat treatment.

(v) Even in wafers in which nitrogen, oxygen, and carbon concentrations in a substrate were same, low-temperature heat treatments were changed, a slip characteristic or a warpage characteristic could be satisfied. However, both the characteristics could not be satisfied.

CLAIMS

1. A silicon wafer having a nitrogen concentration which is 5 x 10^{14} atoms/cm^3 or more to 1 x 10^{16} atoms/cm^3 or less, having a carbon concentration which is 1 x 10^{15} atoms/cm^3 or more to 8.1 x 10^{15} atoms/cm^3 or less, and having BMDs each having an octahedral shape, characterized in that BMDs each of which is located at a position shallower than the silicon wafer surface by a depth of less than 20 μm and has a diagonal length of 200 nm or more has a concentration of not more than 2 x $10^9/cm^3$, and BMDs each of which is located at a position having a depth of more than 50 μm and has a diagonal length of 10 nm or more to 50 nm or less have a concentration of 1 x $10^{12}/cm^3$ or more.

2. The method of manufacturing silicon wafer according to claim 1, characterized in that

a nitrogen concentration of a substrate is 5 x 10^{14} atoms/cm^3 or more to 1 x 10^{16} atoms/cm^3 or less, a carbon concentration is 1 x 10^{15} atoms/cm^3 or more to 8.1 x 10^{15} atoms/cm^3 or less,

a heat treatment including:

(A) a low-temperature heat treatment step of performing a heat treatment in a temperature range of 650°C or more 750°C or less for a required time of 30 minutes or more to 5 hours or less;

(B) furthermore, a heat treatment which raises a temperature in a temperature range of up to 850°C at a temperature raising rate of 0.5°C/minute or more to 2°C/minute or less;

(C) a temperature falling and extracting step of decreasing a temperature of a furnace at a temperature falling rate of 1°C/minute or more to 10°C/minute or less after the heat raising step and extracting the substrate out of the furnace when the temperature of the furnace is 600°C or more to 750°C or less to cool the substrate to a room temperature; and

(D) a high-temperature heat treatment which sets the temperature of the furnace to 600°C or more to 750°C or less after the temperature falling and extracting step, inserts the substrate into the furnace, raising the temperature of the furnace in a temperature range of less than 1100°C at a temperature raising rate of 5°C/minute or more to 10°C/minute or less, raises the temperature in a temperature range of 1100°C or more to 1250°C or less at a temperature raising rate of 1°C/minute or more to 2°C/minute or less, and holds the temperature at 1000°C or more to 1250°C or less to make a diffusion length of interstitial oxygen 50 μm or more is performed.

3. The method of manufacturing the silicon wafer according to claim 1, characterized in that

a nitrogen concentration of a substrate is 5×10^{14} atoms/cm^3 or more to 1×10^{16} atoms/cm^3 or less, a carbon concentration is 1×10^{15} atoms/cm^3 or more to 8.1×10^{15} atoms/cm^3 or less,

a heat treatment including:

(A) a low-temperature heat treatment step of performing a heat treatment in a temperature range of 650°C or more to 750°C or less for a required time of 30 minutes or more to 5 hours or less;

(B) furthermore, a heat treatment which raises a temperature in a temperature range of up to 850°C at a temperature raising rate of 0.5°C/minute or more to 2°C/minute or less; and

(C) furthermore, a high-temperature heat treatment in which a heat raising process up to less than 1100°C is performed at a temperature raising rate of 5°C/minute or more to 10°C/minute or less and in a temperature range of 1100°C or more to 1250°C or less at a temperature raising rate of 1°C/minute or more to 2°C/minute or less, and the temperature is held at 1000°C or more to 1250°C or less to make a diffusion length of interstitial oxygen 50 μm or more is performed.

SILICON WAFER AND METHOD OF MANUFACTURING THE SAME

ABSTRACT

To provide a silicon wafer which can suppress both occurrences of slip dislocation and warpage in device manufacturing processes and a method of manufacturing the same.

A silicon wafer according to the present invention is a silicon wafer having BMDs each having an octahedron shape. BMDs located at a position shallower than the silicon wafer surface by a depth of 20 μm or more and having a diagonal length of 200 nm or more have a concentration of 2 x $10^9/cm^3$ or less, and a BMD located at a position having a depth 50 μm or more and has a diagonal length of 10 nm or more to 50 nm or less has a concentration of 1 x $10^{12}/cm^3$ or more.

[Selected Diagram] Non