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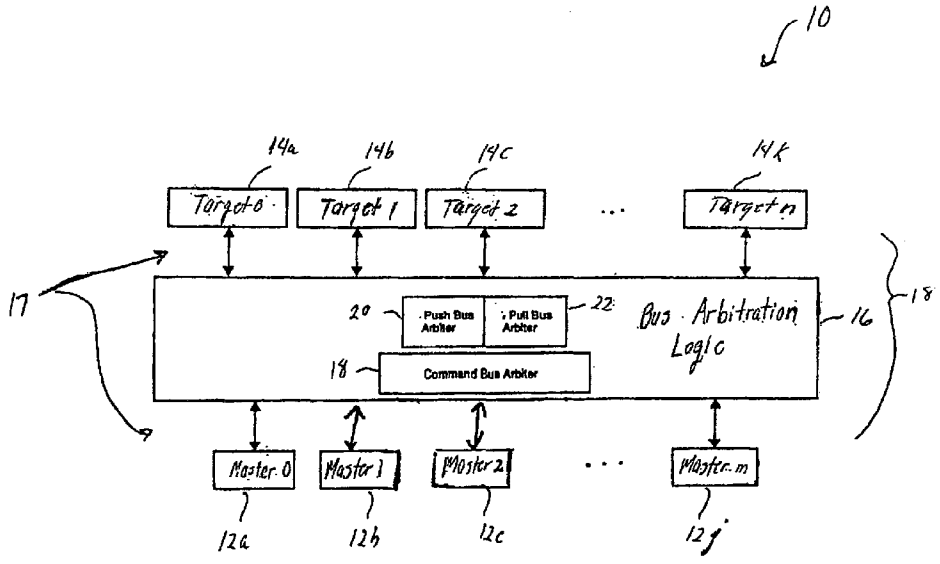
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(54) Title: A MULTIPROCESSOR INFRASTRUCTURE FOR PROVIDING FLEXIBLE BANDWIDTH ALLOCATION VIA MULTIPLE INSTANTIATIONS OF SEPARATE DATA BUSES, CONTROL BUSES AND SUPPORT MECHANISMS



(57) Abstract: A bus mechanism to control information exchanges between bus masters and bus targets over a bus structure that includes separate command, push and pull data buses. Commands are generated by bus masters and are interpreted by bus targets on a per-target basis. Each bus target controls the servicing of a command intended for such target by controlling the transfer of push data over the push bus to a bus master specified in the command as a destination, for a push operation type, and by controlling the transfer of pull data over the pull bus to the target from a bus master specified in the command as a destination, for a pull operation type. Arbitration logic associated with each bus is used to control the flow of the information exchanges on that bus.

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