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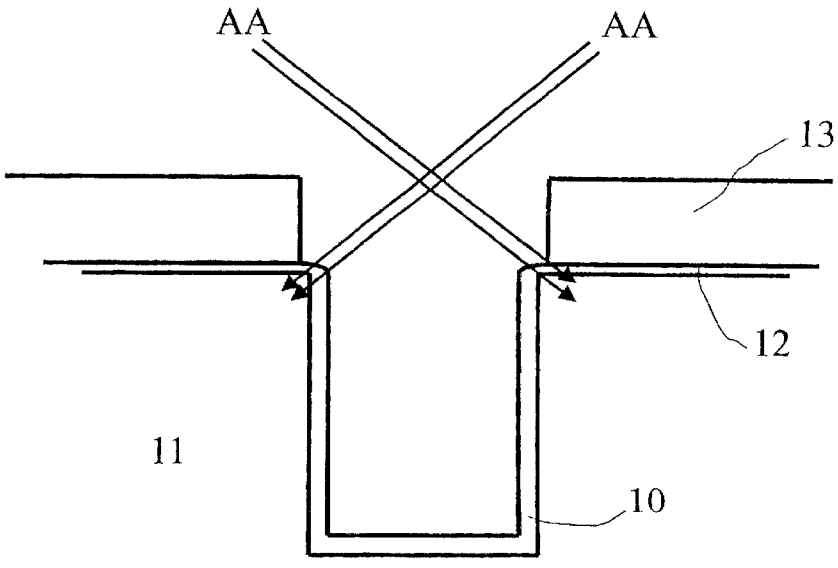
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(54) Title: REDUCTION OF NEGATIVE BIAS TEMPERATURE INSTABILITY IN NARROW WIDTH PMOS USING F2 IMPLANTATION



(57) Abstract: In a process of fabricating a narrow channel width PMOSFET device, the improvement of affecting reduction of negative bias temperature instability by use of F_2 side wall implantation, comprising: a) forming a shallow trench isolation (STI) region in a substrate; b) forming a gate on a gate oxide in the substrate; c) forming a liner layer in said shallow trench isolation region and subjecting the liner layer to oxidation to form a STI liner oxidation layer; d) implanting F_2 into side walls of said STI liner oxidation layer at a large tilted angle in sufficient amounts to affect reduction of negative bias temperature instability after a high density plasma fill of the STI F_2 impanted liner oxidation layer; and e) filling the STI F_2 implanted structure from step c) with a high density plasma (HDP) fill to affect reduction of negative bias temperature instability.

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