

A D/A Converter with a Gamma Compensation
and a Liquid Crystal Display Device

Field of the Invention

5 The present invention is related to an apparatus for driving a liquid crystal display device (LCD), and particularly to a D/A converter (DAC) with a gamma compensation.

Background of the Invention

10 Since, in a display device such as a CRT or LCD, the input voltage and emission output are not in a linear relationship, a gamma (γ) compensation is performed for digital data or analog data.

A digital method is known in which digital data is compensated by a gamma compensation using a look-up table or the like (for instance, PUPA 5-80713), and the data compensated by a gamma compensation is input to a DAC. This method has good stability, but has a disadvantage that accuracy decreases by about 2 bits. That is, even if a DAC of 8 bits is used, the gray scales which can be expressed are those of about 6 bits.

20 Also, there is a method in which digital data is decoded and switches for outputting reference voltages compensated by a gamma compensation are turned on/off by the decoding result. This method is effective if the number of gray scales is small, but, if the number of gray scales increases, the number of reference voltages increase or several bits of the input are discarded, thereby reducing the effective accuracy as in the above described method.

25 An analogue method is known in which non-linear elements are used to implement a gamma compensation of analog data after a D/A conversion by a DAC. Gray scales are maintained if the gamma compensation is successfully performed, but it is difficult to accurately perform the gamma compensation because analog elements are used. In addition, there is a disadvantage that it is difficult to acquire the stability against temperature.

Summary of the Invention

35 According to the invention there is provided a D/A converter for converting digital data read from a frame buffer for each pixel of a display screen to analog data compensated by a gamma compensation, wherein a curve of the gamma compensation is divided to a plurality of ranges sufficient to approximate the curve, comprising:

a decoder having a plurality of output lines corresponding to a number of digits of said digital data, and generating an output corresponding to said digital data on said plurality of output lines;

5 a constant current source;

output means connected to said constant current source for providing an output voltage by a flowing current;

10 a plurality of driver transistors, each connected to one of said plurality of output lines of said decoder and to said constant current source for conducting a current from said constant current source when said connected output line is active;

15 a plurality of limit transistor, each connected to one of said plurality of driver transistors; and

wherein said plurality of output lines of said decoder are grouped correspondingly to each of said plurality of ranges, and a common reference voltage in each group is applied to control terminals of said limit transistors associated with said output lines in
20 each of said groups.

The invention also provides a D/A converter for converting digital data read from a frame buffer for each pixel of a display screen to analog data compensated by a gamma compensation, wherein a curve of the gamma compensation is divided to a plurality of
25 ranges sufficient to approximate the curve, comprising:

a decoder having a plurality of output lines corresponding to a number of digits of said digital data, and generating an output corresponding to said digital data on said plurality of output lines;

30 a constant current source;

output means connected to said constant current source for providing an output voltage by a flowing current;

35 a plurality of driver transistors, each connected to one of said plurality of output lines of said decoder and to said constant current source for conducting a current from said constant current source when said connected output line is active;

a plurality of limit transistor, each connected to one of said plurality of driver transistors; and

wherein said plurality of output lines of said decoder are grouped correspondingly to each of said plurality of ranges, and a reference voltage for defining a current limited by said current limit transistors associated with said output lines in each group is supplied to said each group.

The invention also provides a liquid crystal display device comprising:

10

a D/A converter for converting digital data read from a frame buffer for each pixel of a display screen to analog data compensated by a gamma compensation, wherein a curve of the gamma compensation is divided to a plurality of ranges sufficient to approximate the curve, said D/A converter including:

15

a decoder having a plurality of output lines corresponding to a number of digits of said digital data, and generating an output corresponding to said digital data on said plurality of output lines;

20 a constant current source;

output means connected to said constant current source for providing an output voltage by a flowing current;

25 a plurality of driver transistors, each connected to one of said plurality of output lines of said decoder and to said constant current source for conducting a current from said constant current source when said connected output line is active;

30 a plurality of limit transistor, each connected to one of said plurality of driver transistors; and

wherein said plurality of output lines of said decoder are grouped correspondingly to each of said plurality of ranges, and a common reference voltage in each group is applied to control terminals of said limit transistors associated with said output lines in each of said groups; and

35

a liquid crystal panel including a circuit which drives each data line using the output voltage of said output means.

The invention also provides a liquid crystal display device comprising:

a plurality of D/A converter for converting digital data read from a frame buffer for each pixel of a portion of a display screen to analog data compensated by a gamma compensation, wherein a curve of the gamma compensation is divided to a plurality of ranges sufficient to approximate the curve, each said D/A converter including:

a decoder having a plurality of output lines corresponding to a number of digits of said digital data, and generating an output corresponding to said digital data on said plurality of output lines;

a constant current source;

output means connected to said constant current source for providing an output voltage by a flowing current;

a plurality of driver transistors, each connected to one of said plurality of output lines of said decoder and to said constant current source for conducting a current from said constant current source when said connected output line is active;

a plurality of limit transistor, each connected to one of said plurality of driver transistors; and

wherein said plurality of output lines of said decoder are grouped correspondingly to each of said plurality of ranges, and a common reference voltage in each group is applied to control terminals of said limit transistors associated with said output lines in each of said groups; and

a liquid crystal panel including a circuit which drives data lines associates with the each portion of display screen by using each output voltage of said plurality of D/A converters.

The invention also provides a liquid crystal display device comprising:

a plurality of D/A converter for converting digital data read from a frame buffer for each pixel of a portion a display screen to analog data compensated by a gamma compensation, wherein a curve of the gamma compensation is divided to a plurality of ranges sufficient to approximate the curve, each said D/A converter including:

a decoder having a plurality of output lines corresponding to a number of digits of said digital data, and generating an output corresponding to said digital data on said plurality of output lines;

5 a constant current source;

output means connected to said constant current source for providing an output voltage by a flowing current;

10 a plurality of driver transistors, each connected to one of said plurality of output lines of said decoder and to said constant current source for conducting a current from said constant current source when said connected output line is active;

15 a plurality of limit transistor, each connected to one of said plurality of driver transistors; and

wherein said plurality of output lines of said decoder are grouped correspondingly to each of said plurality of ranges, and a reference voltage for defining a current limited by said current limit transistors associated with said output lines in each group is
20 supplied to said each group; and a liquid crystal panel including a circuit which drives data lines associated with the each portion of display screen by using each output voltage of said plurality of D/A converters.

Preferred embodiments of the invention will now be described, by way of example
25 only, with reference to the accompanying drawings.

Brief Description of the Drawings

Figure 1 is a block diagram of the general construction of the present invention;

30 Figure 2 is a graph showing a gamma compensation curve;

Figure 3 is an example of the circuit for generating reference voltages;

Figure 4 is a figure showing the first variation of the present invention;

35

Figure 5 is a figure showing the second variation of the present invention; and

Figure 6 is a graph showing an example of the gamma compensation curve when the present invention is applied.

The following reference numerals are used in the description.

	1	Decoder
5	3	Group 1
	5	Group 2
	7	Group m
	9	Current source
	11	Transistor
10	13	Resistor
	15	Frame buffer
	17	Output section
	19	Liquid crystal panel
	100	DAC (embodiment of invention)
15	200	DAC

Preferred Embodiments of the Invention

In Figure 1, a schematic diagram of the present invention 100 is shown. The n-bit digital data from a frame buffer 15 is input to a decoder 1. Since the input is an n-bit input, the outputs of the decoder 1 are 2^n-1 (there is no output when the input is zero). In this instance, they are Do1 to Do 2^n-1 . These outputs are connected to the gate of one transistor, respectively. 2^n-1 transistors are arranged in the conventional DAC as described above, and a necessary number of transistors of these transistors are sequentially turned on. In the present invention, current limiting transistors (in Figure 1, Qi, where i is an integer from one to 2^n-1) are connected to those transistors, respectively. The set of two transistors represents one bit. A predetermined number of the sets of two transistors are collected, and treated as a group. The predetermined number is described later.

30 [0018]

The same voltage is used as the gate voltages of the current limiting transistors in the same group. In Figure 1, the gate voltage of the group 1 is Vr1. Similarly, the gate voltages of the groups 2 to m are Vr2 ... Vrm (M: the number of groups). The gate voltage is also described later. The outputs of the groups are all connected to the emitter of a transistor 11. To the emitter of the transistor 11, a current source 9 is also connected. A bias voltage is applied to the base of the

transistor 11, and a resistor 13 is connected to the collector thereof. As the output of the DAC, the voltage drop in the resistor 13 is used.

[0019]

The output of the DAC is connected to a liquid crystal panel 19. The liquid crystal panel 19 includes a circuit for passing the analog data from the DAC to the respective data lines (signal lines) of the liquid crystal panel. There are a method in which the outputs of the DAC 100 of the present invention are passed to the all data lines of the liquid crystal panel, and a method in which the outputs of a plurality of DACs 200 and of the DAC 100 are passed together to the data lines. The latter method is effective, because it can apply to elements (including the DAC) whose operation frequency is low.

[0020]

The operation of the present invention is as follows. The n-bit output from the frame buffer is input to the decoder 1. Decoding is performed in the decoder 1, and from one of the 2^n-1 outputs, the outputs in a number corresponding to the value of the n bits are turned on. The outputs of the decoder 1 are turned on, the transistors connected to them are also turned on and a current flows from the current source 9. However, the current flowing through the transistors is limited by the current limiting transistors. When the transistors belonging to the groups 1 to m are turned on,

respectively, a current flows in these transistors, and thus the current flowing through the transistor 11 having the output terminal gradually decreases. Accordingly, the output voltage also lowers. By passing the output voltage to the data lines of the liquid crystal panel 19, a desired image can be displayed.

[0021]

For the description of the above described predetermined number of transistors and gate voltages V_r , Figure 2 is referred to. This figure is a gamma compensation curve which shows the relationship between the applied voltage and the transmissivity of liquid crystal. The dotted line a is a curve showing the actual transmissivity. On the other hand, to approximate the gamma compensation curve using straight lines, the line segments D1 to Dm are connected. That is, the gamma compensation curve can be expressed by dividing it into m groups, and each group corresponds to each of the groups. The number of the transistors in each group corresponds to the potential difference represented by that group. That is, the required transistors increase as the voltage which must be covered by a group (for instance, in Figure 2, the voltage between V_0 and V_1 is covered by the group 1) increases, and less transistors are required if the voltage is small. Since the gamma compensation curve is approximated by straight lines, the range which can be approximated by a straight line must be defined as one group. In consequence, the number of the transistors varies among groups. For more accurate approximation, the transistors should be divided into more groups, but

the number of elements to be controlled increases as the number of division groups increases, causing a problem in the manufacturing. Thus, usually four to eight transistors form one group.

[0022]

As the gate voltage V_r , a voltage corresponding to the slope of the straight line in Figure 2 of a particular group (actually, the absolute value of the slope, usually the absolute value of the differentiated value at a point) is used. That is, for the group 1, it is a voltage corresponding to the slope (absolute value) of D_1 . If the gate voltage of a current limiting transistor is set in this way, the voltage varies in the group without departing from that straight line. For providing the V_r in a mounting, there is also a method in which the decoder and the portions after the decoder are implemented by an IC, one I/O pins is provided for each group, and voltages set by a technique such as resistive division as in Figure 3 are given to the I/O pins, respectively. However, any method for generating predetermined voltages may be used, and the inputting through I/O pins is not always needed. However, if the voltages can be set by I/O pins, change of the gamma compensation curve can be served.

[0023]

If the transistors are divided into groups and the gate voltages of the current limiting transistors are set for each group, as described above, the all current limiting

transistors can be controlled for each group without being controlled individually, whereby the gamma compensation curve can be approximated by straight lines. However, some portions are caused which largely differ from the true gamma compensation curve. Then, correction of them is performed by the following two variations.

[0024]

The first variation is shown in Figure 4. This is a figure in which the decoder 1 and the output section 17 in 100 of Figure 1 are omitted. In this case, a set of four transistors forms one group. The number of the sets of transistors is arbitrary as described above. A reference voltage V_{r1} is input to the gate of the least significant current limiting transistor Q1 in the group 1. Similarly, a reference voltage V_{r2} is input to the gate of the least significant current limiting transistor Q5 in the group 2. A resistive division using resistors R1, R2, R3 and R4 is performed between the two current limiting transistors. To the gates of the current limiting transistors Q2 to Q4 lying between the above gates, the voltages produced by the respective resistors are supplied, respectively.

[0025]

By this, the voltages given to the gates of the current limiting transistors gradually change. The voltages are as follows if the resistors R1, R2, R3 and R4 are set to the same value for simplicity.

Q1: V_{r1}
 Q2: $(3 * V_{r1} + 1 * V_{r2})/4$
 Q3: $(2 * V_{r1} + 2 * V_{r2})/4$
 Q4: $(1 * V_{r1} + 3 * V_{r2})/4$
 Q5: V_{r2}

[0026]

Naturally, in this case, the respective gate voltages are at equal intervals. The intervals may be changed by adjusting the resistors R1, R2, R3 and R4. Since the admittance of successive transistors linearly varies in this way, the resultant input/output characteristics have the envelope of a quadratic curve. In addition, the reference voltage V_r is a voltage which corresponds to the absolute value of the differentiated value at a point in the corresponding range of the gamma compensation curve.

[0027]

In Figure 5, the second variation of the present invention is shown. In this figure, the decoder 1 and the output section 17 in Figure 1 are also omitted. Further, in this embodiment, a set of eight transistors forms one group. The number of the sets of transistors is arbitrary as described above. A reference voltage V_{r1} is supplied to the gate of the least significant current limiting transistor Q1 in the group 1, and also to the gate of the second least significant current limiting transistor Q2. Further, a reference voltage V_{r2} is supplied to the least significant current limiting

transistor Q9 in the group 2, and also to the gate of the most significant current limiting transistor Q8 in the group 1 and to the second least significant current limiting transistor Q10 in the group 2. In addition, between the gate of the second least significant current limiting transistor in the group 1 and the most significant current limiting transistor Q8 in the group 1, a resistive division is performed using resistors R1 to R6. To the gates of the current limiting transistors Q2 to Q7, the voltages generated by the respective resistors are supplied, respectively.

[0028]

In this way, there can be provided portions where the gate voltage is linearly changed, and portions where it is changed in a curve. The gate voltages of the respective current limiting transistors are as follows if the resistors R1 to R6 are set to the same value for simplicity.

Q1: Vr1
 Q2: Vr1
 Q3: $(5 * Vr1 + 1 * Vr2)/6$
 Q4: $(4 * Vr1 + 2 * Vr2)/6$
 Q5: $(3 * Vr1 + 3 * Vr2)/4$
 Q6: $(2 * Vr1 + 4 * Vr2)/4$
 Q7: $(1 * Vr1 + 5 * Vr2)/4$
 Q8: Vr2
 Q9: Vr2
 Q10: Vr2

[0029]

Naturally, the gate voltages from Q2 to Q8 are at equal intervals. The intervals may be changed adjusting the values of the resistors. Since, in the admittance of the successive current limiting transistor, there are alternately appearing portions where the admittance is constant and portions where it linearly changes, as described above, the resultant input/output characteristics have the envelope synthesized by straight lines and quadratic curves. In addition, the reference voltage V_r is a voltage which corresponds to the absolute value of the differentiated value at the start point of the corresponding range of the gamma compensation curve (for instance, V_0 in the group 1, V_1 in the group 2).

[0030]

In the second variation, the same reference voltage is supplied to the least significant current limiting transistor in a certain group, the second least significant current limiting transistor, and the most significant current limiting transistor in the lower-order group adjacent to the certain group, but the same reference voltage may be provided not only to both sides of the least significant current limiting transistor in the certain group in this way, but also to a predetermined number of adjacent current limiting transistors according to the gamma compensation curve.

[0031]

As described above, the methods have been shown in which the gamma compensation curve is approximated by straight lines, quadratic curves, and straight lines and quadratic curves, but, if not only these methods are used to approximate the gamma compensation curve, but also approximation methods suitable for the respective ranges are used when the gamma compensation curve is divided into ranges, more preferred approximations can be performed.

[0032]

Figure 6 shows how the above three types of approximations are different. "a" shows the approximation by straight lines, "b" shows the approximation by quadratic curves, and "c" shows the approximation by the envelope of straight lines and quadratic curves. Since there are differences as in Figure 6, combination of them gives an approximation closer to the true gamma compensation curve than the approximation by only one method. However, the construction is simple for the approximation by straight lines and sometimes there is no problem with straight lines, and thus consideration should also be made from the viewpoint of cost.

[0033]

Furthermore, although, in the first and second variations, a resistive division is made to provide a

voltage to the gate of each current limiting transistor, the values of the resistors in the resistive division can be varied and resistors may even be removed to cause a short circuit. In this case, the short-circuited sections are approximated by straight lines. Thus, it may be considered that there is a first control of externally providing a
5 reference voltage, and a second control of how to provide the reference voltage to the gate of each current limiting transistor.

As described above, in accordance with a preferred embodiment of the invention, a DAC is provided which is highly stable and can perform an accurate gamma
10 compensation with a high effective accuracy.

A liquid crystal display device is provided which uses the DAC that produces the remarkable advantages as described above.



Claims:

1. A D/A converter for converting digital data read from a frame buffer for each pixel of a display screen to analog data compensated by a gamma compensation, wherein a curve of the gamma compensation is divided to a plurality of ranges sufficient to approximate the curve, comprising:

a decoder having a plurality of output lines corresponding to a number of digits of said digital data, and generating an output corresponding to said digital data on said plurality of output lines;

a constant current source;

output means connected to said constant current source for providing an output voltage by a flowing current;

a plurality of driver transistors, each connected to one of said plurality of output lines of said



decoder and to said constant current source for conducting a current from said constant current source when said connected output line is active;

a plurality of limit transistor; each connected to one of said plurality of driver transistors; and

wherein said plurality of output lines of said decoder are grouped correspondingly to each of said plurality of ranges, and a common reference voltage in each group is applied to control terminals of said limit transistors associated with said output lines in each of said groups.

- 2 A D/A converter for converting digital data read from a frame buffer for each pixel of a display screen to analog data compensated by a gamma compensation, wherein a curve of the gamma compensation is divided to a plurality of ranges sufficient to approximate the curve, comprising:

a decoder having a plurality of output lines corresponding to a number of digits of said digital data, and generating an output corresponding to said digital data on said plurality of output lines;

a constant current source;

output means connected to said constant current source for providing an output voltage by a flowing current;



a plurality of driver transistors, each connected to one of said plurality of output lines of said decoder and to said constant current source for conducting a current from said constant current source when said connected output line is active;

a plurality of limit transistor, each connected to one of said plurality of driver transistors; and

wherein said plurality of output lines of said decoder are grouped correspondingly to each of said plurality of ranges, and a reference voltage for defining a current limited by said current limit transistors associated with said output lines in each group is supplied to said each group.

3 A D/A converter according to Claim 2 wherein said reference voltage corresponds to a differentiated value at a point in said each corresponding range of said curve.

4 A D/A converter according to Claim 3 wherein said reference voltage corresponding to one of said groups is applied to a control terminal of said current limit transistor associated with the least significant output of said decoder in said one of said groups, and

the respective adjacent control terminals between its current limit transistor and said current limit transistor associated with the least significant output of said decoder in the higher-order group



adjacent to said one of said groups are connected through resistors, and a respectively generated voltage is supplied to the control terminal of each said current limit transistor.

- 5 A D/A converter according to Claim 3 wherein the reference voltage corresponding to one of said groups is applied to a control terminal of said current limit transistor associated with the least significant output of said decoder in said one of said groups, to the control terminal of said current limit transistor associated with the second least significant output, and to the control terminal of said current limit transistor associated with the most significant output of said decoder in the lower-order group adjacent to said one of said groups, and

the respective adjacent control terminals between said current limit transistor associated with the second significant output and said current limit transistor associated with the most significant output of said decoder in said one of said groups are connected through resistors, and a respectively generated voltage is applied to the control terminal of each said current limit transistor.

- 6 A D/A converter according to Claim 3 wherein the reference voltage corresponding to one of said groups is applied to a control terminal of said current limit transistor associated with the least significant output of said decoder in said one of



said groups, to the control terminals of said current limit transistors for said driver transistors connected up to the output of an order higher than said least significant output by a predetermined number, and to the control terminals of said current limit transistors for said driver transistors connected up to the output of an order lower than said most significant output of said decoder by a predetermined number in the lower-order group adjacent to said one of said groups, and

the respective adjacent control terminals between said current limit transistor associated with the output of an order higher than said least significant output by the predetermined number and said current limit transistor associated with the output of an order lower than said most significant output of said decoder by the predetermined number in said one of said group are connected through resistors, and the respectively generated voltage is applied to the control terminal of each said current limit transistor.

- 7 A D/A converter according to Claim 2 or 3 wherein one of following supply states of said reference voltage is set for said each group:

a common reference voltage in said each group is applied to control terminals of said current limit transistors associated with said output lines in said each group;



the reference voltage corresponding to one of said groups is applied to a control terminal of said current limit transistor associated with the least significant output of said decoder in said one of said groups, and the respective adjacent control terminals between its current limit transistor and said current limit transistor associated with the least significant output of said decoder in the higher-order group adjacent to said one of said groups are connected through resistors, and a respectively generated voltage is supplied to the control terminal of each said current limit transistor; and

the reference voltage corresponding to one of said groups is applied to a control terminal of said current limit transistor associated with the least significant output of said decoder in said one of said groups, to the control terminals of said current limit transistors for said driver transistors connected up to the output of an order higher than said least significant output by a predetermined number, and to the control terminals of said current limit transistors for said driver transistors connected up to the output of an order lower than said most significant output of said decoder by a predetermined number in the lower-order group adjacent to said one of said groups, and the respective adjacent control terminals between said current limit transistor associated with the output of an order higher than said least significant output by the predetermined



number and said current limit transistor associated with the output of an order lower than said most significant output of said decoder by the predetermined number in said one of said group are connected through resistors, and the respectively generated voltage is applied to the control terminal of each said current limit transistor.

8 A liquid crystal display device comprising:

a D/A converter for converting digital data read from a frame buffer for each pixel of a display screen to analog data compensated by a gamma compensation, wherein a curve of the gamma compensation is divided to a plurality of ranges sufficient to approximate the curve, said D/A converter including:

a decoder having a plurality of output lines corresponding to a number of digits of said digital data, and generating an output corresponding to said digital data on said plurality of output lines;

a constant current source;

output means connected to said constant current source for providing an output voltage by a flowing current;

a plurality of driver transistors, each connected to one of said plurality of output lines of said



decoder and to said constant current source for conducting a current from said constant current source when said connected output line is active;

a plurality of limit transistor, each connected to one of said plurality of driver transistors; and

wherein said plurality of output lines of said decoder are grouped correspondingly to each of said plurality of ranges, and a common reference voltage in each group is applied to control terminals of said limit transistors associated with said output lines in each of said groups; and

a liquid crystal panel including a circuit which drives each data line using the output voltage of said output means.

9 A liquid crystal display device comprising:

a plurality of D/A converter for converting digital data read from a frame buffer for each pixel of a portion a display screen to analog data compensated by a gamma compensation, wherein a curve of the gamma compensation is divided to a plurality of ranges sufficient to approximate the curve, each said D/A converter including:

a decoder having a plurality of output lines corresponding to a number of digits of said digital data, and generating an output corresponding to



said digital data on said plurality of output lines;

a constant current source;

output means connected to said constant current source for providing an output voltage by a flowing current;

a plurality of driver transistors, each connected to one of said plurality of output lines of said decoder and to said constant current source for conducting a current from said constant current source when said connected output line is active;

a plurality of limit transistor, each connected to one of said plurality of driver transistors; and

wherein said plurality of output lines of said decoder are grouped correspondingly to each of said plurality of ranges, and a common reference voltage in each group is applied to control terminals of said limit transistors associated with said output lines in each of said groups; and

a liquid crystal panel including a circuit which drives data lines associated with the each portion of display screen by using each output voltage of said plurality of D/A converters.

10 A liquid crystal display device comprising:



a plurality of D/A converter for converting digital data read from a frame buffer for each pixel of a portion a display screen to analog data compensated by a gamma compensation, wherein a curve of the gamma compensation is divided to a plurality of ranges sufficient to approximate the curve, each said D/A converter including:

a decoder having a plurality of output lines corresponding to a number of digits of said digital data, and generating an output corresponding to said digital data on said plurality of output lines;

a constant current source;

output means connected to said constant current source for providing an output voltage by a flowing current;

a plurality of driver transistors, each connected to one of said plurality of output lines of said decoder and to said constant current source for conducting a current from said constant current source when said connected output line is active;

a plurality of limit transistor, each connected to one of said plurality of driver transistors; and

wherein said plurality of output lines of said decoder are grouped correspondingly to each of said plurality of ranges, and a reference voltage



THIS SHEET HAS BEEN
REPLACED

for defining a current limited by said current limit transistors associated with said output lines in each group is supplied to said each group; and a liquid crystal panel including a circuit which drives data lines associated with the each portion of display screen by using each output voltage of said plurality of D/A converters.

5

11 A D/A converter substantially as hereinbefore described with reference to Figures 1, 2, 3 and 6, and Figure 4 or 5.

10 12 A liquid crystal display device comprising a D/A converter as claimed in claim 11.

This Sheet Has Been Replaced

