

FIG.1

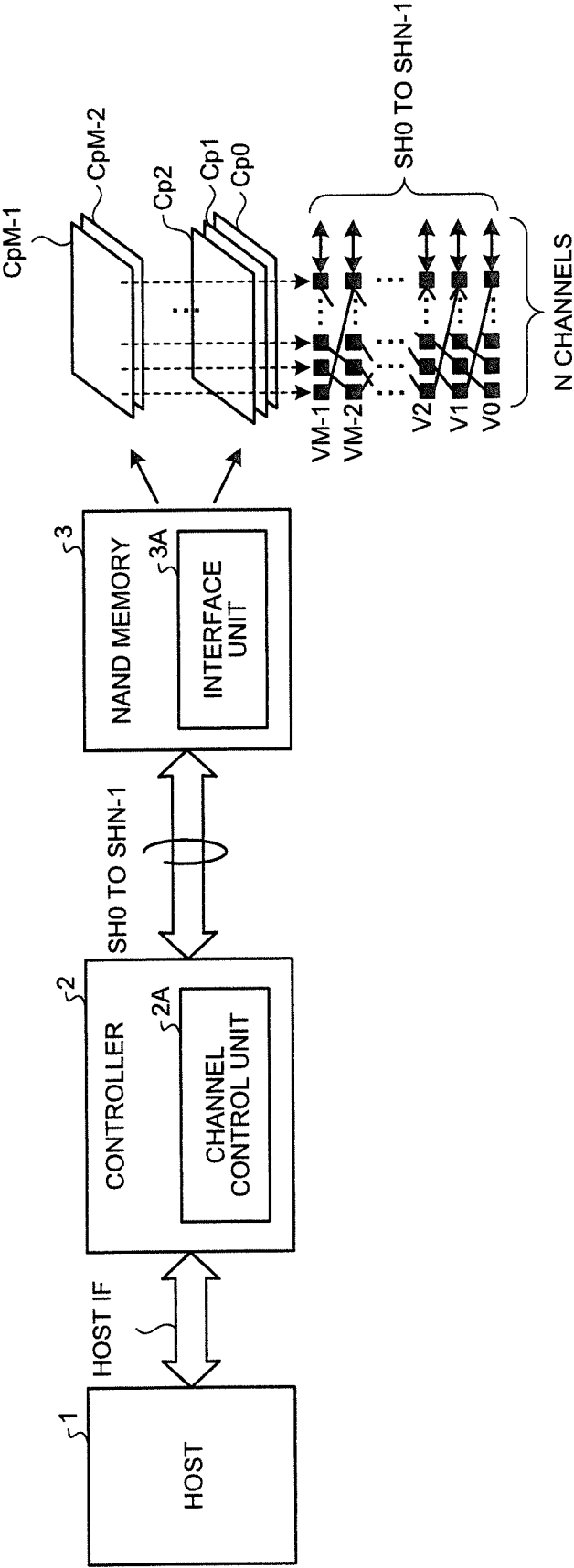


FIG.2

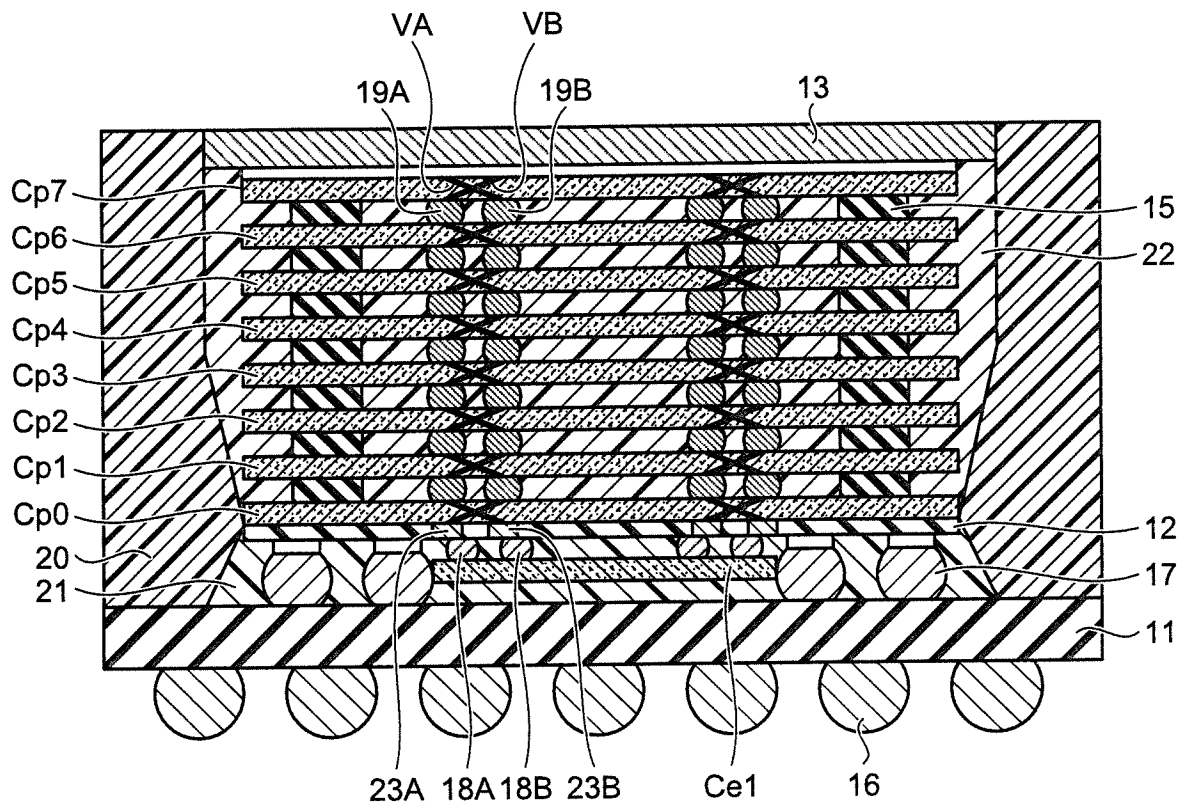


FIG.3

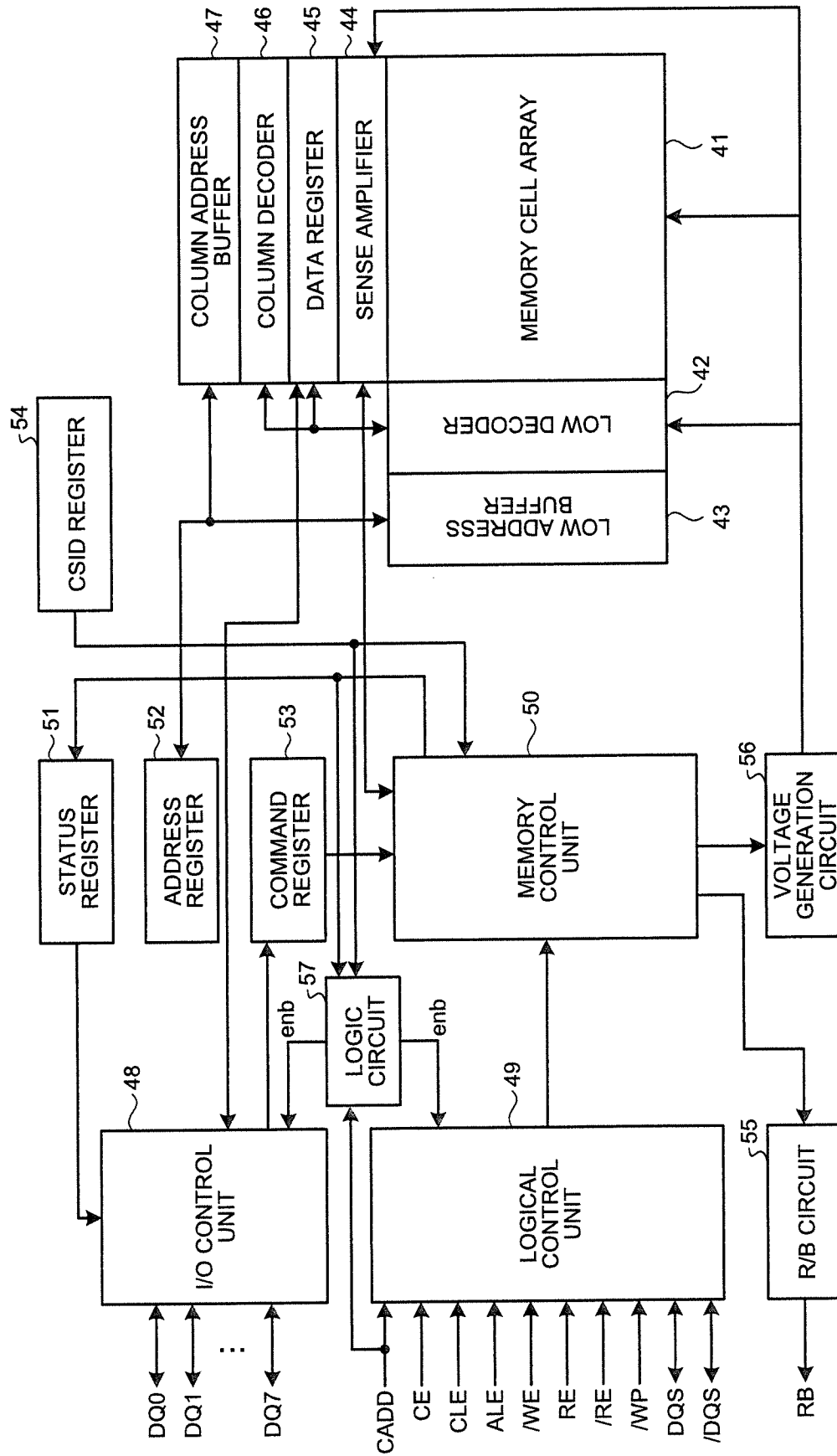


FIG.4

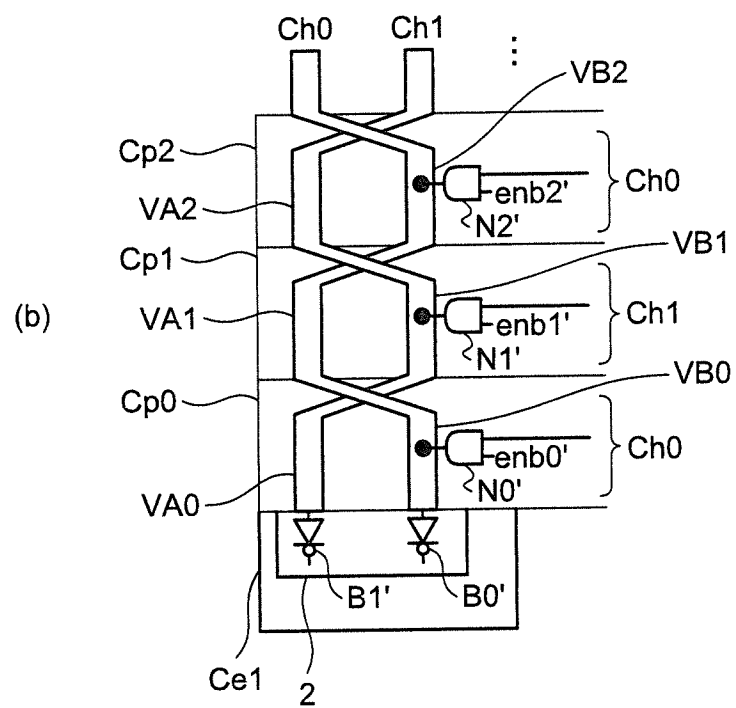
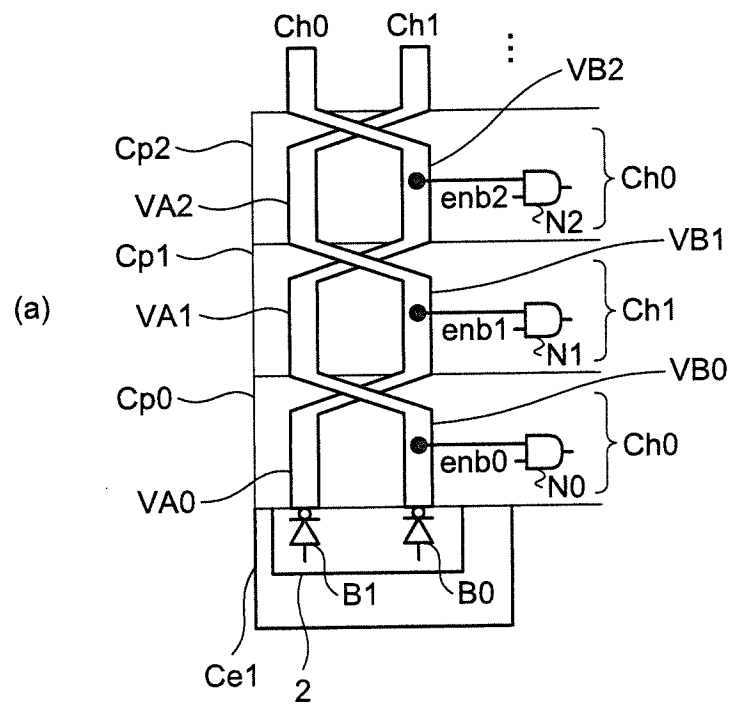


FIG.5

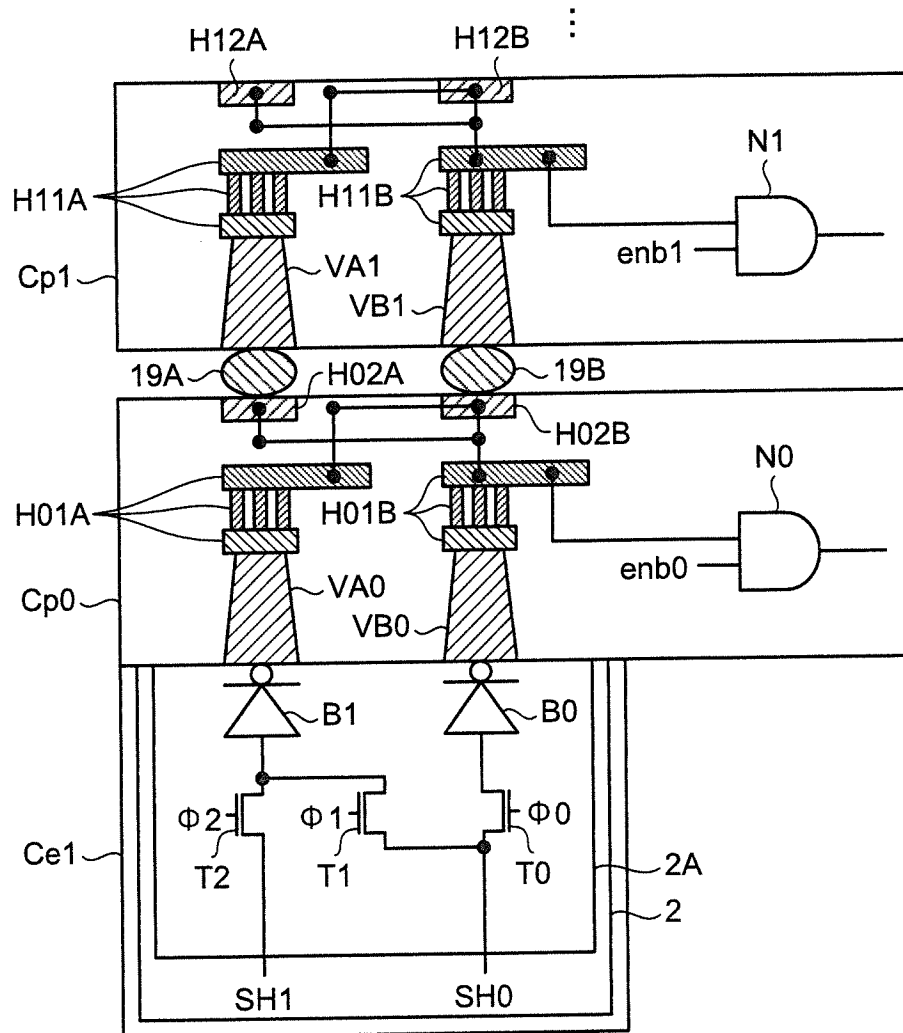


FIG.6

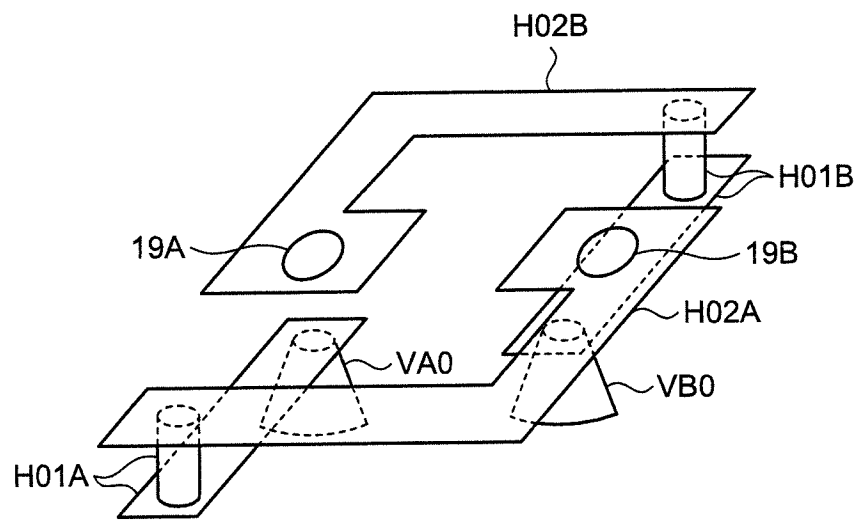


FIG.7

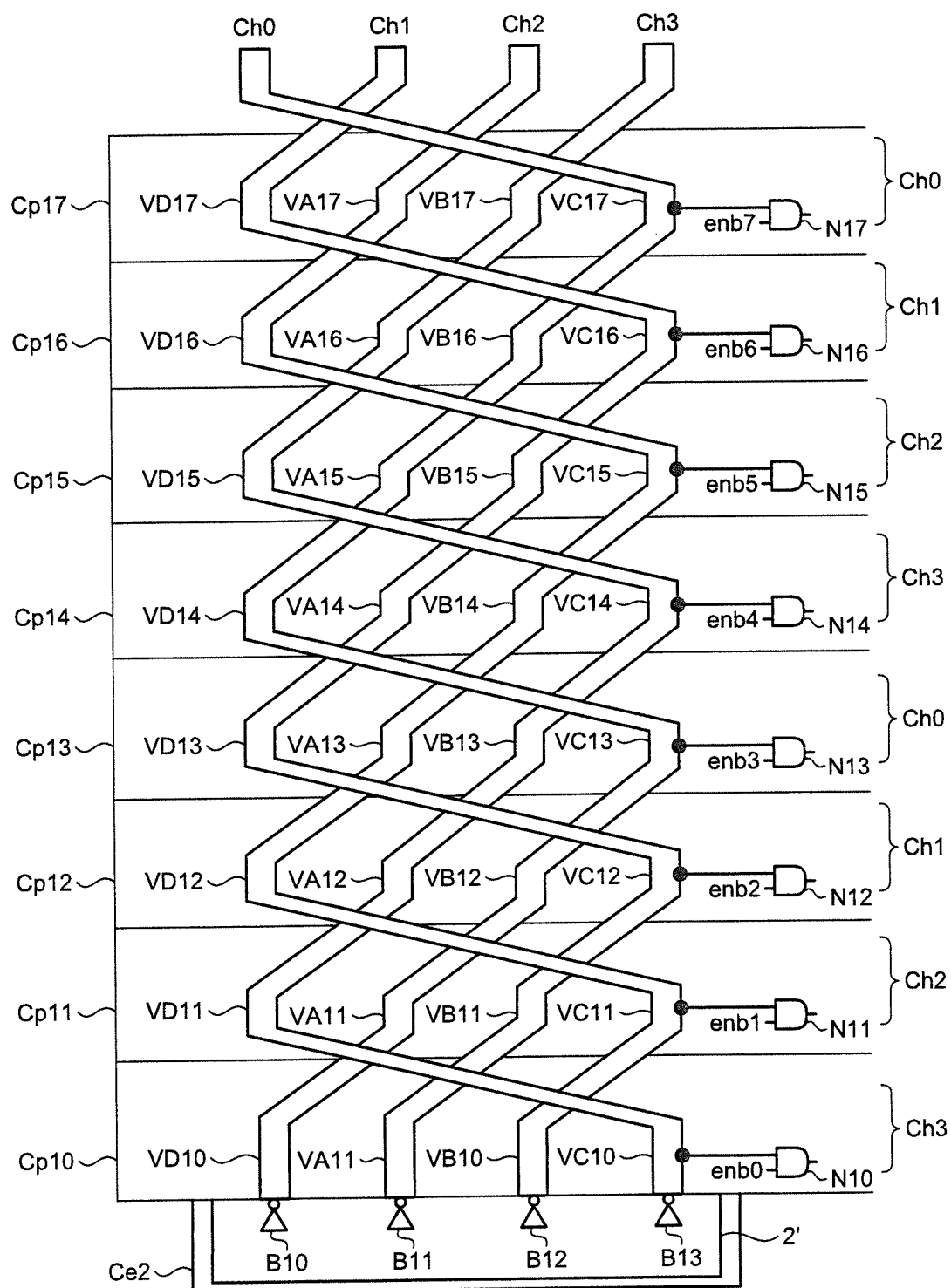


FIG.8

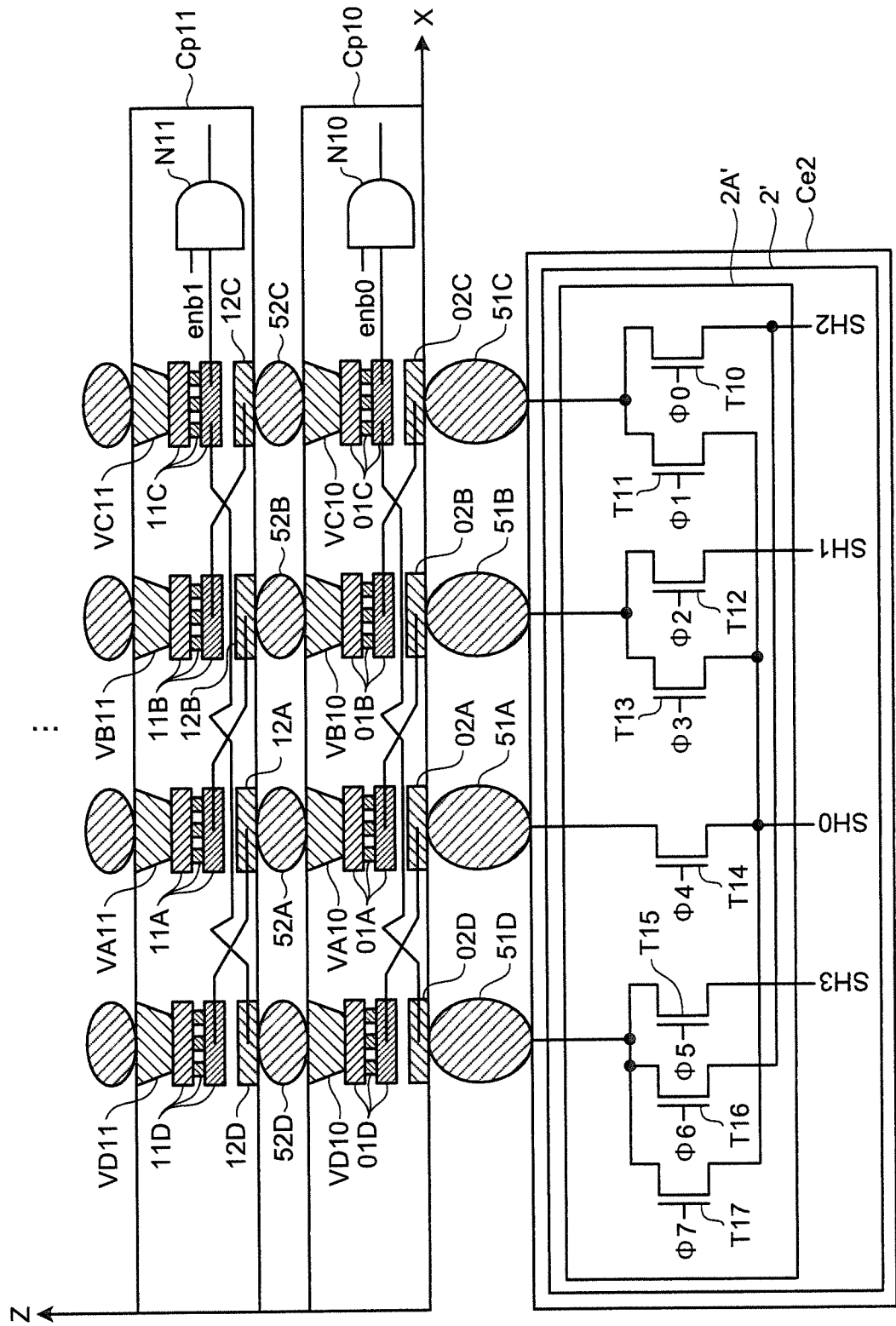


FIG.9

CH: CHANNEL CE: CHIP ENABLE	SH0	SH1	SH2	SH3
1CH/1CE	CE0			
1CH/2CE	CE0		CE2	
1CH/4CE	CE0	CE1	CE2	CE3
EACH 2CH/1CE	CE0		CE2	
EACH 2CH/2CE	CE0	CE1	CE2	CE3
EACH 4CH/1CE	CE0	CE1	CE2	CE3

FIG.10

