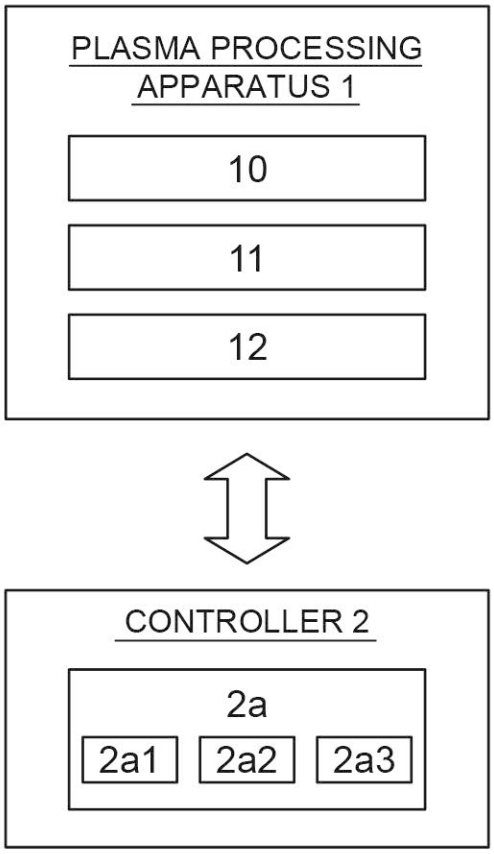
Fig.1


PLASMA PROCESSING APPARATUS 1
10
11
12
CONTROLLER 2
2a
2a1
2a2
2a3

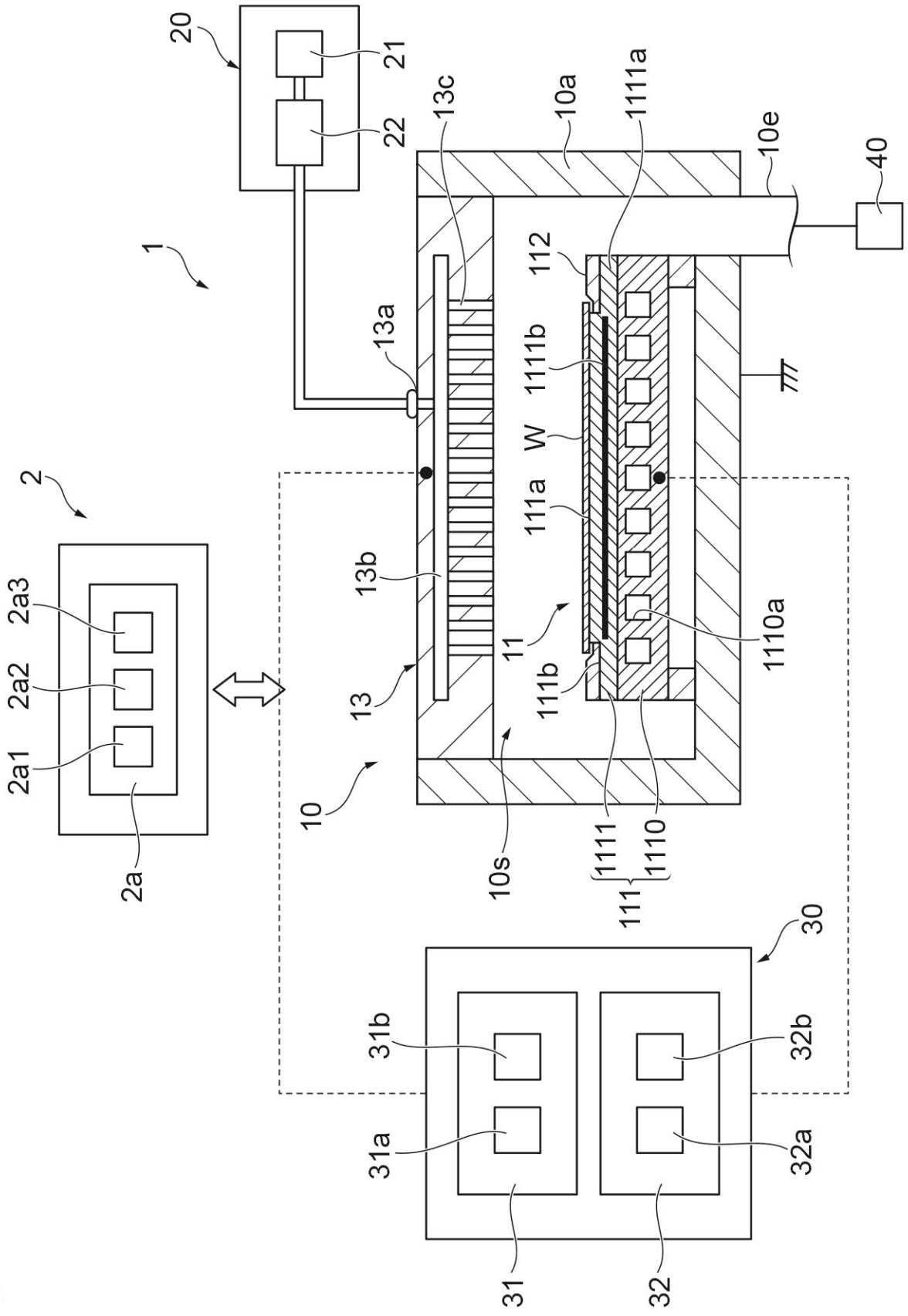
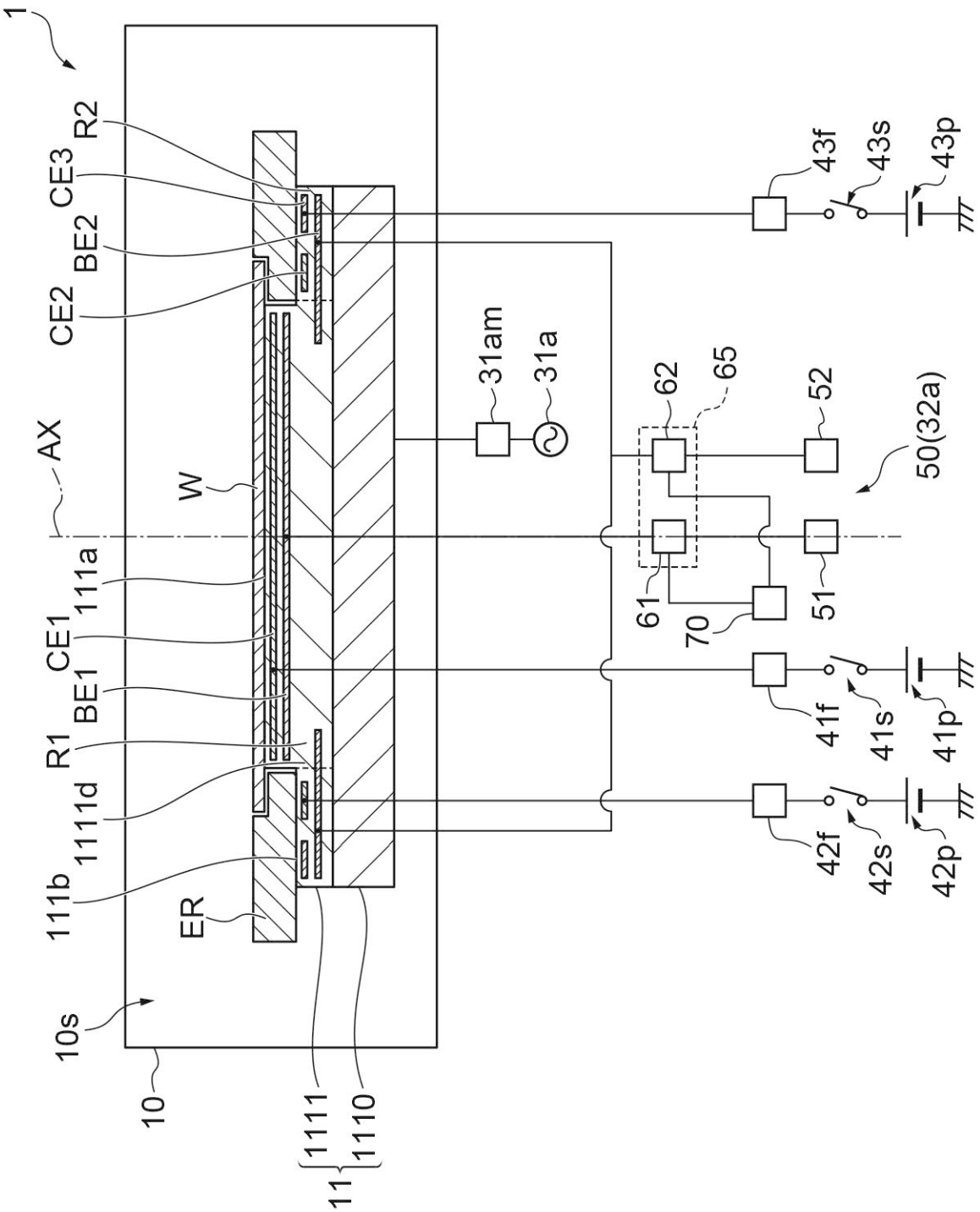

20
21
22
13c
10a
1111a
10e
40
1
112
13a
1111b
W
111a
2
13b
11
1110a
2a3
2a2
2a1
13
111b
10
10s
1111
1110
111
2a
30
31b
32b
31a
32a
31
32

Fig.2

Fig.3


1
R2
CE3
BE2
CE2
AX
W
111a
CE1
BE1
R1
1111d
111b
ER
10s
10
1111
1110
11
31am
31a
62
65
52
50(32a)
61
70
51
43f
43s
43p
41f
41s
41p
42f
42s
42p

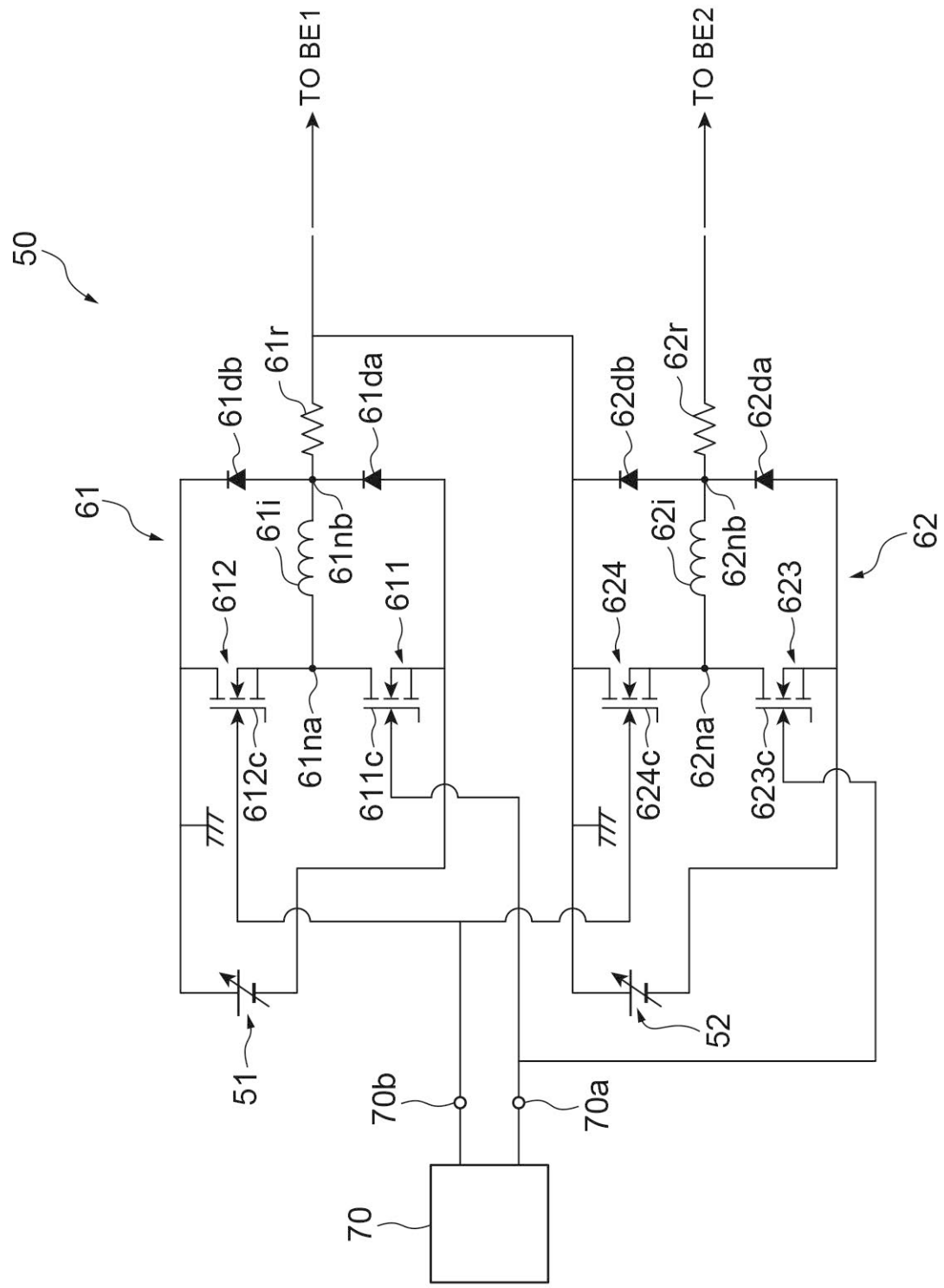

50
TO BE1
TO BE2
61
62
61r
62r
61db
61da
62db
62da
61i
61nb
62i
62nb
612
611
624
623
61na
62na
612c
611c
624c
623c
51
52
70b
70a
70

Fig.4

Fig.5

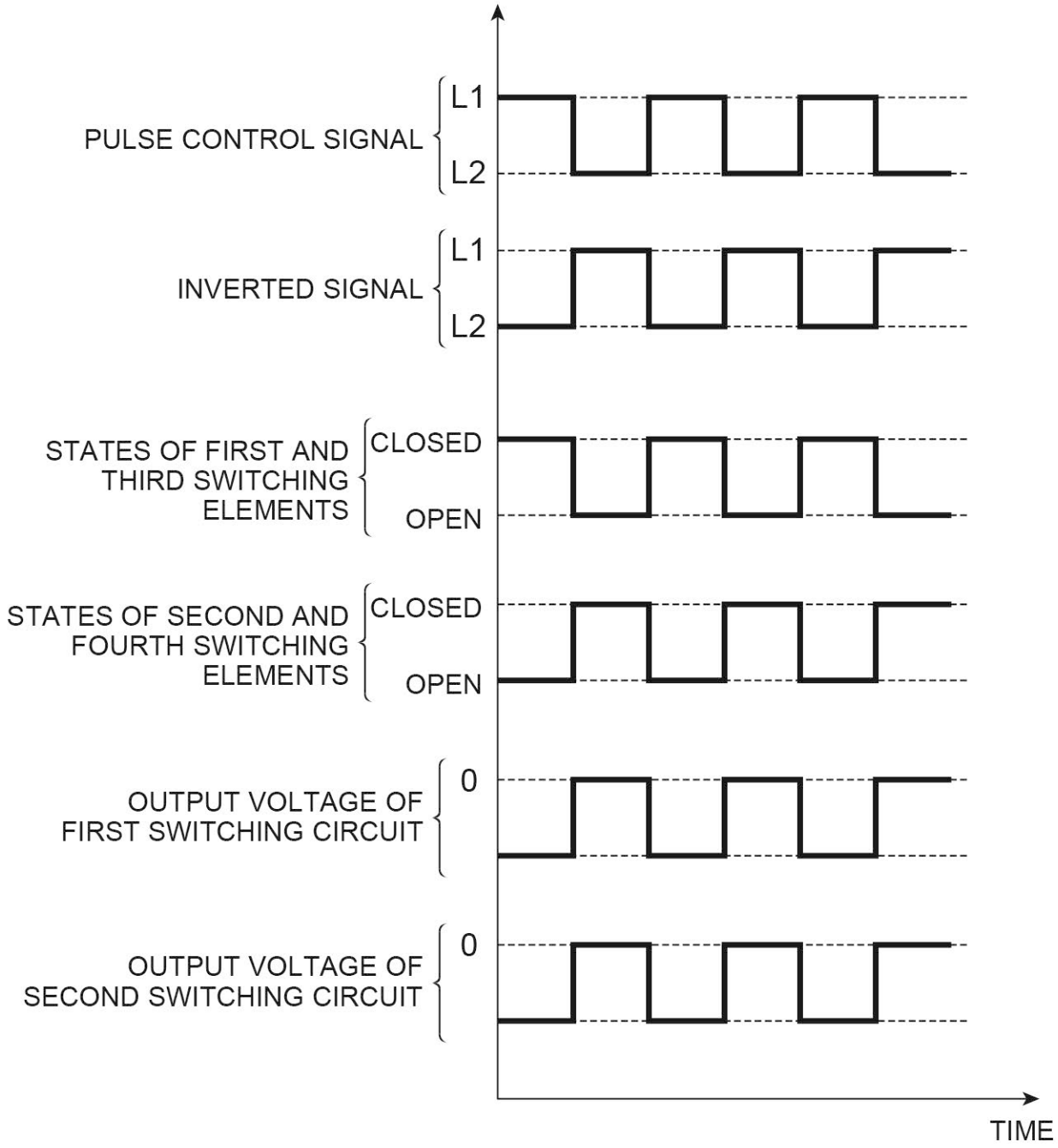

PULSE CONTROL SIGNAL
L1
L2
INVERTED SIGNAL
L1
L2
STATES OF FIRST AND THIRD SWITCHING ELEMENTS
CLOSED
OPEN
STATES OF SECOND AND FOURTH SWITCHING ELEMENTS
CLOSED
OPEN
OUTPUT VOLTAGE OF FIRST SWITCHING CIRCUIT
0
OUTPUT VOLTAGE OF SECOND SWITCHING CIRCUIT
0
TIME

Fig.6

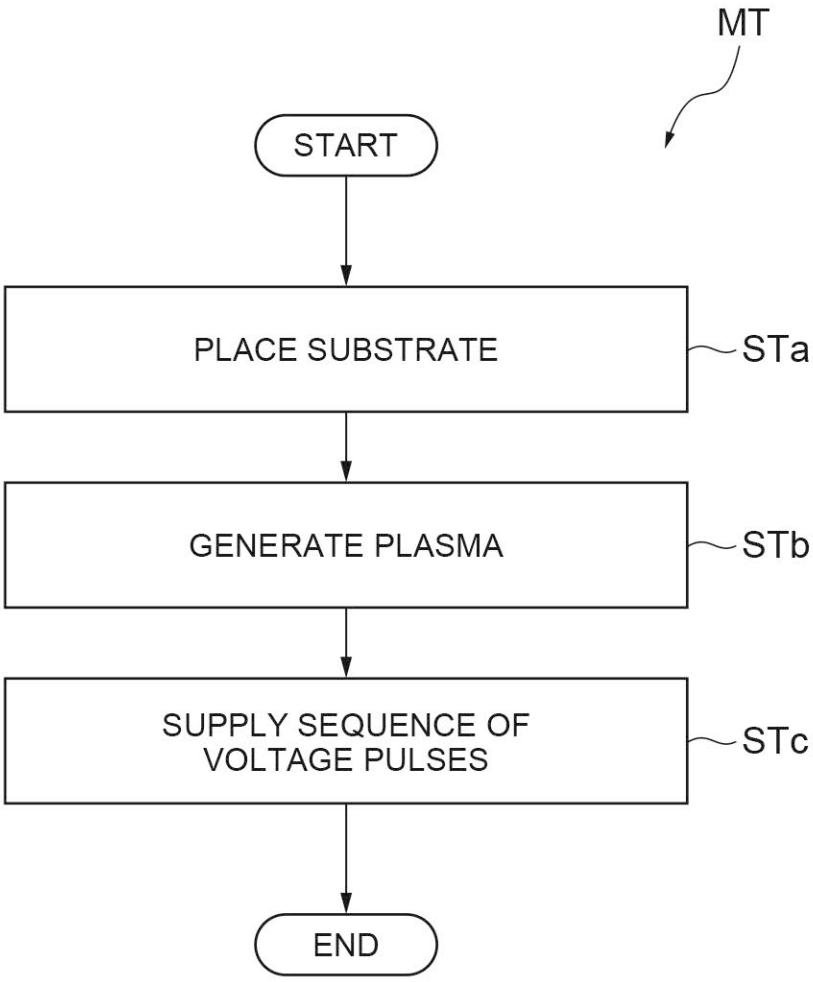

MT
START
PLACE SUBSTRATE
STa
GENERATE PLASMA
STb
SUPPLY SEQUENCE OF VOLTAGE PULSES
STc
END

Fig.7

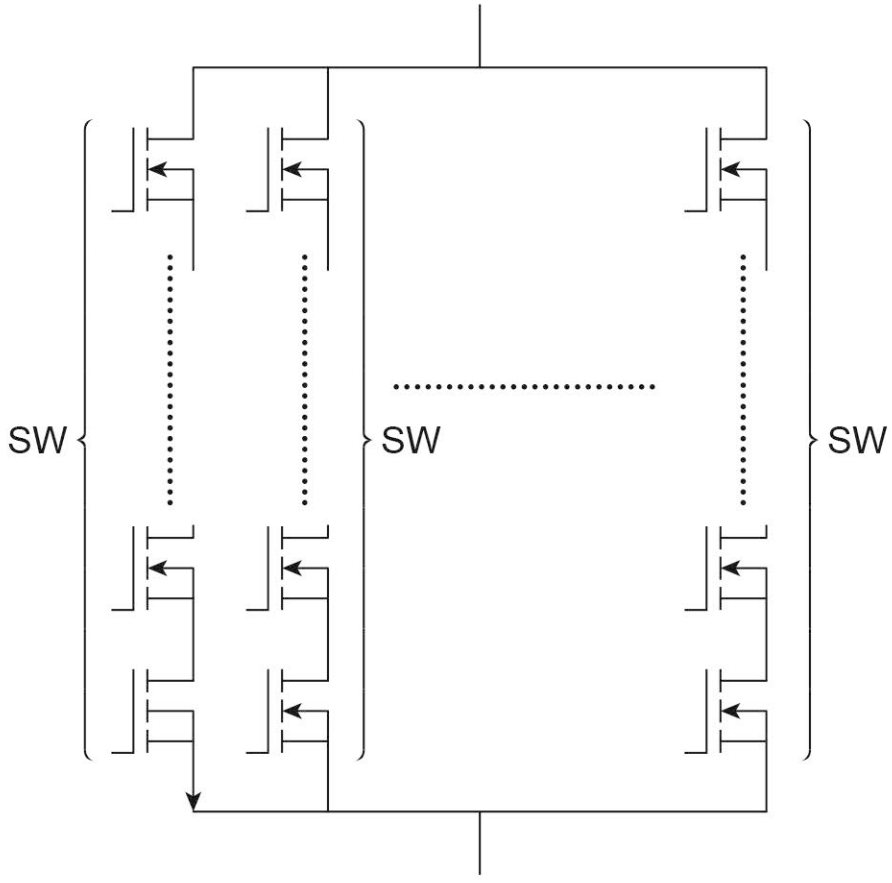


Fig.8

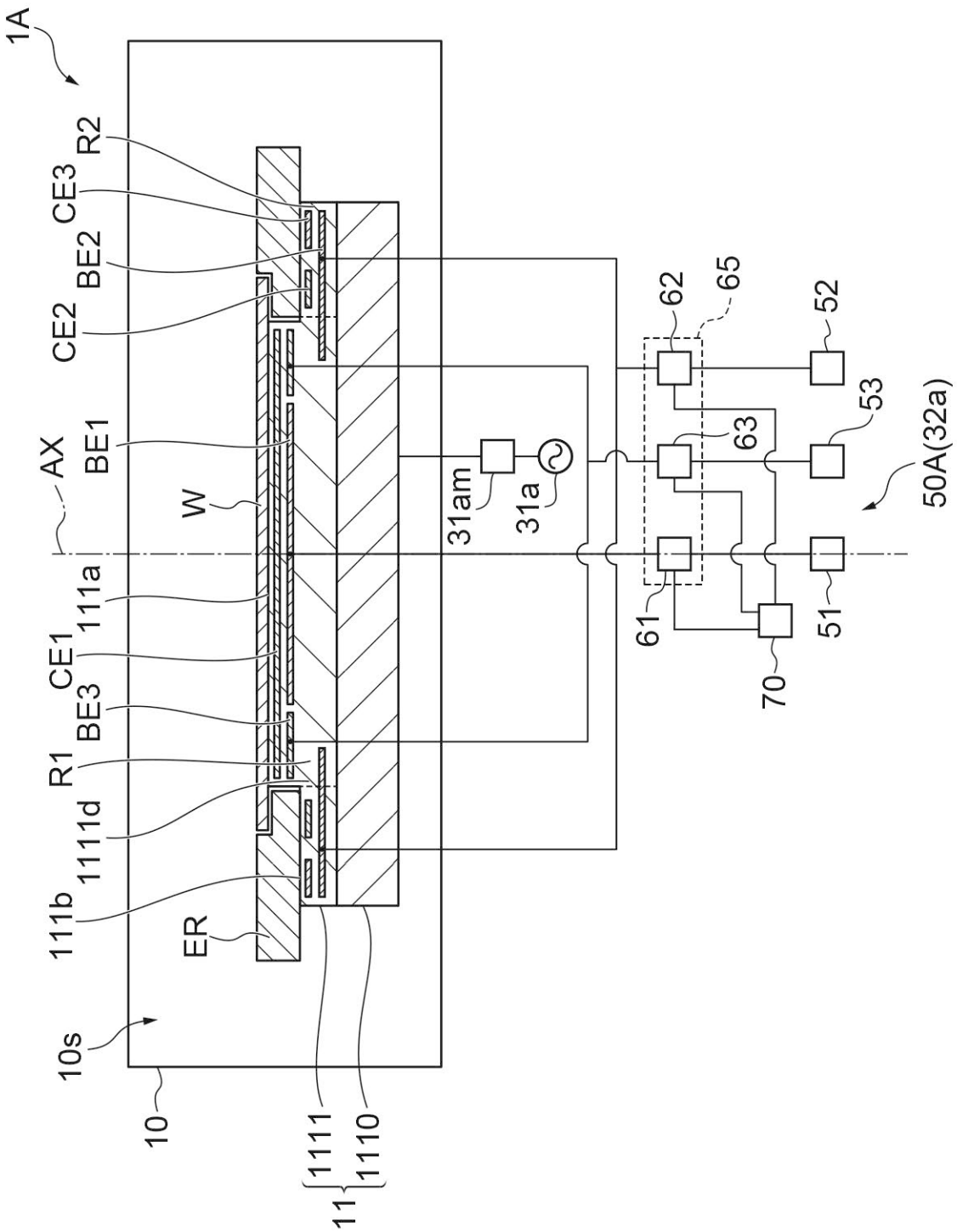
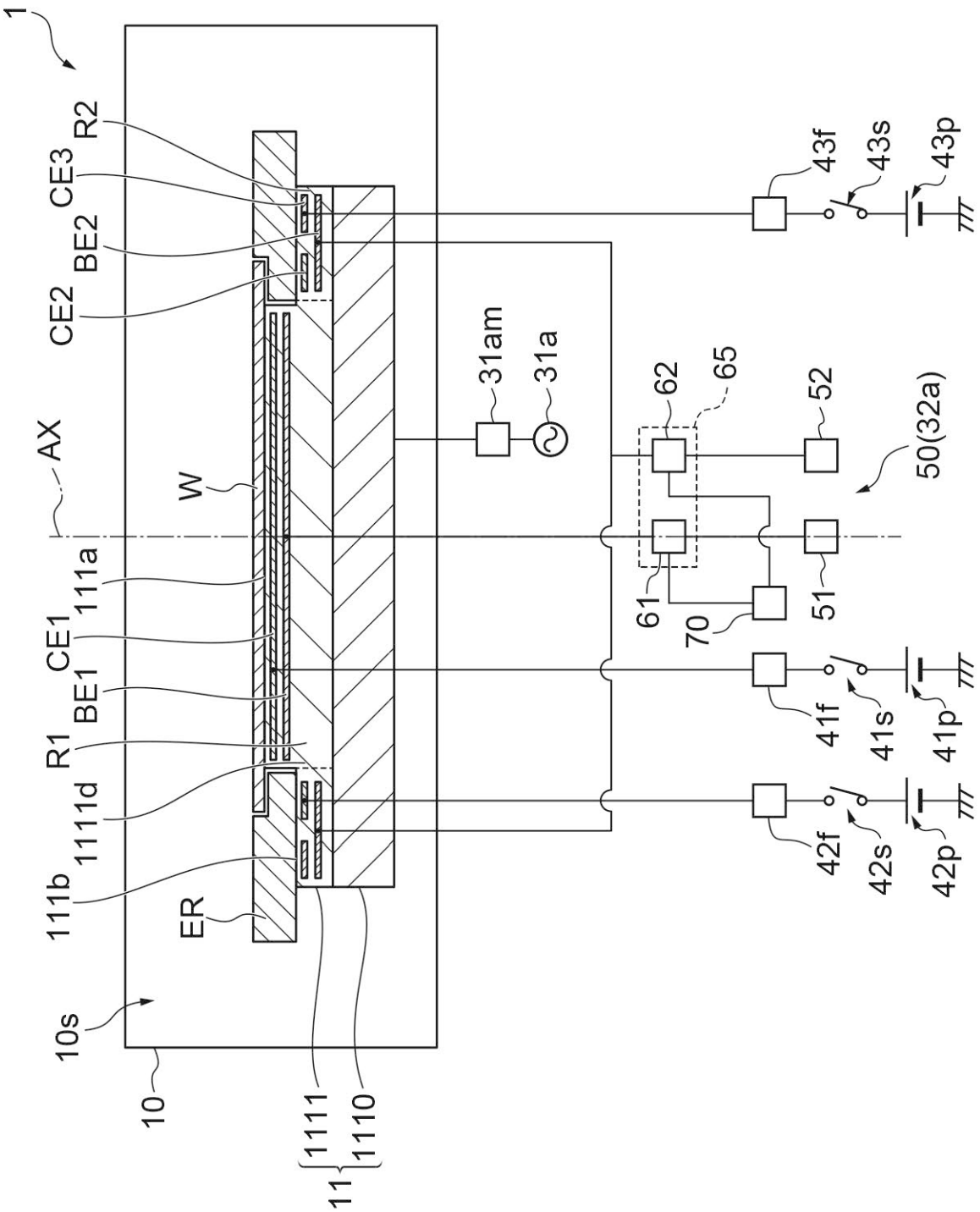

1A
R2
CE3
BE2
CE2
AX
BE1
W
CE1
111a
BE3
R1
1111d
111b
ER
10s
10
1111
1110
11
31am
31a
62
65
52
63
53
50A(32a)
61
51
70

Fig.9


1
R2
CE3
BE2
CE2
AX
W
111a
CE1
BE1
R1
1111d
111b
ER
10s
10
1111
1110
11
31am
31a
62
65
52
50(32a)
61
70
51
43f
43s
43p
41f
41s
41p
42f
42s
42p

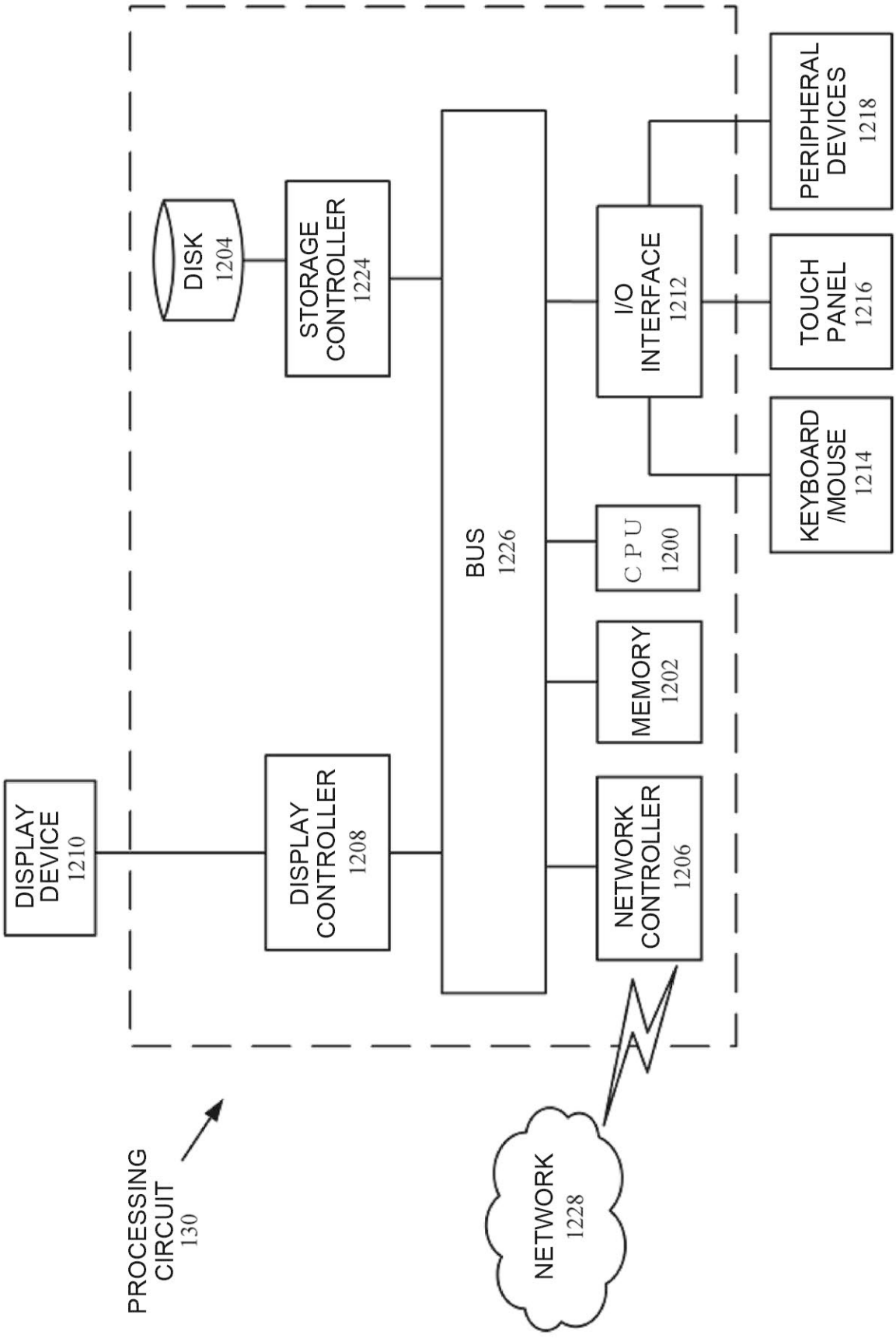

PROCESSING CIRCUIT 130
NETWORK 1228
DISPLAY DEVICE 1210
DISPLAY CONTROLLER 1208
DISK 1204
STORAGE CONTROLLER 1224
BUS 1226
NETWORK CONTROLLER 1206
MEMORY 1202
CPU 1200
I/O INTERFACE 1212
KEYBOARD /MOUSE 1214
TOUCH PANEL 1216
PERIPHERAL DEVICES 1218

Fig.10