METHOD AND APPARATUS TO REDUCE THERMAL VARIATIONS WITHIN AN INTEGRATED CIRCUIT DIE USING THERMAL PROXIMITY CORRECTION

ABSTRACT

A method (and semiconductor device) of fabricating a semiconductor device utilizes a thermal proximity correction (TPC) technique to reduce the impact of thermal variations during anneal. Prior to actual fabrication, a location of interest (e.g., a transistor) within an integrated circuit design is determined and an effective thermal area around the location is defined. Thermal properties of structures intended to be fabricated within this area are used to calculate an estimated temperature that would be achieved at the location of interest from a given anneal process. If the estimated temperature is below or above a predetermined target temperature (or range), TPC is performed. Various TPC techniques may be performed, such as the addition of dummy cells and/or changing dimensions of the structure to be fabricated at the location of interest (resulting in an modified thermally corrected design, to suppress local variations in device performance caused by thermal variations during anneal.

Fig.3