20000 6786-8

PCT WORLD INTELLECTUAL PROPERTY ORGANIZATION
International Bureau

INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification 6 : H01L 21/98, 25/18, 51/20 | A1

(11) International Publication Number: **WO 99/66551**

(43) International Publication Date: 23 December 1999 (23.12.99)

(21) International Application Number: PCT/NO99/00180

(22) International Filing Date: 2 June 1999 (02.06.99)

(30) Priority Data:
1) 19982518 2 June 1998 (02.06.98) NO

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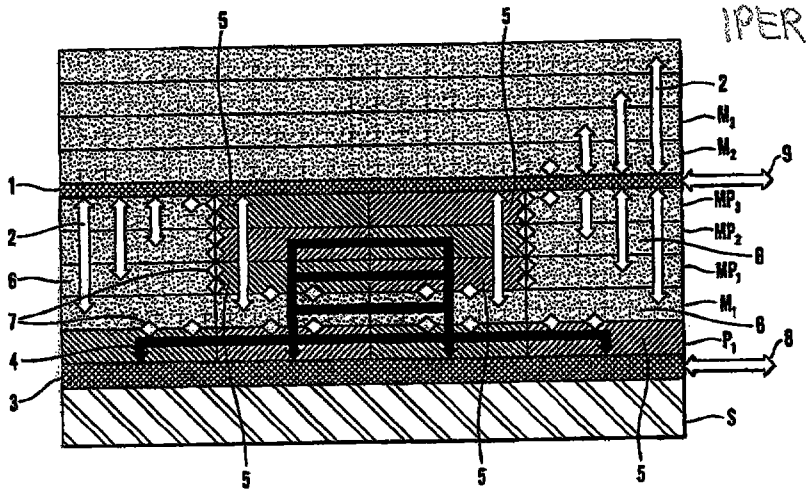
(81) Designated States: AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, CA, CH, CN, CU, CZ, DE, DK, EE, ES, FI, GB, GE, GH, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MD, MG, MK, MN, MW, MX, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TR, TT, UA, UG, US, UZ, VN, YU, ZA, ZW, ARIPO patent (GH, GM, KE, LS, MW, SD, SL, SZ, UG, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GW, ML, MR, NE, SN, TD, TG).

Published
With international search report.
Before the expiration of the time limit for amending the claims and to be republished in the event of the receipt of amendments.
In English translation (filed in Norwegian).

1 PD
1 appln. (See 16/306)
3 Invs.

(54) Title: SCALEABLE INTEGRATED DATA PROCESSING DEVICE

IPC : H01L 21/98
IPER 22/12/99.



(57) Abstract

A scaleable integrated data processing device, particularly a microcomputer, comprises a processing unit with one or more processors and a storage unit with one or more memories. The data processing device is provided on a carrier substrate (S) and comprises mutually adjacent substantially parallel layers (P, M, MP) stacked up on each other, the processing unit and the storage unit being provided in one or more such layers and the separate layers formed with a selected number of processors and memories in selected combinations. In each layer are provided horizontal electrical conducting structures which constitute electrical internal connections in the layer and besides each layer comprises further electrical conducting structures which provide electrical connections to other layers and to the exterior of the data processing device. The integrated data processing device has a scaleable architecture, such that it in principle can be configured with an almost unlimited processor and memory capacity. Particularly can the data processing device implement various forms of scaleable parallel architectures integrated with optimal interconnectivity in three dimensions.

This Sheet Has Been Replaced