ABSTRACT

A METHOD TO FORM MOS TRANSISTORS WITH A COMMON SHALLOW TRENCH ISOLATION AND INTERLEVEL DIELECTRIC GAP FILL

A new method of forming MOS transistors in the manufacture of an integrated circuit device has been achieved. A semiconductor substrate is provided. A pad oxide layer is deposited. A silicon nitride layer is deposited. Trenches are patterned for planned shallow trench isolations. The sidewalls of the trenches are oxidized. A photoresist layer is deposited overlying the silicon nitride layer and filling the trenches. The photoresist layer is etched down to below the top surface of the silicon nitride layer. The silicon nitride layer is patterned to form dummy gate electrodes. Sidewall spacers are formed on the dummy gate electrodes. The photoresist layer is removed. A dielectric layer is deposited overlying the dummy gate electrodes and the trenches. The dielectric layer is polished down to the top surface of the dummy gate electrodes to thereby complete the STI and the ILD. The dummy gate electrodes are etched away. A gate oxide layer is formed. A gate electrode layer is deposited overlying the dielectric layer and filling the openings for the planned transistor gates. The gate electrode layer is polished down to form the transistor gates, and the integrated circuit is completed.

FIGURE 3 IS SUGGESTED FOR PUBLICATION