

(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property
Organization
International Bureau

(43) International Publication Date
24 October 2024 (24.10.2024)



(10) International Publication Number
WO 2024/220121 A1

- (51) **International Patent Classification:**
H01L 23/00 (2006.01) *B24B 37/04* (2006.01)
C23C 18/16 (2006.01)
- (21) **International Application Number:**
PCT/US2024/012804
- (22) **International Filing Date:**
24 January 2024 (24.01.2024)
- (25) **Filing Language:** English
- (26) **Publication Language:** English
- (30) **Priority Data:**
18/304,626 21 April 2023 (21.04.2023) US
- (71) **Applicant: APPLIED MATERIALS, INC.** [US/US];
3050 Bowers Avenue, Santa Clara, California 95054-3299
(US).
- (72) **Inventor: BERNT, Marvin L.**; c/o Applied Materials, Inc.,
3050 Bowers Avenue, Santa Clara, California 95054-3299
(US).

(74) **Agent: FAIRCHILD, Taylor P.** et al.; 1201 Third Avenue,
Suite 3600, Seattle, Washington 98101 (US).

(81) **Designated States** (*unless otherwise indicated, for every kind of national protection available*): AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CV, CZ, DE, DJ, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IQ, IR, IS, IT, JM, JO, JP, KE, KG, KH, KN, KP, KR, KW, KZ, LA, LC, LK, LR, LS, LU, LY, MA, MD, MG, MK, MN, MU, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, WS, ZA, ZM, ZW.

(84) **Designated States** (*unless otherwise indicated, for every kind of regional protection available*): ARIPO (BW, CV, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SC, SD, SL, ST, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT,

(54) **Title: PROCESS FOR THIN ELECTROLESS DEPOSITION**

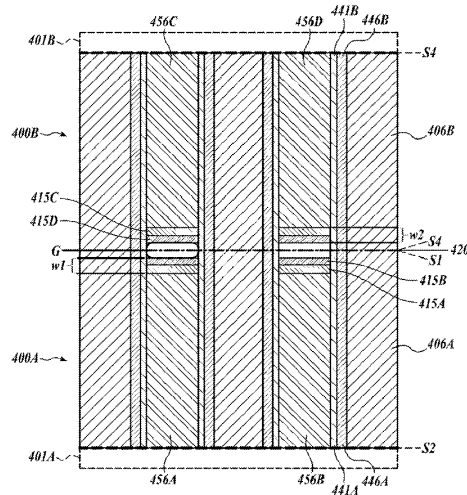


FIG. 4A

(57) **Abstract:** A wafer-to-wafer assembly, including a first wafer having a dielectric, the dielectric having a first side and a second side, opposite the first side, at least one opening etched into first side of the dielectric, a plug seed layer disposed on the first side of the dielectric, a plug disposed in the at least one opening, a first thin layer deposited over the plug, and a second thin layer deposited over the first thin layer. The first thin layer, the second thin layer, or both the first thin layer and the second thin layer is deposited with electroless deposition. Further, a method of wafer-to-wafer bonding with the wafer-to-wafer assembly.

[Continued on next page]

LU, LV, MC, ME, MK, MT, NL, NO, PL, PT, RO, RS, SE,
SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN,
GQ, GW, KM, ML, MR, NE, SN, TD, TG).

Declarations under Rule 4.17:

- *as to applicant's entitlement to apply for and be granted a patent (Rule 4.17(ii))*
- *as to the applicant's entitlement to claim the priority of the earlier application (Rule 4.17(iii))*

Published:

- *with international search report (Art. 21(3))*
- *with amended claims (Art. 19(1))*