

Description

The invention relates to an amplifier arrangement comprising a first amplifier having a first output terminal for connection to a first terminal of a load, and having at least a first transistor for supplying a first current related to a first load current flowing via the first output terminal, first means for generating a first signal which is a measure of the first current, a second amplifier having a second output terminal for connection to a second terminal of the load, and having at least a second transistor for supplying a second current related to a second load current flowing via the second output terminal, second means for generating a second signal which is a measure of the second current, and protection means for limiting the first and the second load current in order to protect the first and the second amplifier.

In general, such an amplifier arrangement can be used for driving a load coupled between two amplifiers, which amplifiers are protected against supplying excessive load currents, and in particular the arrangement is suitable for use in car radios, where short circuits to earth always constitute a problem.

Such an amplifier arrangement is generally known because most amplifier arrangements comprise a protection device for protecting the amplifiers used in the arrangement. This protection device comprises means for generating one or more signals which are each a measure of a current or voltage related to the load currents and also comprises protection means which are responsive to said signals to limit the load currents. In amplifier arrangements of the type defined in the opening paragraph the two amplifiers are each protected in a substantially identical way. One possibility of implementing the protection of an amplifier is disclosed in European Patent Application 0,132,863. In said amplifier the means generate two signals, which are measures of a load-current-related current and voltage respectively, and the protection means comprise a control amplifier. This control amplifier is driven if the difference between the two signals exceeds a threshold value and thereby limits the amplifier drive and thus the load current. The known protection devices protect the amplifiers against short-circuits to earth, but comparatively small short-circuit currents are not detected. These short-circuit currents give rise to a loss of power and may cause thermal damage to the amplifier arrangement.

Therefore, it is an object of the invention to provide an amplifier arrangement which comprises both amplifiers and a protection device and which is capable of detecting short-circuits independently of the magnitudes of the short-circuit currents.

An amplifier arrangement in accordance with the invention is characterized in that the amplifier arrangement further comprises third means for gener-

ating a first control signal which is a measure of the sum of the first and the second signal and which serves for controlling the protection means.

The invention is based on the recognition of the fact that when a short-circuit current occurs the first and the second load current are no longer equal and that this deviation can be detected by comparing the first and the second signal with each other, which signals are related to the first and the second load current. By this comparison and with the aid of the third means the first control signal for controlling the protection means is obtained.

IEEE Journal of Solid State Circuits, Vol. SC-18, No. 6, December 1983, New York, USA; pages 665-677, "Integrated Electronic Subscriber Line Interface Circuit with Ringing on Chip", by R.M. Sirsi et al. discloses first and second means for generating first and second signals which are summed in third means for generating a first control signal which is a measure of the sum of the first and the second signal. However, the first control signal is used for controlling a circuit having a technical function and purpose which differs from the technical function and purpose of a protection means for limiting the load currents.

A first embodiment of an amplifier arrangement in accordance with the invention may be characterized in that the third means comprise a current mirror having an input terminal for receiving the first and second signals and an output terminal for supplying the first control signal, the input terminal of the current mirror and the output terminal of the current mirror being coupled to one another by means of two series-coupled transistors each having a control electrode, a first main electrode and a second main electrode, the two control electrodes being coupled to a reference-voltage terminal to receive a reference voltage, the two first main electrodes being coupled to the input terminal to receive both the first and the second signal, and the second main electrodes being coupled to the input terminal and the output terminal respectively. This embodiment enables the sum of the first and the second signal to be formed in a simple manner. When the two series-coupled transistors are used the voltage on the third terminal, in relation to the reference voltage, dictates the magnitude of the control signal, which is a measure of the current via the third terminal.

A second embodiment of an amplifier arrangement in accordance with the invention may be characterized in that the first means comprise at least two transistors each having a control electrode, a first main electrode and a second main electrode, the control electrodes being coupled both to one another and to one first main electrode, the first main electrodes each being coupled to a current source, and the second main electrodes being coupled to one another by means of a pair of series-coupled resistors, one second main electrode being coupled to an input terminal

to receive at least the first current and the other second main electrode being coupled to an output terminal to supply the first signal, and in that the second means comprise at least two transistors each having a control electrode, a first main electrode and a second main electrode, the control electrodes being coupled both to each other and to one first main electrode, the first main electrodes each being coupled to a current source, and the second main electrodes being coupled to one another by means of a second pair of series-coupled resistors, one second main electrode being coupled to an input terminal to receive at least the second current and the other second main electrode being coupled to an output terminal to supply the second signal. Both in the first and in the second means the two transistors with the associated resistors pair constitute a degenerate current mirror, in which the currents through the transistors are dictated by the current sources and in which the voltages across the resistors as well as the values of the resistors determine the ratio between the first current and the first signal and the ratio between the second current and the second signal.

A third embodiment of an amplifier arrangement in accordance with the invention may be characterized in that the first amplifier further comprises at least a third transistor for supplying a third current related to the first load current flowing via the first output terminal, the first means are adapted to generate also a third signal which is a measure of the third current, the second amplifier further comprises at least a fourth transistor for supplying a fourth current related to the second load current flowing via the second output terminal, the second means are adapted to generate also a fourth signal which is a measure of the fourth current, and the third means are adapted to generate also a second control signal which is a measure of the sum of the third and the fourth signal and which serves to control the protection means, which third means may be characterized further in that they comprise two substantially identical devices for generating the first and the second control signal respectively. The first and the second means may be characterized further in that the first means further comprise at least two transistors each having a control electrode, a first main electrode and a second main electrode, the control electrodes being coupled both to each other and to one first main electrode, the first main electrodes each being coupled to a current source, and the second main electrodes being coupled to each other by means of a third pair of series-coupled resistors, one second main electrode being coupled to an input terminal to receive the third current and the other second main electrode being coupled to an output terminal to supply the third signal, and in that the second means comprise at least two transistors each having a control electrode, a first main electrode and a second main electrode, the con-

trol electrodes being coupled both to one another and to one first main electrode, the first main electrodes each being coupled to a current source, and the second main electrodes being coupled to one another by means of a fourth pair of series-coupled resistors, one second main electrode being coupled to an input terminal to receive the fourth current and the other second main electrode being coupled to an output terminal to supply the fourth signal. In this embodiment the first and the second amplifier constitute a bridge amplifier comprising at least four transistors. The currents through these transistors are related to the first or the second load current and serve as measures of the four signals which control the protection means via the third means.

A fourth embodiment of an amplifier arrangement in accordance with the invention may be characterized in that the first amplifier further comprises at least a third transistor for supplying a third current, related to the first load current flowing via the first output terminal, and the second amplifier further comprises at least a fourth transistor for supplying a fourth current related to the second load current flowing via the second output terminal, and in that the first signal is a measure of both the first and the fourth current and the second signal is a measure of both the second and the third current. The first and the second amplifier again form a bridge amplifier. By applying the first and the fourth current to the first means and by applying the second and the third current to the second means the number of components is reduced as compared with the third embodiment. Now the first, the second and the third means may be constructed as described for the first and the second embodiment, the two current pairs each driving the degenerate current mirror via a resistor.

A further embodiment of an amplifier arrangement in accordance with the invention may be characterized in that at least one of the means is further adapted to generate at least one further control signal which is a measure of one of the currents through the transistors and which serves for controlling the protection means. The use of a larger number of control signals enables the currents through the four transistors to be also limited in an absolute sense. This is in order to prevent both the amplifiers and the load from being overloaded.

The invention will now be described in more detail, by way of example, with reference to the accompanying drawings in which

Fig. 1 is a first block diagram of an amplifier arrangement in accordance with the invention,

Fig. 2 shows an example of the first means for an amplifier arrangement in accordance with the invention,

Fig. 3 shows an example of the second means for an amplifier arrangement in accordance with the invention,

Fig. 4 shows an example of the third means for an amplifier arrangement in accordance with the invention,

Fig. 5 is a second block diagram of an amplifier arrangement in accordance with the invention,

Fig. 6 shows a substantially mirror-symmetrical part of a bridge amplifier arrangement in accordance with the invention,

Fig. 7 shows a third block diagram of an amplifier arrangement in accordance with the invention, and

Fig. 8 shows an embodiment of a complete bridge amplifier arrangement in accordance with the invention.

Fig. 1 shows a first block diagram of an amplifier arrangement in accordance with the invention. The arrangement comprises a first amplifier A1, a second amplifier A2 and a protection device comprising first means M1, second means M2, third means M3 and protection means B. The first amplifier A1 has an input terminal for receiving an input signal Vin1, an output terminal 5 for connection to a first terminal of a load, and a terminal 7 to which the first means M1 are connected. The second amplifier A2 has an input terminal 2 for receiving an input signal Vin2, an output terminal 6 for connection to a second terminal of the load, and a terminal 8 to which the second means M2 are connected. The third means M3 are coupled to the first means M1 via a terminal 11, to the second means M2 via a terminal 12, and to the protection means B via both a terminal 15 and a terminal 16. The protection means B are coupled both to the first amplifier A1 and to the second amplifier A2. When a load is coupled between the two output terminals 5 and 6 and the two amplifiers A1 and A2 are driven with the input signals Vin1 and Vin2 respectively a first load current will flow via the output terminal 5 and a second load current will flow via the output terminal 6. Moreover, a current i1 related to the first load current will flow via the terminal 7 and a current i2 related to the second load current will flow via the terminal 8. The currents i1 and i2 may each be, for example, a main electrode current of an output transistor. The first and the second means M1 and M2 are responsive to these currents i1 and i2, respectively to generate a signal s1 and s2 respectively. These signals s1 and s2 are applied to the third means M3 via the terminals 11 and 12 respectively, in which third means the signals s1 and s2 are compared and in which a control signal r1 is generated. This control signal r1 is equal to the sum, or the difference, of the signals s1 and s2. The control signal r1 controls the protection means B via the terminals 15 and 16, which protection means influence the amplifiers A1 and A2 if necessary. In the absence of a short-circuit of the output terminals 5 and 6 to one of the supply voltage terminals the two load currents are equal and opposite so that the currents i1 and i2 are substantially equal in an absolute

sense, which also applies to the signals s1 and s2. Consequently, the control signal r1 is substantially zero and the protection means B receive no drive. In the case of a short-circuit the control signal r1 is not zero. The protection means B are then controlled by the control signal r1 in order to protect the amplifiers A1 and A2. Moreover, the control signal r1 can be used for generating a warning signal, for example by means of a lamp.

Fig. 2 shows an example of the first means M1 for an amplifier arrangement in accordance with the invention, like parts bearing the same reference numerals as in Fig. 1. A transistor T1 and a transistor T2 form a current mirror, the first main electrode of the transistor T1 being coupled both to a supply voltage terminal Vdd via a resistor R11 and to the terminal 7, and the first main electrode of the transistor T2 being coupled both to the supply voltage terminal Vdd via a resistor R12 and to the second main electrode of a transistor T3, whose first main electrode is coupled to the terminal 11 and whose control electrode is coupled to the second main electrode of the transistor T2. The control electrodes of the transistors T1 and T2 are coupled to each other and are connected to the second main electrode of the transistor T1. Moreover, this embodiment comprises a second current mirror comprising the transistors T4, T5 and T6, whose control electrodes are coupled to each other and are connected both to the supply voltage terminal Vdd via a current source J1 and to the second main electrode of the transistor T4 and whose first main electrodes are coupled to a supply voltage terminal Vss. The transistors T5 and T6 have their second main electrodes coupled to the second main electrode of the transistor T1 and of the transistor T2 respectively. The transistors T5 and T6 each form a current source and respectively dictate the currents through the transistors T1 and T2 and the voltages across the first main electrode and the control electrode of the transistors T1 and T2. These voltages determine the ratio between the voltages across the resistors R11 and R12 in that the transistors T1 and T2 have their control electrodes coupled to each other and have their first main electrodes coupled to the supply voltage terminal Vdd via the resistors R11 and R12, respectively. In addition to the currents defined by the transistors T5 and T6 respectively, the current i1, which is related to the first load current, and the signal s1, which is applied to the third means M3, flow through the resistors R11 and R12. Since the ratio between the voltages across the resistors R11 and R12 is maintained equal by the bias currents of the transistors T1 and T2, a variation of the current i1 will result in a related variation of the signal s1. Consequently, the signal s1 is a measure of the current i1 and of the first load current. If the values of the resistors R11 and R12 are not equal it is possible to compensate for an offset in the transfer of the current i1 to the signal s1 by means of

a resistor arranged in series with one of the first main electrodes of the transistors T1 and T2. For this purpose the arrangement shown in Fig.2 comprises, for example, a resistor R13 arranged in series with the first main electrode of the transistor T1, in order to obtain an improved quiescent current setting. The transistor T3 provides independence of the voltage on the terminal 1 and of the magnitude of the current flowing via the terminal 11.

Fig. 3 shows an example of the second means M2 for an amplifier arrangement in accordance with the invention, like parts bearing the same reference numerals as in the preceding Figures. In the present arrangement a transistor T7 and a transistor T8 form a current mirror. The first main electrode of the transistor T7 is coupled both to the supply voltage terminal Vss via a resistor R21 and to the terminal 8, and the first main electrode of the transistor T8 is coupled both to the supply voltage terminal Vss via a resistor R22 and to the second main electrode of a transistor T9, whose first main electrode is coupled to the terminal 12 and whose control electrode is coupled to the second main electrode of the transistor T8. The control electrodes of the transistors T7 and T8 are coupled to one another and are connected to the second main electrode of the transistor T7. This embodiment further comprises a second current mirror comprising the transistors T10, T11 and T12, whose control electrodes are coupled to one another and are connected both to the supply voltage terminal Vss via a current source J2 and to the second main electrode of the transistor T10 and whose first main electrodes are coupled to the supply voltage terminal Vdd. The second main electrodes of the transistors T11 and T12 are coupled to the second main electrodes of the transistor T7 and that of the transistor T8, respectively. The arrangement shown in Fig. 3 only differs from the arrangement shown in Fig. 2 in that the supply voltages Vdd and Vss have been interchanged and in that transistors of another type have been used. However, the two arrangements operate in a similar way, so that it is easy to see that the signal s2 flowing via the terminal 12 is a measure of the current i2 which flows via the terminal 8 and which is related to the second load current. In order to obtain an improved quiescent current setting it is also possible to arrange a resistor R23 in series with the first main electrode of the transistor T7 in the present embodiment.

Fig. 4 shows an example of the third means M3 for an amplifier arrangement in accordance with the invention, like parts again bearing the same reference numerals as in the preceding Figures. A transistor T13 and a transistor T14 constitute a current mirror. The first main electrodes of said transistors are coupled to the supply voltage terminal Vss. Moreover, this embodiment comprises two series-connected transistors T15 and T16, whose main electrodes are both coupled to the terminal 11 and the terminal 12

and whose control electrodes are both coupled to a reference voltage terminal 20 to receive a reference voltage Vref1. The second main electrode of the transistor T15 is coupled both to the second main electrode of the transistor T14 and to the terminals 15 and 16. The second main electrode of the transistor T16 is coupled to the second main electrode of the transistor T13 and to the control electrodes of the transistors T13 and T14. This circuit forms the sum of the signal s1 flowing via the terminal 11 and the signal s2 flowing via the terminal 12. Since the signals s1 and s2 have opposite polarities as a result of the mutual orientation of the current mirrors in the means M1 and M2, the control signal r1 flowing via the terminals 15 and 16 represents the sum of the signals s1 and s2. The control signal R1 serves to control the protection means B. It is not necessary to utilize a threshold circuit. Depending on the polarity of the current applied to the first main electrodes of the transistors T15 and T16 resulting from the summation of the opposite signals s1 and s2, one of the transistors will conduct. In the case of a current flowing away from the two first main electrodes the transistor T15 will conduct and the transistors T13, T14 and T16 will be cut off. The current through the transistor T15 will then be substantially equal to the control signal r1. In the case of a current which flows to the two first main electrodes the transistor T16 will conduct and the transistor T15 will cut off. By means of the current mirror comprising the transistors T13 and T14 the control signal r1 will then be dictated by the current through the transistor T16. In this embodiment the polarity of the control signal r1 is identical in both cases.

Fig. 5 shows a second block diagram of an amplifier arrangement in accordance with the invention, like parts bearing the same reference numerals as in the preceding Figures. In comparison with Fig. 1 this block diagram has some extensions. For example, the first amplifier A1 comprises both an input terminal 3 for receiving an input signal Vin3 and a terminal 9, to which the first means M1 are connected, and the second amplifier A2 comprises both an input terminal 4 for receiving an input signal Vin4 and a terminal 10, to which the second means M2 are connected. Moreover, the first means M1 and the second means M2 are coupled to the third means M3 via a terminal 13 and a terminal 14 respectively, which third means M3 are also coupled to the protection means B via a terminal 17 and a terminal 18. The amplifiers A1 and A2 each comprise two amplifier elements which are each driven by an input signal. The amplifier elements of the amplifier A1 are each coupled to the protection means B and each supply a portion of the first load current, the current i1 being related to one portion and the current i3 flowing via the terminal 9 being related to the other portion. Each of the amplifier elements of the amplifier A2 is also coupled to the protection means B. They each supply a portion of the

second load current, the current i_2 being related to one portion and the current i_4 flowing via the terminal 10 being related to the other portion. The first means M1, in relation to the currents i_1 and i_3 , generate the signal s_1 and a signal s_3 flowing via the terminals 11 and 13, respectively. The second means, in relation to the currents i_2 and i_4 generate the signal s_2 and a signal s_4 flowing via the terminals 12 and 14, respectively. The third means M3 derive from the signals s_1 and s_2 the control signal r_1 and from the signals s_3 and s_4 a control signal r_2 flowing via the terminals 17 and 18. These control signals are employed by the protection means B in order to protect the amplifier elements. Thus, the currents i_3 and i_4 are processed similarly to the currents i_1 and i_2 . This amplifier arrangement is very suitable for use in a bridge amplifier arrangement having a push-pull output stage.

Fig. 6 shows an example of a substantially mirror-symmetrical part of a bridge amplifier arrangement in accordance with the invention, like parts again bearing the same reference numerals as in the preceding Figures. This embodiment is based on one half of the block diagram shown in Fig. 5. In this embodiment the amplifier elements of the first amplifier A1 are constituted by a transistor PT1 having its control electrode coupled to the terminal 1, its first main electrode to the output terminal 5 and its second main electrode to the terminal 7, and a transistor PT3 having its control electrode coupled to the terminal 3, its first main electrode to the terminal 9 and its second main electrode to the output terminal 5. The first means M1 comprise a circuit comprising two sections, of which the first section 30 corresponds to the arrangement shown in Fig. 2 and the other section 40 corresponds to the arrangement shown in Fig. 3, comprising some additional elements. For example, the control electrode and the second main electrode of the transistor T1 are coupled to each other by means of a transistor T27 which has its first and its second main electrode connected to respectively the second main electrode and the control electrode of the transistor T1 and which has its control electrode coupled to a reference voltage terminal 21 to receive a reference voltage V_{ref2} . In addition, the first main electrode of a transistor T18 and the second main electrode of a transistor T19 are coupled to each other by means of a resistor R34 and a transistor T28. Together with a transistor T29 the transistor T28 constitutes a current mirror for generating a control signal r_3 , which is related to the signal s_3 . For this purpose the transistor T29 has its first main electrode coupled to the supply voltage terminal V_{ss} via a resistor R35, its second main electrode to the terminal 19 and its control electrode to the second main electrode of the transistor T19 and to the interconnected second main electrode and control electrode of the transistor T28, which has its first main electrode coupled to the first main electrode of the transistor T18 by the resistor

R34. The third means M3 in Fig. 6 comprise a circuit corresponding to that shown in Fig. 4. In the complete amplifier arrangement the third means M3 should comprise at least two of said circuits and both the second amplifier A2 and the second means M2 will be substantially identical to the first amplifier A1 and the first means M1 respectively. The additional transistor T27 reduces the effect of supply-voltage variations on the currents through the transistors T1 and T2. The control signal R_3 generated by the additional current mirror (T28, T29) directly constitutes a measure of the current supplied to the load by the transistor PT3 and will drive the protection means B via a threshold circuit in the case of an overload. Thus, the control signal R_3 protects both the amplifier and the load against excessive currents. For the remainder, the operation of the amplifier arrangement is similar to that described with reference to the preceding Figures.

Fig. 7 shows a third block diagram of an amplifier arrangement in accordance with the invention like parts bearing the same reference numerals as in the preceding Figures. This block diagram represents a bridge amplifier, for which purpose the two amplifiers A1 and A2 again comprise two amplifier elements each. This bridge amplifier can be protected by means similar to those in the amplifiers A1 and A2 in Fig. 1 and is a simplified version of that shown in Fig. 5. The first means M1 receive the current i_1 and the current i_4 via the terminals 7 and 10 respectively to generate the signal s_1 . The second means M2 receive the current i_2 and the current i_3 via the terminals 8 and 9 respectively to generate the signal s_2 . By means of the signals s_1 and s_2 the third means M3 produce a control signal r_1 with which the protection means B are controlled via the terminals 15 and 16. In a practical embodiment of this block diagram the terminals 7 and 10 may be coupled to each other, so that the currents i_1 and i_4 both flow through the resistor R11, as employed for example in the arrangement shown in Fig. 2. The terminals 8 and 9 may also be coupled to one another, so that the currents i_2 and i_3 both flow through the resistor R21 as used for example in the arrangement shown in Fig. 3. The operation of the arrangement is similar to that of the arrangements shown in the preceding Figures.

Fig. 8 shows an embodiment of a complete bridge amplifier arrangement in accordance with the invention, like parts bearing the same reference numerals as in the preceding Figures. This embodiment is based on the block diagram shown in Fig. 7. Herein the amplifier elements of the second amplifier A2 comprise a transistor PT2, having its control electrode coupled to the terminal 2, having its first main electrode coupled to the output terminal 6 and having its second main electrode coupled to the terminal 8, and a transistor PT4, having its control electrode coupled to the terminal 4, having its first main electrode

coupled to the terminal 10 and having its second main electrode coupled to the output terminal 6. The first means M1 comprise a circuit as shown in Fig. 2 but in which the second current mirror (T4, T5, T6) has been replaced by a current source J5 coupled to the second main electrode of the transistor T1 and by a current source J6 coupled to the second main electrode of the transistor T2. The transistor T27 is added again and the main electrodes of the transistors T1 and T2 are further coupled both the terminal 10 and the supply-voltage terminal Vdd by means of a set of resistors R41, R42 and R43. The second means M2 comprise a circuit as shown in Fig. 3, but in which the second current mirror (T10, T11, T12) has been replaced by a current source J11 coupled to the second main electrode of the transistor T7 and by a current source J12 coupled to the second main electrode of the transistor T8. The first main electrodes of the transistors T7 and T8 are further coupled to both the terminal 9 and the supply-voltage terminal Vss by a set of resistors R31, R32 and R33. The third means M3 comprise a circuit as shown in Fig. 4. The present embodiment provides a simple method of protecting a bridge amplifier arrangement, the operation of this embodiment not being different from that of the embodiments described with reference to the preceding Figures.

The first means M1 and the second means M2 can be constructed in a variety of ways, which also applies to the third means M3, which need not necessarily receive two signals of opposite polarity. However, in that case a threshold circuit is required, which may operate with a variable related threshold value.

Claims

1. An amplifier arrangement comprising a first amplifier (A1) having a first input terminal (1) and a first output terminal (5), the latter being for connection to a first terminal of a load and having at least a first transistor (PT1) for supplying a first current (I1) related to a first load current flowing via the first output terminal (5), a second amplifier (A2) having a second input terminal (2) and a second output terminal (6), the latter being for connection to a second terminal of the load and having at least a second transistor (PT2) for supplying a second current (I2) related to a second load current flowing via the second output terminal (6), first means (M1) for generating a first signal (S1) which is a measure of the first current (I1), second means (M2) for generating a second signal (S2) which is a measure of the second current (I2), and protection means (B) for limiting the first and the second load current in order to protect the first (A1) and the second (A2) amplifier, characterized in that the amplifier arrangement

further comprises third means (M3) for generating a first control signal (R1) which is a measure of the sum of the first (S1) and the second (S2) signal and which serves for controlling the protection means (B).

2. An amplifier arrangement as claimed in Claim 1, characterized in that the third means (M3) comprise a current mirror (T13, T14) having an input terminal (11, 12) for receiving the first and second signals (S1, S2) and an output terminal (15, 16) for supplying the first control signal (R1) the input terminal (11, 12) of the current mirror and the output terminal (15, 16) of the current mirror being coupled to one another by means of two series-coupled transistors (T15, T16) each having a control electrode, a first main electrode and a second main electrode, the two control electrodes being coupled to a reference voltage terminal (20) to receive a reference voltage, the two first main electrodes being coupled to the input terminal (11, 12) to receive both the first (S1) and the second (S2) signal, and the second main electrodes being coupled to the input terminal (11, 12) and the output terminal (15, 16) respectively.
3. An amplifier arrangement as claimed in Claim 1 or 2 characterized in that the first means (M1) comprise at least two transistors (T1, T2) each having a control electrode, a first main electrode and a second main electrode, the control electrodes being coupled both to one another and to one first main electrode, the first main electrodes each being coupled to a current source (T5, T6), and the second main electrodes being coupled to one another by means of a pair of series-coupled resistors (R11, R12), one second main electrode being coupled to an input terminal (7) to receive at least the first current (I1) and the other second main electrode being coupled to an output terminal (11) to supply the first signal (S1), and in that the second means (M2) comprise at least two transistors (T7, T8) each having a control electrode, a first main electrode and a second main electrode, the control electrodes being coupled both to each other and to one first main electrode, the first main electrodes each being coupled to a current source (T11, T12), and the second main electrodes being coupled to one another by means of a second pair of series-coupled resistors (R21, R22), one second main electrode being coupled to an input terminal (8) to receive at least the second current (I2) and the other second main electrode being coupled to an output terminal (12) to supply the second signal (S2).
4. An amplifier arrangement as claimed in Claim 1, 2, or 3, characterized in that the first amplifier

coupled to the terminal 10 and having its second main electrode coupled to the output terminal 6. The first means M1 comprise a circuit as shown in Fig. 2 but in which the second current mirror (T4, T5, T6) has been replaced by a current source J5 coupled to the second main electrode of the transistor T1 and by a current source J6 coupled to the second main electrode of the transistor T2. The transistor T27 is added again and the main electrodes of the transistors T1 and T2 are further coupled both the terminal 10 and the supply-voltage terminal Vdd by means of a set of resistors R41, R42 and R43. The second means M2 comprise a circuit as shown in Fig. 3, but in which the second current mirror (T10, T11, T12) has been replaced by a current source J11 coupled to the second main electrode of the transistor T7 and by a current source J12 coupled to the second main electrode of the transistor T8. The first main electrodes of the transistors T7 and T8 are further coupled to both the terminal 9 and the supply-voltage terminal Vss by a set of resistors R31, R32 and R33. The third means M3 comprise a circuit as shown in Fig. 4. The present embodiment provides a simple method of protecting a bridge amplifier arrangement, the operation of this embodiment not being different from that of the embodiments described with reference to the preceding Figures.

The first means M1 and the second means M2 can be constructed in a variety of ways, which also applies to the third means M3, which need not necessarily receive two signals of opposite polarity. However, in that case a threshold circuit is required, which may operate with a variable related threshold value.

Claims

1. An amplifier arrangement comprising a first amplifier (A1) having a first input terminal (1) and a first output terminal (5), the latter being for connection to a first terminal of a load and having at least a first transistor (PT1) for supplying a first current (i1) related to a first load current flowing via the first output terminal (5), a second amplifier (A2) having a second input terminal (2) and a second output terminal (6), the latter being for connection to a second terminal of the load and having at least a second transistor (PT2) for supplying a second current (i2) related to a second load current flowing via the second output terminal (6), first means (M1) for generating a first signal (S1) which is a measure of the first current (i1), second means (M2) for generating a second signal (S2) which is a measure of the second current (i2), and protection means (B) for limiting the first and the second load current in order to protect the first (A1) and the second (A2) amplifier, characterized in that the amplifier arrangement further comprises third means (M3) for generating a first control signal (R1) which is a measure of the sum of the first (S1) and the second (S2) signal and which serves for controlling the protection means (B).
2. An amplifier arrangement as claimed in Claim 1, characterized in that the third means (M3) comprise a current mirror (T13, T14) having an input terminal (11, 12) for receiving the first and second signals (S1, S2) and an output terminal (15, 16) for supplying the first control signal (R1) the input terminal (11, 12) of the current mirror and the output terminal (15, 16) of the current mirror being coupled to one another by means of two series-coupled transistors (T15, T16) each having a control electrode, a first main electrode and a second main electrode, the two control electrodes being coupled to a reference voltage terminal (20) to receive a reference voltage, the two first main electrodes being coupled to the input terminal (11, 12) to receive both the first (S1) and the second (S2) signal, and the second main electrodes being coupled to the input terminal (11, 12) and the output terminal (15, 16) respectively.
3. An amplifier arrangement as claimed in Claim 1 or 2 characterized in that the first means (M1) comprise at least two transistors (T1, T2) each having a control electrode, a first main electrode and a second main electrode, the control electrodes being coupled both to one another and to one first main electrode, the first main electrodes each being coupled to a current source (T5, T6), and the second main electrodes being coupled to one another by means of a pair of series-coupled resistors (R11, R12), one second main electrode being coupled to an input terminal (7) to receive at least the first current (i1) and the other second main electrode being coupled to an output terminal (11) to supply the first signal (S1), and in that the second means (M2) comprise at least two transistors (T7, T8) each having a control electrode, a first main electrode and a second main electrode, the control electrodes being coupled both to each other and to one first main electrode, the first main electrodes each being coupled to a current source (T11, T12), and the second main electrodes being coupled to one another by means of a second pair of series-coupled resistors (R21, R22), one second main electrode being coupled to an input terminal (8) to receive at least the second current (i2) and the other second main electrode being coupled to an output terminal (12) to supply the second signal (S2).
4. An amplifier arrangement as claimed in Claim 1, 2, or 3, characterized in that the first amplifier



(A1) further comprises at least a third transistor (PT3) for supplying a third current (i3) related to the first load current flowing via the first output terminal (5), the first means (M1) are adapted to generate also a third signal (S3) which is a measure of the third current (i3), the second amplifier (A2) further comprises at least a fourth transistor (PT4) for supplying a fourth current (i4) related to the second load current flowing via the second output terminal (6), the second means (M2) are adapted to generate also a fourth signal (S4) which is a measure of the fourth current (i4), and the third means (M3) are adapted to generate also a second control signal (R2) which is a measure of the sum of the third (S3) and the fourth (S4) signal and which serves to control the protection means (B).

5. An amplifier arrangement as claimed in Claim 4, characterized in that the third means (M3) comprise two substantially identical devices for generating the first (R1) and the second (R2) control signal respectively.

6. An amplifier arrangement as claimed in Claim 4 or 5, characterized in that the first means (M1) further comprise at least two transistors (T17, T18) each having a control electrode, a first main electrode and a second main electrode, the control electrodes being coupled both to each other and to one first main electrode, the first main electrodes each being coupled to a current source (T21, T22), and the second main electrodes being coupled to each other by means of a third pair of series-coupled resistors (R31, R32), one second main electrode being coupled to an input terminal (9) to receive the third current (i3) and the other second main electrode being coupled to an output terminal (13) to supply the third signal (S3), and in that the second means (M2) comprise at least two transistors each having a control electrode, a first main electrode and a second main electrode, the control electrodes being coupled both to one another and to one first main electrode, the first main electrodes each being coupled to a current source, and the second main electrodes being coupled to one another by means of a fourth pair of series-coupled resistors, one second main electrode being coupled to an input terminal to receive the fourth current (i4) and the other second main electrode being coupled to an output terminal to supply the fourth signal.

7. An amplifier arrangement as claimed in Claim 1, 2 or 3, characterized in that the first amplifier (A1) further comprises at least a third transistor (PT3) for supplying a third current (i3) related to the first

load current flowing via the first output terminal (5), and the second amplifier (A2) further comprises at least a fourth transistor (PT4) for supplying a fourth current (i4) related to the second load current flowing via the second output terminal (6), and in that the first signal (S1) is a measure of both the first (i1) and the fourth (i4) current and the second (S2) signal is a measure of both the second (i2) and the third (i3) current.

8. An amplifier arrangement as claimed in any one of the preceding Claims, characterized in that at least one of the means (M1) is further adapted to generate at least one further control signal (R3) which is a measure of one of the currents (i3) through the transistors and which serves for controlling the protection means.

Patentansprüche

1. Verstärkeranordnung mit einem ersten Verstärker (A1), der einen ersten Eingangsanschluß (1) und einen ersten Ausgangsanschluß (5) hat, wobei letzterer zur Verbindung mit einem ersten Anschluß einer Last dient, und mindestens einen ersten Transistor (PT1) zum Liefern eines ersten, mit einem über den ersten Ausgangsanschluß (5) fließenden ersten Laststrom zusammenhängenden Stroms (i1) hat, mit einem zweiten Verstärker (A2), der einen zweiten Eingangsanschluß (2) und einen zweiten Ausgangsanschluß (6) hat, wobei letzterer zur Verbindung mit einem zweiten Anschluß der Last dient, und mindestens einen zweiten Transistor (PT2) zum Liefern eines zweiten, mit einem über den zweiten Ausgangsanschluß (6) fließenden ersten Laststrom zusammenhängenden Stroms (i2) hat, erste Mittel (M1) zum Generieren eines ersten Signals (S1), das ein Maß für den ersten Strom (i1) ist, zweite Mittel (M2) zum Generieren eines zweiten Signals (S2), das ein Maß für den zweiten Strom (i2) ist, und Schutzmittel (B) zum Begrenzen des ersten und des zweiten Laststroms zum Schutz des ersten (A1) und des zweiten (A2) Verstärkers, dadurch gekennzeichnet, daß die Verstärkeranordnung weiterhin dritte Mittel (M3) zum Generieren eines ersten Steuersignals (R1) umfassen, das ein Maß für die Summe aus dem ersten (S1) und dem zweiten (S2) Signal ist und das zur Steuerung der Schutzmittel (B) dient.
2. Verstärkeranordnung nach Anspruch 1, dadurch gekennzeichnet, daß die dritten Mittel (M3) einen Stromspegel (T13, T14) mit einem Eingangsanschluß (11, 12) zum Empfangen des ersten und des zweiten Signals (S1, S2) und einen Ausgangsanschluß (15, 16) zum Liefern des ersten



- Steuersignals (R1) umfassen, wobei der Eingangsanschluß (11, 12) des Stromspiegels und der Ausgangsanschluß (15, 16) des Stromspiegels mittels zweier in Reihe geschalteter Transistoren (T15, T16) miteinander gekoppelt sind, von denen jeder eine Steuerelektrode, eine erste Hauptelektrode und eine zweite Hauptelektrode hat, wobei die beiden Steuerelektroden zum Empfangen einer Bezugsspannung mit einem Bezugsspannungsanschluß (20) gekoppelt sind, die beiden ersten Hauptelektroden zum Empfangen sowohl des ersten (S1) als auch des zweiten (S2) Signals mit dem Eingangsanschluß (11, 12) gekoppelt sind, und die zweiten Hauptelektroden mit dem Eingangsanschluß (11, 12) bzw. dem Ausgangsanschluß (15, 16) gekoppelt sind.
5. Verstärkeranordnung nach Anspruch 1 oder 2, dadurch gekennzeichnet, daß die ersten Mittel (M1) mindestens zwei Transistoren (T1, T2) umfassen, von denen jeder eine Steuerelektrode, eine erste Hauptelektrode und eine zweite Hauptelektrode hat, wobei die Steuerelektroden sowohl miteinander als auch mit der einen ersten Hauptelektrode gekoppelt sind, wobei die ersten Hauptelektroden jeweils mit einer Stromquelle (T5, T6) gekoppelt sind und die zweiten Hauptelektroden mittels eines Paares in Reihe geschalteter Widerstände (R11, R12) miteinander gekoppelt sind, wobei die eine zweite Hauptelektrode mit einem Eingangsanschluß (7) zum Empfangen mindestens des ersten Stroms (i1) und die andere zweite Hauptelektrode mit einem Ausgangsanschluß (11) zum Liefern des ersten Signals (S1) gekoppelt sind, und daß die zweiten Mittel (M2) mindestens zwei Transistoren (T7, T8) umfassen, von denen jeder eine Steuerelektrode, eine erste Hauptelektrode und eine zweite Hauptelektrode hat, wobei die Steuerelektroden sowohl miteinander als auch mit der einen ersten Hauptelektrode gekoppelt sind, wobei die ersten Hauptelektroden jeweils mit einer Stromquelle (T11, T12) gekoppelt sind und die zweiten Hauptelektroden mittels eines zweiten Paares in Reihe geschalteter Widerstände (R21, R22) miteinander gekoppelt sind, wobei die eine zweite Hauptelektrode mit einem Eingangsanschluß (8) zum Empfangen mindestens des zweiten Stroms (i2) und die andere zweite Hauptelektrode mit einem Ausgangsanschluß (12) zum Liefern des zweiten Signals (S2) gekoppelt ist.
4. Verstärkeranordnung nach Anspruch 1, 2, 3 oder 4, dadurch gekennzeichnet, daß der erste Verstärker (A1) weiterhin mindestens einen dritten Transistor (PT3) zum Liefern eines mit dem über den ersten Ausgangsanschluß (5) fließenden ersten Laststrom zusammenhängenden dritten Stroms (i3) umfaßt, die ersten Mittel (M1) zum Generieren auch eines dritten Signals (S3) eingerichtet sind, das ein Maß für den dritten Strom (i3) ist, der zweite Verstärker (A2) weiterhin mindestens einen vierten Transistor (PT4) zum Liefern eines mit dem über den zweiten Ausgangsanschluß (6) fließenden zweiten Laststrom zusammenhängenden vierten Stroms (i4) umfaßt, die zweiten Mittel (M2) zum Generieren auch eines vierten Signals (S4) eingerichtet sind, das ein Maß für den vierten Strom (i4) ist, und die dritten Mittel (M3) zum Generieren auch eines zweiten Steuersignals (R2) eingerichtet sind, das ein Maß für die Summe aus dem dritten (S3) und dem vierten Signal (S4) ist und zum Steuern der Schutzmittel (B) dient.
5. Verstärkeranordnung nach Anspruch 4, dadurch gekennzeichnet, daß die dritten Mittel (M3) zwei nahezu identische Einrichtungen zum Generieren des ersten (R1) bzw. des zweiten (R2) Steuersignals umfassen.
6. Verstärkeranordnung nach Anspruch 4 oder 5, dadurch gekennzeichnet, daß die ersten Mittel (M1) weiterhin mindestens zwei Transistoren (T17, T18) umfassen, von denen jeder eine Steuerelektrode, eine erste Hauptelektrode und eine zweite Hauptelektrode hat, wobei die Steuerelektroden sowohl miteinander als auch mit der einen ersten Hauptelektrode gekoppelt sind, wobei die ersten Hauptelektroden jeweils mit einer Stromquelle (T21, T22) gekoppelt sind und die zweiten Hauptelektroden mittels eines dritten Paares in Reihe geschalteter Widerstände (R31, R32) miteinander gekoppelt sind, wobei die eine zweite Hauptelektrode mit einem Eingangsanschluß (9) zum Empfangen des dritten Stroms (i3) und die andere zweite Hauptelektrode mit einem Ausgangsanschluß (13) zum Liefern des dritten Signals (S3) gekoppelt ist, und daß die zweiten Mittel (M2) mindestens zwei Transistoren umfassen, von denen jeder eine Steuerelektrode, eine erste Hauptelektrode und eine zweite Hauptelektrode hat, wobei die Steuerelektroden sowohl miteinander als auch mit der einen ersten Hauptelektrode gekoppelt sind, wobei die ersten Hauptelektroden jeweils mit einer Stromquelle gekoppelt sind und die zweiten Hauptelektroden mittels eines vierten Paares in Reihe geschalteter Widerstände miteinander gekoppelt sind, wobei die eine zweite Hauptelektrode mit einem Eingangsanschluß zum Empfangen des vierten Stroms (i4) und die andere zweite Hauptelektrode mit einem Ausgangsanschluß zum Liefern des vierten Signals gekoppelt ist.
7. Verstärkeranordnung nach Anspruch 1, 2 oder 3,



dadurch gekennzeichnet, daß der erste Verstärker (A1) weiterhin mindestens einen dritten Transistor (PT3) zum Liefern eines mit dem über den ersten Ausgangsanschluß (5) fließenden ersten Laststrom zusammenhängenden dritten Stroms (i3) umfaßt und der zweite Verstärker (A2) weiterhin mindestens einen vierten Transistor (PT4) zum Liefern eines mit dem über den zweiten Ausgangsanschluß (6) fließenden zweiten Laststrom zusammenhängenden vierten Stroms (i4) umfaßt, und daß das erste Signal (S1) ein Maß für sowohl den ersten (i1) als auch den vierten Strom (i4) ist und das zweite Signal (S2) ein Maß für sowohl den zweiten (i2) als auch den dritten (i3) Strom ist.

8. Verstärkeranordnung nach einem der vorhergehenden Ansprüche, dadurch gekennzeichnet, daß mindestens eines der Mittel (M1) weiterhin eingerichtet ist, mindestens ein weiteres Steuersignal (R3) zu generieren, das ein Maß für einen der durch die Transistoren fließenden Ströme (i3) ist und das zur Steuerung der Schutzmittel dient.

Revendications

1. Circuit d'amplification comportant un premier amplificateur (A1) présentant une première borne d'entrée (1) et une première borne de sortie (5), la borne mentionnée en dernière instance étant conçue pour être reliée à une première borne d'une charge et présentant au moins un premier transistor (PT1) pour fournir un premier courant (i1) relatif à un premier courant de charge se propageant par l'intermédiaire de la première borne de sortie (5), un deuxième amplificateur (A2) présentant une deuxième borne d'entrée (2) et une deuxième borne de sortie (6), la borne mentionnée en dernière instance étant conçue pour être reliée à une deuxième borne de la charge et présentant au moins un deuxième transistor (PT2) pour fournir un deuxième courant (i2) relatif à un deuxième courant de charge se propageant par l'intermédiaire de la deuxième borne de sortie (6), de premiers moyens (M1) pour engendrer un premier signal (S1) qui est une mesure du premier courant (i1), de deuxièmes moyens (M2) pour engendrer un deuxième signal (S2) qui est une mesure du deuxième courant (i2), et des moyens de protection (B) pour limiter les premier et deuxième courants de charge afin de protéger les premier (A1) et deuxième (A2) amplificateurs, caractérisé en ce que le circuit d'amplification comporte encore de troisièmes moyens (M3) pour engendrer un premier signal de commande (R1) qui est une mesure de la somme des premier (S1) et deuxième (S2) signaux et qui sert à

commander les moyens de protection (B).

2. Circuit d'amplification selon la revendication 1, caractérisé en ce que les troisièmes moyens (M3) comportent un miroir de courant (T13, T14) présentant une borne d'entrée (11, 12) pour recevoir les premier (S1) et deuxième (S2) signaux et une borne de sortie (15, 16) pour fournir le premier signal de commande (R1), la borne d'entrée (11, 12) du miroir de courant et la borne de sortie (15, 16) du miroir de courant étant couplées l'une à l'autre au moyen de deux transistors (T15, T16) montés en série et présentant chacun une électrode de commande, savoir une première électrode de principale et une deuxième électrode principale, les deux électrodes de commande étant couplées à une borne de tension de référence (20) pour recevoir une tension de référence, les deux premières électrodes principales étant couplées à la borne d'entrée (11, 12) pour recevoir le premier signal (S1) aussi bien que le deuxième signal (S2), et les deuxièmes électrodes principales étant couplées à la borne d'entrée (11, 12) respectivement à la borne de sortie (15, 16).

3. Circuit d'amplification selon la revendication 1 ou 2, caractérisé en ce que les premiers moyens (M1) comportent au moins deux transistors (T1, T2) ayant chacun une électrode de commande, savoir une première électrode principale et une deuxième électrode principale, les électrodes de commande étant couplées l'une à l'autre aussi bien qu'à une première électrode principale, les premières électrodes principales étant couplées chacune à une source de courant (T5, T6), et les deuxièmes électrodes principales étant couplées l'une à l'autre au moyen d'une paire de résistances (R11, R12) montées en série, une deuxième électrode principale étant couplée à une borne d'entrée (7) pour recevoir au moins le premier courant (i1) et l'autre deuxième électrode principale étant couplée à une borne de sortie (11) pour fournir le premier signal (S1), et en ce que les deuxièmes moyens (M2) comportent au moins deux transistors (T7, T8) ayant chacun une électrode de commande, savoir une première électrode de principale et une deuxième électrode principale, les électrodes de commande étant couplées l'une à l'autre aussi bien qu'à une première électrode principale, les premières électrodes principales étant couplées à une source de courant (T11, T12) et les deuxièmes électrodes principales étant couplées l'une à l'autre au moyen d'une deuxième paire de résistances (R21, R22) montées en série, une deuxième électrode principale étant couplée à une borne d'entrée (18) pour recevoir au moins le deuxième courant (i2) et l'autre deuxième électrode principale étant couplée à



une borne de sortie (12) pour fournir le deuxième signal (S2).

4. Circuit d'amplification selon la revendication 1, 2 ou 3, caractérisé en ce que le premier amplificateur (A1) comporte encore au moins un troisième transistor (PT3) pour fournir un troisième courant (i3) relatif au premier courant de charge se propageant par l'intermédiaire de la première borne de sortie (5), les premiers moyens (M1) sont adaptés de manière à engendrer également un troisième signal (S3) qui est une mesure du troisième courant (i3), le deuxième amplificateur (A2) comporte au moins un quatrième transistor (PT4) pour fournir un quatrième courant (i4) relatif au deuxième courant de charge se propageant par l'intermédiaire de la deuxième borne de sortie (6), les deuxièmes moyens (M2) sont conçus de manière à engendrer également un quatrième signal (S4) qui est une mesure du quatrième courant (i4), et les troisièmes moyens (M3) sont conçus de manière à engendrer également un deuxième signal de commande (R2) qui est une mesure de la somme des troisième (S3) et quatrième (S4) signaux et qui sert à commander les moyens de protection (B). 10
5. Circuit d'amplification selon la revendication 4, caractérisé en ce que les troisièmes moyens (M3) comportent deux dispositifs sensiblement identiques pour engendrer le premier (R1) respectivement le deuxième (R2) signal de commande. 15
6. Circuit d'amplification selon la revendication 4 ou 5, caractérisé en ce que les premiers moyens (M1) comportent au moins deux transistors (T17, T18) ayant chacun une électrode de commande, savoir une première électrode principale et une deuxième électrode principale, les électrodes de commande étant couplées l'une à l'autre aussi bien qu'à une première électrode principale, les premières électrodes principales étant couplées chacune à une source de courant (T21, T22), et les deuxièmes électrodes principales étant couplées l'une à l'autre au moyen d'une troisième paire de résistances (R31, R32) montées en série, une deuxième électrode principale étant couplée à une borne d'entrée (9) pour recevoir le troisième courant (i3) et l'autre deuxième électrode principale étant couplée à une borne de sortie (13) pour fournir le troisième signal (S3), et en ce que les deuxièmes moyens (M2) comportent au moins deux transistors ayant chacun une électrode de commande, savoir une première électrode principale et une deuxième électrode principale, les électrodes de commande étant couplées l'une à l'autre aussi bien qu'à une première élec- 20 25 30 35 40 45 50 55

trode principale, les premières électrodes principales étant couplées chacune à une source de courant, et les deuxièmes électrodes principales étant couplées l'une à l'autre au moyen d'une quatrième paire de résistances montées en série, une deuxième électrode principale étant couplée à une borne d'entrée pour recevoir le quatrième courant (i4) et l'autre deuxième électrode principale étant couplée à une borne de sortie pour fournir le quatrième signal.

7. Circuit d'amplification selon la revendication 1, 2 ou 3, caractérisé en ce que le premier amplificateur (A1) comporte encore au moins un troisième transistor (PT3) pour fournir un troisième courant (i3) relatif au premier courant de charge se propageant par l'intermédiaire de la première borne de sortie (5), et que le deuxième amplificateur (A2) comporte encore au moins un quatrième transistor (PT4) pour fournir un quatrième courant (i4) relatif au deuxième courant de charge se propageant par l'intermédiaire de la deuxième borne de sortie (6), et en ce que le premier signal (S1) est une mesure du premier (i1) aussi bien que du quatrième courant (i4) et que le deuxième signal (S2) est une mesure du deuxième (i2) aussi bien que du troisième (i3) courant. 15 20 25
8. Circuit d'amplification selon l'une quelconque des revendications précédentes, caractérisé en ce qu'au moins l'un des moyens (M1) est encore adapté à engendrer au moins encore un autre signal de commande (R3) qui est une mesure de l'un des courants (i3) traversant les transistors et qui sert à commander les moyens de protection. 30 35 40 45 50 55

