

KEY SCAN CIRCUIT AND METHOD OF OPERATING THE SAME

The present invention relates to a key scan circuit and to a method of operating a key scan circuit. The method and circuit are adapted for use in a microcomputer system utilizing a bilateral port.

In a conventional key scan circuit as disclosed in the applicant's Korean Patent Publication No. 89-2297, signals sensed in a key matrix circuit are fed to data input ports D0-D2 of a microprocessor 1 through a multiplexer 4 as shown in Fig. 1. In Fig. 1, output ports P0, P1, P2 and P3 of microprocessor 1 are respectively coupled to input terminals a, b, c and d of demultiplexer 2. Falling pulses from output terminals O-F of demultiplexer 2 are sequentially supplied to each row scan line Y0-Y15 of matrix circuit 3. Thereafter, data from column scan lines X0-X7 of the matrix circuit 3 is inputted to input terminals 0-7 of multiplexer 4. The outputs Q0-Q2 of multiplexer 4 are input to the data input ports D0-D2 of microprocessor 1. Accordingly, the conventional key scan circuit checks keys by directly driving ports, requiring additional circuitry such as a demultiplexer and a data buffer, and further requires an additional circuit including diodes to guard against short circuits at the ports, in case two or more keys are pressed simultaneously.

Therefore it is an object of the present invention to provide a key scan circuit and method therefor allowing simplified key processing.

According to a first aspect of the invention there is provided a keypad scanning circuit for a microcomputer system consisting of a keypad having an $m \times n$ key matrix circuit and a microcomputer for recognising keying operation from the keypad, the keypad scanning circuit comprising:

a first port for receiving m row signals from said keypad via row scan lines;

a first memory selectable to store the logic value of the m row signals input to said first port logically multiplied by the currently stored logic value;

a second port for supplying n column signals to said keypad via column scan lines;

a data direction-register for setting each bit of said second port as an input or an output; and

a second memory selectable to store the logic value currently stored in said second memory logically summed to the logic value in said data direction register.

According to a further aspect of the invention there is provided a method of operating a scanning circuit including a matrix keypad, first and second

ports connected to respective row and column scan lines of said keypad, first and second memories and a data direction register for setting each bit of said second port to be used as an input or an output, said method comprising the steps of:

- i) initialising the system by setting predetermined logic values in said first and second memories and said data direction register;
- ii) sequentially scanning each column scan line of the matrix keypad in accordance with successive logic values stored in the data direction register;
- iii) upon detecting that a key in a scanned column scan line has been depressed, storing into said first memory the logical product of the current logic value stored in said first memory and the current logic value stored in said first port, and storing into said second memory the logical sum of the current logic value stored in said second memory and the current logic value stored in the data direction register;
- iv) error checking to check that multiple keys have not been depressed; and
- v) if no error is detected, determining the value of the key depressed.

The above objects and advantages of the invention will become more apparent from the following description of a preferred embodiment of the present

invention with reference to the attached drawings in which:

Fig. 1 is a schematic circuit diagram of a conventional key scan circuit;

5 Fig. 2 is a schematic circuit diagram showing a preferred embodiment of a key scan circuit according to the present invention;

Fig. 3 is a flow chart illustrating the method of operation of the key scan circuit shown in Fig. 2;

10 Fig. 4 illustrates a rotation shift left (RSL) operation of the data direction register shown in Fig. 2; and

Figs. 5A and 5B are schematic circuit diagrams showing two further embodiments of the bilateral port used in the key scan circuit of the microcomputer system according to the present invention.

A description of a preferred embodiment of the present invention follows with reference to the attached drawings.

20 Referring to Fig. 2, there is shown a key scan circuit of a microcomputer system including a keypad 20 having an $m \times n$ key matrix circuit connected directly to microcomputer 10 via row scan lines 50 and column scan lines 40, without additional circuitry
25 such as demultiplexers of the conventional circuits. A preferred embodiment of the present invention will

be explained in which keypad 20 has a key matrix circuit composed of a 4 x 4 key matrix; that is 16 keys from 0 through F. A microcomputer 10 comprises a first port PA having 4 bits b0, b1, b2 and b3 for receiving a 4-bit row signal via row scan lines when any key is pressed on keypad 20; a first memory MA for storing the logic value of the 4-bit row signal input to the first port PA logically multiplied by the previously stored logic value therein; a second port PB having 4 bits b0, b1, b2, b3 for outputting a 4-bit column signal from the keypad 20 via column scan lines; a data direction register DDR for setting each bit of the second port PB to an input or output mode; a second memory MB for storing the logic value of the 4-bit column signal input to the second port PB logically summed with the logic value of each bit of a data direction register DDR. Pull-up resistor portion 30 for supplying a reference logic value to keypad 20 are coupled to the keypad 20 and an AND gate 60. The AND gate 60 provides a logical product of the signals output from keypad 20, to be used as a control signal for performing an automatic on/off function of the microcomputer system or for supplying a key check signal.

The operation of the above key scan circuit according to the present invention will be described

below in detail with reference to Fig. 3 which is a flowchart illustrating the method of operation of a microcomputer system according to the present invention.

5 Referring to Fig. 3, the microcomputer system initializes certain parameters in order to check whether a key of keypad 20 has been pressed. This is accomplished in step S601 by setting the first port PA to an input-only mode and establishing the values of
10 the respective bits in the second port PB, the first and second memories MA and MB, and the data direction register DDR, as '0000', '1111', '0000' and '1111', respectively. Here, each bit of the bilateral port PB is in an output mode when the value of the
15 corresponding bit of the data direction register DDR is '1', and each bit of the bilateral port PB is in an input mode when the value of the corresponding bit of the data direction register DDR is '0'.

 Step S602 represents a user function. If the
20 user presses one or more keys in step S602, the program advances to step S603 in order to check which key is pressed. In step S603, the data direction register DDR is set to '0001' to begin checking the
25 keys from the first column. This particular operation means that b3, b2 and b1 of the second port PB are in the input mode, and b0 is in the output mode. If any

keys in that column have been pressed, they are found in step S604, where the first port PA is checked against the value "1111" which corresponds to the pull-up resistors 30. If PA matches "1111", it is
5 determined that as none of the input port bits are pulled low, no pressed key exists in that column. Then, the program proceeds to step S606, where data direction register DDR clears a carry bit value C and performs a rotate shift left (RSL) function in order
10 to check the next column as shown in Fig. 4.

Meanwhile, if in step S604 PA is shown to be other than "1111", it is determined that at least one key has been pressed in step S602, and processing advances to step S605 where the microprocessor
15 carries out two logic functions: first, the current value of first memory MA is multiplied by the logic value of the first port PA, then restored into MA, and secondly, the current value of second memory MB is summed with the logic value of data direction register
20 DDR, then restored into MB. After step S605, the carry bit is cleared and an RSL function is done by the data direction register DDR in step S606.

In step S607 it is checked whether carry bit C equals one. This occurs when the data direction
25 register DDR, set to "0001" in step S603, has completed 4 RSL functions and all columns have been

scanned. Steps S604, S605, and S606 are repeated until C=1.

After key-scanning, it is determined in steps S608 and S609 how many, if any, keys are pressed. If C=1 in step S607, it is determined whether second memory MB is still set to "0000" in step S608. If MB = 0000 in step S608, processing is complete with no pressed keys being detected. However, if MB $\neq$ 0000 in step S608, processing moves to step S609 to determine if there has been a double-key error. If more than one logic "0's" appear in first memory MA, or if more than one logic "1's" are present in second memory MB, it is judged in step S609 that multiple keys have been pushed, and then processing advances to step S610 and an error process is performed and processing is completed.

In the meantime, if there is only one "0" in MA and one "1" in MB in step S609, the key's value is determined in step 611 with the formula: $4m+n=MV$, which allows the key's value to be entered in step 612 and the procedure terminates. Here, MV denotes the key's value, m corresponds to a value of m when the mth bit of first memory MA is a logic "0", and n corresponds to a value of n when the nth bit second memory MB is a logic "1".

For example, if the 9th key of the keypad's

matrix is pushed in step S602, "1011" is supplied to the first port PA. In doing so, the value "1111" (the initial value of MA set in step S601) is logically multiplied by the value "1011" (the currently held input value of PA), and the product "1011" is stored in the first memory MA. The value in second memory MB is calculated by logically summing the value "0000" (the initial value of MB set in step S601) with the value "0010" (the current state of DDR), and the result "0010" is stored in the second memory MB. Thus as m is 2 (b2) and n is 1 (b1), MV is calculated to be 9, or the 9th key in the matrix.

To add more, the logic values of row and column signals which are values of the row-column signal of the key are stored in each bit of the first and second memories MA and MB by scanning keys during steps S603 to S607. The reason for setting the value of the data direction register DDR to "0001" in step S603 is to scan the keypad 20 from the first column, thereby preventing short circuits by designating bits b3, b2 and b1 of the bilateral second port PB to be in an input mode in case multiple keys are pushed at the same time. In step S606, it is checked whether or not a key of each column has been pushed, and in step S605, a signal indicating the location of a pushed key is stored in each of memories MA and MB. In step

S606, the value of the data direction register DDR is shifted to check the next column, and in step S607, it is checked whether or not a carry bit has been generated to determine whether or not the scan is complete. In step S608, it is checked whether no key has been pushed if the value of the second memory MB is unchanged, and step S609 determines whether or not more than one key has been pushed if the bit values of the first and second memories MA and MB have changed.

5 As this time, if more than one key has been pushed, it is determined that a "double key" error has occurred in step S610, and if only one key is pushed, it is determined which key has been pressed in step 611.

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Which key has been pushed is determined based on the bit values stored in the first and second memories MA and MB. In the example of Fig. 2, the bit value varies according to the sequence 0→4→8→C. This is a simplified structure, showing the bit value changing in multiples of 4. If the bit b0 of the first memory MA changes when the bit b0 column of the second port PB is scanned, the key value is defined as "0" according to the formula $MV = 4m + n$. If bit b1 of the first memory MA changes at the same bit column as above, the key value is defined as "4". According to

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the same method, if the bit b2 of MA and the bit b1 of MB change, it is indicated by $4 + 2 + 1 = 9$ as $m + 2$

and $n = 1$ are substituted in the formula, that is, the 9th key is pushed,

Two additional embodiments of the key scan circuit of a microcomputer system according to the present invention are shown in Figs. 5A and 5B. The
5 embodiments use open-collector and open-drain transistors, respectively, positioned along the column scan lines, instead of using a bilateral port such as the second port PB in the microcomputer shown in
10 Figure 2, thereby obtaining the same effect as a bilateral port.

The operation of the embodiments is such that if a "high" is fed to the input port of an inverter, the collector of the transistor is open, and if a "low" is
15 input, the collector of the transistor goes low to properly set the value in the data direction register, just as in the bilateral port, thereby preventing
- circuit shorts.

Further, as shown in Fig. 2, by adding an AND
20 gate 60 to the output of the key scan circuit in each embodiment of the present invention, a logical product of the logic signals applied to each port may be used as a control signal for automatically turning on the system whenever a key is pushed, or for a key
25 processing function.

As described above in detail, the key scan

circuit and the method thereof of the microcomputer system properly sets the logic value of the data direction register having a bilateral port or an open collector transistor, thereby preventing circuit shorts caused when multiple keys are pushed, and eliminating excess circuitry.

There is thus provided a relatively simple key scan circuit which does not require diodes for preventing short circuits during a key scan operation.

The circuit provides simple means for turning on the circuit as well as key checking means.

**CLAIMS:**

1. A keypad scanning circuit for a microcomputer system consisting of a keypad having an $m \times n$ key matrix circuit and a microcomputer for recognising keying operation from the keypad, the keypad scanning circuit comprising:

a first port for receiving m row signals from said keypad via row scan lines;

a first memory selectable to store the logic value of the m row signals input to said first port logically multiplied by the currently stored logic value;

a second port for supplying n column signals to said keypad via column scan lines;

a data direction register for setting each bit of said second port as an input or an output; and

a second memory selectable to store the logic value currently stored in said second memory logically summed to the logic value in said data direction register.

2. A keypad scanning circuit as claimed in claim 1 wherein the first memory is selected to store the logic value stored in the first port multiplied by the logic value currently stored in the first memory and the second memory is selected to store the sum of the



logic value stored in the data direction register and the logic value currently stored in the second memory upon detecting that a key in a scanned column scan line has been depressed.

5 3. A keypad scanning circuit for a microcomputer system as claimed in claim 1 or claim 2, wherein each row has a key value corresponding to the row number multiplied by the number of columns.

10 4. A keypad scanning circuit for a microcomputer system as claimed in any one of the preceding claims, wherein said $m \times n$ key matrix circuit is a 4×4 key matrix circuit.

15 5. A keypad scanning circuit for a microcomputer system as claimed in any one of the preceding claims, further comprising an AND gate having its inputs connected to the row scan lines.

20 6. A keypad scanning circuit as claimed in claim 5, wherein the output of the AND gate is supplied to the scanning circuit to provide a key check signal and/or an on/off function signal.

7. A keypad scanning circuit for a microcomputer



system as claimed in any one of the preceding claims, wherein said second port is formed of open-collector type bipolar transistors.

5 8. A keypad scanning circuit for a microcomputer system as claimed in any one of claims 1 to 6, wherein said second port is formed of open-drain type MOS transistors.

10 9. A keypad scanning circuit as claimed in any one of the preceding claims including means for determining the key value based on the values stored in said first and second memories.

15 10. A keypad scanning circuit for a microcomputer system as claimed in any one of the preceding claims including pull-up resistors connected between said row scan lines and a reference voltage.

20 11. A method of operating a scanning circuit including a matrix keypad, first and second ports connected to respective row and column scan lines of said keypad, first and second memories and a data direction register for setting each bit of said second port to be used as an input or an output, said method comprising the steps of:



- i) initialising the system by setting predetermined logic values in said first and second memories and said data direction register;
- ii) sequentially scanning each column scan line of the matrix keypad in accordance with successive logic values stored in the data direction register;
- iii) upon detecting that a key in a scanned column scan line has been depressed, storing into said first memory the logical product of the current logic value stored in said first memory and the current logic value stored in said first port, and storing into said second memory the logical sum of the current logic value stored in said second memory and the current logic value stored in the data direction register;
- iv) error checking to check that multiple keys have not been depressed; and
- v) if no error is detected, determining the value of the key depressed.

12. A method as claimed in claim 11 wherein the logic value initially stored in the data direction register is sequentially shifted until all column scan lines have been scanned.

13. A method as claimed in claim 12 wherein scanning continues until the carry bit of the data direction



register is "1".

14. A method as claimed in claim any one of claims 11 to 13 wherein error checking comprises checking whether the number of logic 0's in said first memory is greater than 1 or whether the number of logic 1's in said second memory is greater than 1.

15. A method as claimed in any one of claims 11 to 14 wherein the initialisation process includes the step of designating said first port as an input only port.

16. A method as claimed in any one of claims 11 to 15 wherein the key value is determined using the logic values stored in the first and second memories.

17. A method as claimed in any one of claims 11 to 16 wherein key value MV is determined in accordance with the formula $MV = 4R + C$, where R is the row number and C is the column number.

18. A method as claimed in any one of claims 11 to 17 wherein the predetermined logic value stored in said first memory is "1111", the predetermined logic value stored in said second memory is "0000" and the predetermined logic value stored in said data



direction register is "0001".

19. A key scan method in a microcomputer including a keypad having an $m \times n$ key matrix circuit, first and second ports for processing $m \times n$ row and column signals, a first memory and a second memory for storing the logic values corresponding to said first and second ports, and a data direction register for setting each bit of said second port so as to be as an input or an output, said method comprising the steps of:

initialising said microcomputer system by presetting said second port, first and second memories, and data direction register with predetermined logic values;

scanning each bit of said data direction register when a key of said matrix keypad is pushed;

deciding whether or not the current input value of said first port matches said predetermined logic value stored in the first memory, and, if the current value matches the logic value, performing a shift function to the bit values of said data direction register or, if the current value does not match the logic value, storing in said first memory, the logic product of the current logic value of the first memory and the current logic value of said first port,



storing in said second memory, the logical sum of the current logic value of the second memory and the current logic value of said data direction register, and then performing a shift function to the bit values of said data direction register, and sequentially repeating said processes until the carry bit of said data direction register becomes "1"; and

determining whether or not the current logic value of the second memory matches said predetermined logic value set in the initial step when the carry bit becomes "1", and if matched, completing the operation, and if not, determining whether or not the number of current logic "0's" stored in said first memory is greater than one, or whether or not the number of current logic "1's" stored in said second memory is greater than one, thereby checking if more than one key has been pushed, completing the operation by error processing if one or both statements are true, and if both statements are false, determining the key's value according to a predetermined formula.

20. A method as claimed in claim 19, wherein the key value is determined on the basis of the values stored in the first and second memories.

21. A method substantially as hereinbefore described



with reference to Figures 2 to 4 or 3 to 5A or 3, 4 and 5B of the accompanying drawings.

22. A keypad scanning circuit substantially as
hereinbefore described with reference to Figures 2 to
5 4 or 3 to 5A or 3, 4 and 5B of the accompanying
drawings.
