

"DIGITAL WORD SYNCHRONIZING ARRANGEMENTS"

Our invention relates to a digital word synchronizing arrangement. In particular, our invention relates to an arrangement or a method for achieving synchronization with digital synchronizing words provided at selected intervals in a digital message.

Sequences of digital signals are frequently used to transmit data, because such sequences can be transmitted rapidly and efficiently. However, such rapid transmission requires equally rapid and efficient synchronization of the data receiver with the words forming the information of the transmitted data message. Without such synchronization, the beginning and end of each information word is unknown, resulting in meaningless data. The synchronization problem is increased if the transmission medium is noisy or subject to fading, as it frequently is if the medium is a radio channel. For these and other reasons, predetermined synchronizing words are provided sequentially at spaced locations or times in a data message to provide a data receiver with the opportunity to recognize the synchronizing words and synchronize itself so as to accurately detect where the

information parts or words of the data message begin and end.

Briefly, in the present specification there is described an improved synchronising arrangement
5 in which we compare the received digital signals in a message with a stored predetermined digital synchronising word. Upon the initial correct comparison indicating a correctly received synchronising word, we compare the next four subsequently
10 received synchronising words with the stored predetermined synchronising word. If any two of these four subsequent comparisons indicates a correctly received synchronising word, we produce an in-synchronisation signal to indicate that word
15 synchronisation has been achieved, and to indicate that information words can then be accurately read and utilised. However, if less than two of these four subsequent comparisons indicate a correctly received synchronising word, we resume comparison
20 of the subsequent digital signals until another initial correct synchronising word is indicated. We then compare the next four synchronising words, and if any two are correct, we produce an in-synchronisation signal. If less than two are
25 correct, we start again. This process is repeated as often as needed or until no more synchronising words are received.

In the accompanying drawings, by way of example only:-

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FIGURE 1 is a diagram illustrating a digital message for which a synchronizing arrangement embodying the invention can be used;

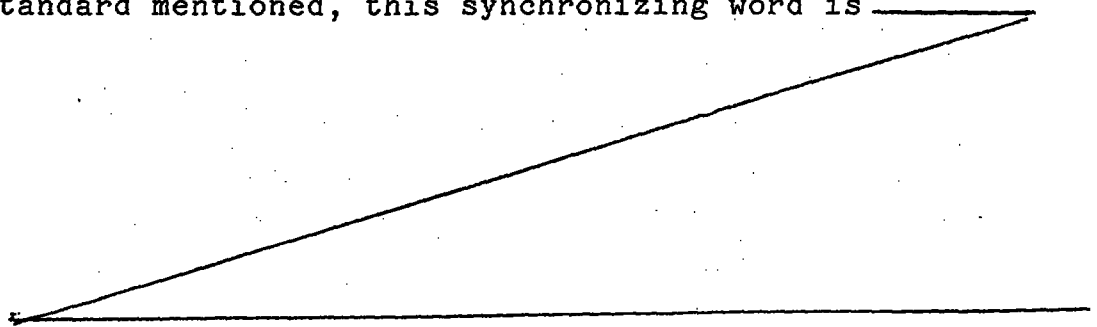
FIGURE 2 is a block diagram illustrating the synchronizing arrangement; and

FIGURE 3 is a flow chart or diagram illustrating the operation of the synchronizing arrangement of FIGURE 2.

While persons of ordinary skill in the art will, after reading this description, appreciate that our preferred synchronizing arrangement can be used with various formats of data messages having various synchronizing words, we have selected the sequential data format of FIGURE 1 to explain the operation of our arrangement. This data format is intended to be used to transmit a data message in cellular radio telephone systems. And while we describe our preferred arrangement with binary types of data, persons skilled in the art will appreciate that it can be used with other types of data, such as ternary signals. The data format comprises a total of 1032 bits, and the bit number that starts each part of the format is indicated. The format of FIGURE 1 starts with 101 dotting bits, which typically are alternate 1's and 0's to achieve bit synchronization. Next, starting with bit 102, the first synchronizing word of 11 bits is transmitted. In the cellular data message standard mentioned, this synchronizing word is

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comprised as follows: 11100010010. While other synchronizing words can be used, the indicated format is desirable in that it has a relatively small chance of being repeated in a message word. Following the first synchronizing word, a first message word of 40 bits starting with bit 113 is transmitted. These bits have binary values that convey the desired message. Next, starting with bit 153, 37 dotting bits are transmitted. These are followed by the second synchronizing word which is identical to the first synchronizing word. The second synchronizing word is followed by a second message word, which typically is the same as the first message word. This sequence is repeated to provide a total of 11 sequences comprised of dotting bits, a synchronizing word, and a message word. And, the synchronizing words are typically equally spaced by 77 bits: 40 bits of a message word plus 37 synchronizing bits. However, such equal spacing or time interval is not essential.

One of the reasons that this format was selected was that it typically enables a radio receiver to achieve bit synchronization and word synchronization in a relatively short time and with reasonable accuracy. This accuracy is improved if a word synchronizing arrangement in accordance with our invention is utilized.

FIGURE 2 shows a block diagram that illustrates our synchronizing arrangement. While a typical preferred embodiment of our invention would more likely be achieved by means of a microprocessor and associated

memory circuits, we have provided the block diagram of FIGURE 2 in order to facilitate the understanding of our arrangement.

5 As shown, our arrangement includes a receiver 10 which receives and processes incoming signals from either a wire or radio medium, and if necessary, demodulates these signals. If these signals include speech or other information, they can be applied to appropriate circuits. The data signals are applied to a signal
10 conditioner 11 which, if the data is in the form of modulated signals, converts these signals to digital signals having the appropriate or desired voltage levels. These digital signals are applied to a bit
15 synchronization circuit 12 which, as known in the art, produces a clock signal of the appropriate frequency that is synchronized with the incoming bit signals. The clock signal is applied to various portions of our arrangement as needed. The bit signals are applied to a
20 synchronizing word comparator or comparison circuit 13 which compares the incoming bit signals with a stored synchronizing word having the desired or predetermined bit sequence in a storage circuit 14. This comparison may be either in series or in parallel. Each time a
25 correct sequence of synchronizing word bits (such as the 11100010010 mentioned) is found from this comparison, the comparator 13 produces an output signal that is applied to a good synchronizing word counter 15. When
30 reset, the comparator 13 operates in a bit by bit mode to look at each new bit to determine if that new bit plus the prior (ten) bits form the correct synchronizing

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word. After an initial detection of a correct synchronizing word, the comparator 13 operates in a position mode and only looks at the 11 (or appropriate number of) bits which occur at the time or position of the next synchronizing word.

5 The counter 15 has appropriate outputs that respectively indicate a count of 1 good word, or a count of 2 good words, or a count of 3 or more good words as shown. Each time a count of 1, or a count of 2, or a count of 3 is reached, an enable signal is applied to a synchronizing word position indicator 16. If the count of counter 15 is less than 1, the indicator 16 is disabled.

10 The position indicator 16 is arranged to count clock bits from the circuit 12 so that when the indicator 16 is enabled by the initial detection of a synchronizing word, it can count the number of bits to indicate the time position or location of the next expected synchronizing word. After being enabled by an initial detection of a synchronizing word, the indicator 16 produces an output 1, 2, 3 or 4 respectively for the time or position in which succeeding synchronizing words 1, 2, 3 or 4 should appear. Thus, with reference to FIGURE 1 again, if the first synchronizing word (bits 102 through 112) is correctly detected, the position indicator 16 can then count the number of bits to indicate the position of the second synchronizing word. This count would be the first message word of 40 bits plus the next 37 dotting bits, so that at the appearance of bit 190 of the second synchronizing word, the indicator 16 provides an output signal at output 1 to

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indicate that the first synchronizing word, after a detection of the initial synchronizing word, is in position. An output signal is provided at outputs 2, 3 and 4 to indicate the time or position of the second, third and fourth synchronizing words respectively after the initial detection of a synchronizing word. Of course, the initial detection may occur at any location in the message shown in FIGURE 1. Each of the outputs 1, 2, 3 and 4 are applied to the synchronizing word comparator 13 to cause the comparator 13 to operate in the position mode and look for a synchronizing word at the proper time or position.

When the word position indicator 16 produces an output 4, this indicates that four synchronizing word positions have occurred since the initial correctly detected synchronizing word. This 4 output is applied to an enable input of an in-synchronization output gate 18.

This 4 output from the indicator 16 is applied to open or enable an in-synchronization output gate 18. If the good word counter 15 has reached a count of 3 or more, its 3 output is passed by the enabled gate 18 to indicate that word synchronization has been achieved by detection of a first correct synchronizing word, and by detection of two additional synchronizing words during the next four synchronizing word positions. When passed by the gate 18, this in-synchronization signal can be utilized by a decode circuit 21 to indicate to the receiver 10 or other circuits that word synchronization has been achieved, and hence the message words of FIGURE

1 can be accurately and correctly decoded or utilized.

The position indicator 16 is also provided with an output to indicate the end of the position of synchronizing word 4. This output is applied to reset the word comparator 13 for bit by bit comparison, and to reset the word counter 15 and the position indicator 16 to zero. Upon this reset, the arrangement starts looking for an initial synchronizing word again, whether an in-synchronization output was produced or was not produced.

FIGURE 3 shows a flow chart or diagram illustrating the operation of the arrangement of FIGURE 2, and also illustrating the operation that would be performed by a microprocessor and appropriate memory circuits to achieve the same function as that provided by the arrangement of FIGURE 2. With respect to FIGURE 3, a start function is initiated by a start circuit 30 to clear or reset the various circuits as indicated by the block 31. This permits the sequential digital bits to be shifted into the word comparator as indicated by the block 32.

Bits continue to be shifted into the word comparator as long as no initial synchronizing (sync in FIGURE 3) word is detected as indicated by the decision block 33. However, once an initial synchronizing word is detected, the circuit waits for additional synchronizing and message words as indicated by the block 34. Each time a subsequent synchronizing word position occurs, the decision block 35 determines whether a correct synchronizing word is present or detected. If the

determination is no, a word counter 37 is incremented. If the determination is yes, a correct synchronizing word counter 36 is incremented, which in turn increments the word counter 37. Thus the word counter 37 is incremented each time a correct or incorrect synchronizing word appears or is detected.

The count output of the block 37 is applied to a decision block 38 which determines when five synchronizing words (including the initial synchronizing word) have been received. As long as less than five synchronizing words (including correct and incorrect) have been received, the decision block 38 keeps the block 34 waiting for synchronizing and message words. When five synchronizing words (including correct and incorrect) have been received, a block 39 opens the output gate 18. A decision block 40 determines whether three of these five words are correct. If not, the arrangement is restarted to look for an initial synchronizing word on a bit by bit comparison. If three words are correct, an in-synchronization signal is sent by the block 41 to the output gate 18 of FIGURE 2. If the decision block 42 indicates the gate 18 is open, the in-synchronization signal is applied to a block 43 to decode the message words. After this decoding, the circuit is restarted to look for another message.

Summary

It will thus be seen that we have provided an improved word synchronizing circuit which operates to provide word synchronization in response to a first good synchronizing word detection, followed by two additional

good synchronizing word detections during the next four synchronizing word positions. And while we contemplate that the synchronizing words are equally spaced in time, this may not be necessary in some applications. With our synchronizing arrangement operating with the data message of FIGURE 1, we have found that with a bit error rate of 0.05, our synchronizing arrangement produces a correct in-synchronization output signal for 69.2% of the time, and with an error or false indication of an in-synchronization condition only once every 39.8 hours.

While the arrangement shown in the FIGURES and described is our preferred embodiment, persons skilled in the art will appreciate that modifications may be made. Therefore, while our invention has been described with reference to a particular embodiment, it is to be understood that modifications, particularly in terms of circuit implementation, may be made without departing from the spirit of the invention or from the scope of the claims.



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CLAIMS

1. A system for achieving synchronisation with a digital data message having a synchronisation word transmitted a plurality of times during the message, wherein each received synchronisation word is
5 compared with a stored synchronisation word to produce a first signal whenever the received word corresponds to the stored word, and wherein an in-synchronisation signal is produced only when one of the first signals is followed by at least two more
10 of the first signals during any sequence of any of the next four comparisons of the received synchronisation words with the stored word.
2. A system according to claim 1 wherein said transmitted synchronising words are spaced at uniform
15 intervals during said message, and wherein said next four comparisons are made at said uniform intervals.
3. A system according to claim 1 wherein said transmitted synchronising words are spaced
20 at predetermined intervals during said message, and wherein said next four comparisons are made at said predetermined intervals.
4. Synchronisation apparatus for use in a communication system having a receiver for receiving
25 digital messages from a transmitter, the apparatus comprising: means responsive to the received messages for deriving digital messages in which each message has a plurality of synchronisation words at locations spaced at predetermined
30 intervals, means for producing a synchronisation signal for each derived synchronisation word having a predetermined sequence of digital values, means for counting the word locations and the synchronisation signals, and means for producing an in-synchronisation
35 output signal only when at least two synchronisation



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signals are counted in any of the next four word locations following production of a first synchronisation signal during the message.

5. The synchronising apparatus of claim 4
5 wherein said digital message has a plurality of identical synchronising words occurring at locations therein which are spaced at predetermined equal intervals.

6. A method for detecting a digital synchron-
10 ising word comprised of a sequence of digital signals having a predetermined characteristic and appearing at a plurality of spaced predetermined times in a digital message, said method comprising the steps of:

- 15 a. comparing said sequence of digital signals with a stored digital word and producing a first detected word signal in response to the first sequence of digital signals in a message being the
20 same as said stored digital word;
- b. comparing said sequence of digital signals with said stored digital word at said predetermined times subsequent to said first detected word signal being produced, and
25 producing a second detected word signal in response to each sequence of digital signals at subsequent predetermined times being the same as said stored digital word;
- 30 c. counting said second detected word signals subsequent to said first detected word signal;
- 35 d. and producing an in-synchronisation signal in response to production of at least two detected word signals during any sequence



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of any of said next four subsequent
predetermined times.

7. A method according to claim 6 and, in the absence of at least two detected word signals during said next four subsequent predetermined times, comparing said sequence of digital signals with said stored digital word until said first detected word signal is produced.
8. A method according to claim 6 and, in the absence of two second detected word signals during said four subsequent predetermined times, further comprising the step of resetting the count of detected word signals to zero, and comparing said sequence of digital signals with said stored digital word until said first detected word signal is produced.
9. A system for achieving synchronisation with a data message having serial bits forming a synchronisation word transmitted a plurality of times during the message, the system comprising: means for comparing received serial bits with a stored synchronising word and producing an initial signal in response to an initial comparison in which a series of bits correspond to the stored synchronising word, and producing a good word signal in response to each subsequent comparison in which each series of bits correspond to the stored synchronising word; and means for producing an in-synchronisation signal only when at least two good word signals are produced during any sequence of any of the next four subsequent comparisons following production of the initial signal.
10. A system according to claim 9 wherein said initial comparison is made each time a new bit is received.



11. A system according to claim 9 wherein each of said subsequent comparisons is made in response to a synchronising word position indication.
- 5 12. A system according to claim 10 wherein each of said subsequent comparisons is made in response to a synchronising word position indication.
13. A system according to claim 9 and comprising means to restart said initial comparison following said next four subsequent comparisons.
- 10 14. A system according to claim 10 and comprising means to restart said initial comparison following said next four subsequent comparisons.
- 15 15. A system according to claim 11 and comprising means to restart said initial comparison following said next four subsequent comparisons.
16. A system according to claim 12 and comprising means to restart said initial comparison following said next four subsequent comparisons.
- 20 17. A method for detecting a digital synchronising word comprised of a sequence of digital signals having a predetermined characteristic and appearing at a plurality of spaced predetermined times in a digital message, said method comprising the steps of:
- 25 a. initially comparing said sequence of digital signals each time a new signal occurs in said sequence with a stored digital word and producing an initial signal in response to the first sequence of digital
- 30 signals in a message being the same as said stored digital word;
- 35 b. subsequently comparing said sequence of digital signals on a time position basis with said stored digital word at said predetermined times subsequent to said



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initial signal being produced, and producing
a second signal in response to each sequence
of digital signals at subsequent predeter-
mined times being the same as said stored
digital word;

5 c. counting said second signals subsequent
to said initial signal;

d. producing an in-synchronisation signal
in response to production of at least two
10 of said second signals during any sequence
of any of said next four subsequent
predetermined times;

e. and starting said initial comparison
following said four predetermined times.

15 18. A method for reliably establishing word
framing or synchronisation in a digital communication
system where a predetermined synchronisation word
is repeated at known time-spaced intervals during
a digital message transmission, said method
20 comprising the steps of:

establishing tentative word framing by
first detecting an occurrence of said synchronisation
word;

25 attempting to detect the expected presence of
said synchronisation word at a plurality of the next
succeeding of said known time-spaced intervals based
on said established tentative word framing; and

determining whether at least any two of the
next four expected synchronisation words are success-
30 fully detected and establishing the existence of a
reliable confirmed word framing condition after said
first detected occurrence if at least any two of the
next four expected synchronisation words are success-
fully detected.

35 19. A method for generating a reliable word



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- synchronisation signal in a received string of digital signals expected to include a predetermined synchronisation word in each of predetermined sync-word time slots, said method comprising the steps
- 5 of:
- searching for the first detectable occurrence of said synchronisation word in said received string of digital signals and establishing tentative word frame timing based thereon;
- 10 generating said word synchronisation signal if any two or more of the four next expected synchronisation words are successfully detected using said tentative word frame timing; and
- returning to said searching step if less
- 15 than any two of said four next expected synchronisation words are successfully detected using said tentative word frame timing.
20. A method as in claim 19 wherein said searching step includes the step of establishing bit
- 20 synchronisation.
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