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METHOD OF MANUFACTURING SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE

Background of the Invention

The present invention relates to a method of manufacturing a semiconductor integrated circuit device (hereinbelow, termed "Bi-MOS IC") in which bipolar transistors and metal-insulator-semiconductor field effect transistors (hereinbelow, termed "MOS FETs") are formed within the same semiconductor body.

There have heretofore been developed various processes by which bipolar transistors and n-channel MOS FETs (n-MOS FETs) or complementary MOS FETs (c-MOS FETs) are caused to coexist within a single semiconductor body. An example of conventional processes is as described below.

(1) An n^+-type buried layer is formed in a part of the major surface of a p-type silicon (Si) substrate. Further, an n-type Si layer is epitaxially grown on the p-type Si substrate.

(2) Boron (B) is diffused from parts of the surface of the n-type epitaxial layer so as to form p-type diffused layers for isolation reaching the p-type substrate, thereby to form several electrically-isolated island regions within the n-type Si layer.

(3) In another part of the n-type epitaxial layer, a deep p-type region (usually called "p-type well") is formed by similar boron diffusion from the surface of the epitaxial layer.

(4) An n-channel MOS FET is formed in the p-type well region. On the other hand, a p-channel MOS FET and a bipolar transistor are formed in the other island regions within the n-type Si layer.

The above process is disclosed in the official gazette of Japanese Laid-open Patent Application No.54-131887.

Such process is directed toward a Bi-MOS IC in which the thickness of the epitaxial n-type silicon layer is approximately 10 μm or greater (the depth of an emitter is approximately 5 μm). Recently, ICs have been made finer in order to enhance the operating speeds of elements or to reduce the chip area. In this regard, when the thickness of an epitaxial Si layer becomes as small as below 5 μm, the foregoing process brings about the problem that the base-collector breakdown voltage of the bipolar n-p-n transistor becomes smaller.

More specifically, the p-type well for forming the n-channel MOS FET must be rendered deep to some extent (approximately as deep as the epitaxial layer) in order to ensure the source-drain breakdown voltage of the n-channel MOS FET to be formed in the major surface

of the well. On the other hand, since the surface impurity density of the p-type well determines the V_{th} (threshold voltage) of the MOS FET, the diffusion of an impurity at a high density is undesirable. In forming the p-type well, therefore, the diffusion treatment needs to be performed at a low density ($C_s \fallingdotseq 1 \times 10^{16}$ cm^{-3}) as well as a high temperature (1200 ^{o}C) and for a long time of 4-6 hours. During the heat treatment, an n-type impurity (such as Sb or P) diffuses from the n^+-type buried layer located just under the base layer of the bipolar transistor, upwardly into the epitaxial layer as high as about 3.5 μm and reaches the vicinity of the base layer of the n-p-n transistor. In consequence, the collector-base breakdown voltage is made lower.

Therefore, when the upward extension of the n^+-type buried layer is taken into account, the thickness of the epitaxial layer is limited to 7 μm as the minimum value. It has been difficult to make the Bi-MOS IC finer by forming it with a smaller thickness and to enhance the operating speed of the bipolar transistor.

A technique similar to the present invention is disclosed in the official gazette of Japanese Laid-open Patent Application No. 57-75453. The disclosed process, however, must introduce impurities from the surface of a semiconductor body by separate steps in order to

form an isolation region and a p-type well region and has the disadvantage of a larger number of steps.

Therefore the present invention provides a method of manufacturing a semiconductor integrated circuit device comprising:

(1) the step of introducing an impurity of a first conductivity type into a plurality of parts of one major surface of a substrate containing a first conductivity type impurity, to form a plurality of impurity-doped regions which have an impurity density higher than that of said substrate;

(2) the step of forming an epitaxial semiconductor layer containing an impurity of a second conductivity type, on the major surface of said substrate;

(3) the step of introducing a first conductivity type impurity simultaneously into those parts of the surface of said epitaxial semiconductor layer which overlie said plurality of impurity-doped regions;

(4) the step of diffusing the first conductivity type impurity of said plurality of impurity-doped regions into said epitaxial semiconductor layer by heat treatment, and subjecting to drive-in diffusion the first conductivity type impurity introduced in the major surface of said epitaxial semiconductor layer, to connect together the diffused layers formed by the respective diffusions and to form a PN junction isolation portion and a semiconductor region for forming a MOS FET;

(5) the step of selectively forming a thick oxide film on a major surface of said epitaxial semiconductor layer which overlies said impurity-doped region for the PN junction isolation portion;

(6) the step of forming the MOS FET in said semiconductor region; and

(7) the step of forming a bipolar transistor in another part of said epitaxial semiconductor layer.

An embodiment of the invention will now be described in detail, by way of example, with reference to the accompanying drawings, in which:

Figures 1 to 10 are sectional flow diagrams which show Bi-CMOS IC process according to the present invention; and

Figure 11 is an impurity density curve diagram of an n-channel MOS FET in a Bi-CMOS IC mode according to the present invention.

Figures 1 to 10 are sectional flow diagrams corresponding to the following respective steps of a process for a fine Bi-CMOS IC wherein the thickness of an epitaxial layer is as small as 1.5 - 3 μm and wherein an isolation portion is formed of an oxide film and a diffused layer.

(1) As shown in Figure 1, a p^--type Si crystal substrate 100 of high resistivity is prepared, and an oxide film (SiO_2 film) 200 formed by oxidizing the surface thereof is photoetched and Sb (antimony) or the like is deposited and diffused, thereby to form an n^+-type buried layer 300.

This n^+-type buried layer 300 is formed as a part of the collector of a bipolar n-p-n transistor.

(2) An oxide film 400 is formed on the whole surface again. As shown in Figure 2, it is photoetched to open parts for forming an isolation portion and a well, whereupon B (boron) is deposited (or ion-implanted) and diffused to form p^+-type buried layers 500 and 600.

(3) As shown in Figure 3, Si is epitaxially grown on the whole surface so as to form an n-type Si layer 700 which is approximately 3 μm thick. The surface of the n-type Si layer 700 is oxidized to form an oxide film 800.

(4) As shown in Figure 4, parts of the oxide film 800 are photoetched and opened in correspondence with the p-type buried layers 500 and 600, whereupon B (boron) is deposited (or ion-implanted). In this case, the impurity is introduced in such a quantity that the surface impurity density of the p-type well will be optimised.

(5) In the epitaxial n-type Si layer 700, the B (boron) is diffused from the upper and lower parts thereof, to form the p-type isolation portion 900 and p-type well 1000 as shown in Figure 5.

(6) The oxide film 800 is etched and removed. Nitride (Si_3N_4) is deposited on an oxide film 1100 formed anew, and is selectively photoetched to form a nitride film 1200. Using the nitride film 1200 as a mask, the surface of the n-type Si layer is locally oxidized to form a thick field oxide film 1300 (1300a, 1300b, 1300c) as shown in

Figure 6. The field oxide film 1300 intrudes below the surface of the n-type Si layer 700 to a depth of about 1 μm, and one part thereof 1300a lies in contact with the upper surface of the p-type isolation portion 900 so as to form an isolation portion composed of the two 1300a and 900. Another part 1300b of the field oxide film 1300 is formed in a position where it lies in contact with the peripheral part of the p-type well, and it serves as an isolation portion between the n-type layer and p-type well. Still another part 1300c serves as an isolation portion between the collector and base in the surface of the bipolar portion formed in the n^+-type buried layer.

(7) As shown in Figure 7, an SiO_2 film 1400 is formed by chemical vapour deposition (hereinbelow, termed "CVD"), and a part thereof is opened by photoetching. Using the CVD oxide film 1400 and the field oxide film 1300a, 1300c as a mask, boron is deposited on and diffused into a part of the n-type layer 700 of the bipolar portion, whereby the p-type base 1500 of the n-p-n transistor is formed in self-alignment fashion. The depth of the base in this case is rendered approximately 0.7 μm.

(8) After the oxide film 1400 formed by the CVD and a thin oxide film on the surface of the Si layer have been etched and removed, a gate oxide film 1600 is formed by thermal oxidation, and Si is deposited thereon from a vapour phase so as to form a polycrystalline Si layer. Photoetching is subsequently performed to leave polycrystalline Si gates

1700 on the MOS FET side as shown in Figure 8. A mask made of an oxide film 1800 is reformed. Using the field oxide film 1300a, 1300b and polycrystalline Si gate 1700 as a mask, boron (B) is deposited (or ion-implanted) and diffused, whereby the source and drain 1900 of the p-channel MOS FET are formed in self-alignment fashion. The depth of the p^+-type source in this case is rendered 0.4 - 0.5 μm.

(9) The oxide film 1800 is removed. An oxide film 2000 is formed anew by CVD, and is photoetched to open parts thereof as shown in Figure 9. Arsenic (As) is deposited (or ion-implanted) and then diffused, thereby to form the n^+-type source and drain 2100 of the n-channel MOS FET in the surface of the p-type well 1000 and also to form the n^+-type emitter 2200 and n^+-type collector (contact portion 2300 of the n-p-n transistor. The depth of the emitter in this case is rendered approximately 0.4 μm. The collector may well be rendered so deep as to reach the n^+-type buried layer 300 by another step.

(10) The oxide film 2000 is removed, and an insulating film 2400 of PSG (phosphosilicate glass) or the like is formed on the whole surface. After photoetching the PSG film to form contact holes, Al (aluminum) is evaporated, and the Al is photoetched. Thus, electrodes 2500 ohmically connected to the respective semiconductor regions are completed as shown in Figure 10. Although not shown in the figure, gate Al electrodes are led out via through holes provided in the PSG film in the extensions of the

polycrystalline Si gates.

Figure 11 shows an impurity density profile in the section of a part of the n-channel MOS FET (section B - B' in Figure 19) manufactured by the foregoing process.

In the embodiment described described above, the p-type well is formed in a shape in which it is directly coupled with the p^--type substrate. In the upward and downward diffusions for forming the well, therefore, the density of the diffusion from the lower portion (the p-type buried layer) can be rendered higher than that from the upper portion, and the downward diffusion rate can be increased in the state in which the upper layer to form the MOS FET therein is held at a low density. Thus, the period of time of the heat treatment for forming the well region is shortened to about ½ of that in the prior-art method, and the "upward extension" of the n^+ buried layer on the bipolar side can be suppressed to about ½ of that in the prior-art method.

Accordingly, even when the epitaxial layer is as thin as 1.5 μm - 3.0 μm, the low-density epitaxial layer 0.7 μm - 1.3 μm thick remains even after the upward extension of the n^+-type buried layer, so that the characteristics of the n-p-n transistor do not degrade.

Since the n^+ buried layer is not formed in the MOS FET forming region, the heat treatment is not attended with the diffusion of an impurity into the epitaxial layer, so that the source-drain breakdown voltage does not degrade.

Also, the impurity is introduced into the major surfaces of the isolation forming region and the p-type well forming region at the density at which the p-type well comes to have the optimum impurity density, and the heat treatment is conducted to form the p-type well and the isolation region. The thick oxide film is thereafter formed on the isolation region so as to prevent the appearance of a parasitic channel ascribable to the inversion of the p^--type substrate. This thick oxide film serves also as a mask for the diffusion of the base of the n-p-n transistor.

In this manner, the steps are made common to prevent the increase of the number of steps. The thick oxide film also has the advantage that the junction capacitance is small, so the operating speed of the transistor is not degraded.

In addition, since the diffusion of the p-type well and that of the isolation p-type layer are simultaneously performed from below, the process is shortened, and the lateral spread of the portions can be suppressed.

The formation of the field oxide film requires a heat treatment at a temperature of about 100 °C for about 7 hours in case of the normal pressure. Since, however, this temperature is low in comparison with 1200 °C which is the temperature of the diffusion of the p-type well, the heat treatment little affects the upward extension of the n^+-type buried layer.

As explained above, according to the present inven-

tion, a thin fast-operating bipolar transistor having an epitaxial layer whose thickness is 5 μm or less is permitted to coexist with a MOS FET, and the area of the element can be reduced, whereby a Bi-MOS IC of high operating speed and large capacity can be provided. The present invention is applicable at least to the general processes of Bi-CMOS ICs and Bi-n-channel MOS ICs, and it is effective especially when applied to devices aiming at a higher operating speed and a high density of integration, for example, a gate array of at least 1 k gates.

CLAIMS:

1. A method of manufacturing a semiconductor integrated circuit device comprising:

(1) the step of introducing an impurity of a first conductivity type into a plurality of parts of one major surface of a substrate containing a first conductivity type impurity, to form a plurality of impurity-doped regions which have an impurity density higher than that of said substrate;

(2) the step of forming an epitaxial semiconductor layer containing an impurity of a second conductivity type, on the major surface of said substrate;

(3) the step of introducing a first conductivity type impurity simultaneously into those parts of the surface of said epitaxial semiconductor layer which overlie said plurality of impurity-doped regions;

(4) the step of diffusing the first conductivity type impurity of said plurality of impurity-doped regions into said epitaxial semiconductor layer by heat treatment, and subjecting to drive-in diffusion the first conductivity type impurity introduced in the major surface of said epitaxial semiconductor layer, to connect together the diffused layers formed by the respective diffusions and to form a PN junction isolation portion and a semiconductor region for forming a MOS FET;

(5) the step of selectively forming a thick oxide film on a major surface of said epitaxial semiconductor

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layer which overlies said impurity-doped region for the PN junction isolation portion;

(6) the step of forming the MOS FET in said semiconductor region; and

(7) the step of forming a bipolar transistor in another part of said epitaxial semiconductor layer.

2. A method of manufacturing a semiconductor integrated circuit device according to Claim 1, comprising the step of introducing a first conductivity type impurity into a selected part of the major surface of said epitaxial semiconductor layer by using as a mask said thick oxide film formed on said major surface of said isolation region, to form a base of the bipolar transistor.

3. A method of manufacturing a semiconductor integrated circuit device according to Claim 2, comprising the step of introducing a second conductivity type impurity into said base of said bipolar transistor, to form an emitter thereof, and introducing said second conductivity type impurity also into the first conductivity type semiconductor regions, to form a source and a drain of said MOS FET.

4. A method of manufacturing a semiconductor integrated circuit device, substantially as any described herein with reference to the accompanying drawings.

5. A semiconductor integrated circuit device made using a method according to any one of the preceding claims.