CLAIMS

1. A device, comprising:

a plurality of fin field-effect transistors disposed in rows;

a plurality of insulating fins each disposed between the rows; and

a plurality of memory elements each coupled to a terminal of a fin field-effect transistor among the plurality of fin field-effect transistors.

2. The device of claim 1, wherein the plurality of insulating fins at least partially define furrows in which gates of each of the plurality of fin-field effect transistors are disposed.

3. The device of claim 2, wherein at least a portion of the insulating fins is disposed under the gates.

4. The device of claim 1, wherein each of the fin field-effect transistors among the plurality of fin field-effect transistors comprises a generally U-shaped distal portion.

5. The device of claim 1, wherein the plurality of fin field-effect transistors comprises a plurality of dual-gate fin field-effect transistors.

6. A device, comprising:

a plurality of rows of transistors, each transistor comprising:

a semiconductor fin; and

a gate, at least part of which is disposed adjacent the semiconductor fin; and

a plurality of insulating fins each disposed between a pair of rows of transistors among the plurality of rows of transistors.

7. The device of claim 6, wherein each insulating fin among the plurality of insulating fins comprises a base, and wherein the base is disposed at least partially under at least one of gates.

8. The device of claim 6, wherein the insulating fins extend along at least a substantial portion of a length of the rows of transistors.

9. The device of claim 6, wherein each insulating fin among the plurality of insulating fins comprises a liner disposed between the insulating fin and a substrate.

10. The device of claim 6, wherein each row of transistors among the plurality of rows of transistors comprises a pair of gates disposed on opposite sides of the row of transistors.

11. The device of claim 6, wherein the insulating fins are each less than 1 F wide.

12. A device, comprising:

a first transistor and a second transistor each comprising:

a semiconductor fin extending generally perpendicularly from a substrate and generally linearly in a direction parallel to the substrate; and

a pair of gates formed on either side of the semiconductor fin and extending generally parallel to the semiconductor fin; and

an insulating fin disposed between the first transistor and the second transistor and extending generally parallel to the semiconductor fin of each of the first and second transistors.

13. The device of claim 12, wherein the insulating fin, the semiconductor fin of the first transistor, and the semiconductor fin of the second transistor define a pair of furrows on either side of the insulating fin, wherein a gate among the pair of gates of the first transistor is disposed in a furrow among the pair of furrows and a gate among

the pair of gates of the second transistor is disposed in the other furrow among the pair of furrows.

14. The device of claim 12, wherein the semiconductor fins each comprises a pair of legs separated by a trench.

15. The device of claim 12, comprising a liner disposed at least partially under the insulating fin.

16. The device of claim 12, wherein the first transistor and the second transistor each comprises an upper doped region and a lower doped region, wherein the upper doped region is doped different from the lower doped region.

17. A method, comprising:

forming a precursor fin on a substrate;

forming a liner film on the substrate;

at least partially filling a void adjacent the precursor fin with an inter-gate dielectric;

removing at least a portion of the liner film;

removing a portion of the inter-gate dielectric exposed by removing the portion of the liner film;

forming a furrow in the substrate, wherein the furrow is disposed between a semiconductor fin formed from the substrate and an insulating fin formed from the inter-gate dielectric.

18. The method of claim 17, wherein the precursor fin, the inter-gate dielectric, and the furrow are narrower than the photolithographic-resolution limit.

19. The method of claim 17, comprising undercutting the precursor fin with a wet etch.

20. The method of claim 17, wherein the forming the liner film comprises forming a shoulder of liner film on either side of the precursor fin.

21. The method of claim 17, comprising forming isolation trenches in the substrate prior to forming the precursor fin, wherein the isolation trenches extend generally perpendicular to the precursor fin.

22. The method of claim 21, comprising forming shallow trenches in the substrate prior to forming the precursor fin, wherein the shallow trenches are shallower than the isolation trenches.

CLAIMS

1. A device, comprising:

fin field-effect transistors disposed in rows, wherein each of the fin field-effect transistors comprises a semiconductor fin comprising a generally U-shaped distal portion with two legs comprising a source and a drain of each of the fin field-effect transistors, wherein the two legs define a gap therebetween, wherein the two legs and the gap are aligned such that a drive current generated between the source and the drain flows in a direction parallel to alignment of the rows;

an insulator disposed solely in the gap of the semiconductor fin of each of the fin field-effect transistors; and

insulating fins each disposed in a second gap defined between the fin field-effect transistors disposed in the rows.

2. A device, comprising:

fin field-effect transistors disposed in rows, wherein each of the fin field-effect transistors comprises a semiconductor fin comprising a generally U-shaped distal portion with two legs comprising a source and a drain of each of the fin field-effect transistors, wherein the two legs define a gap therebetween;

an insulator disposed solely in the gap of the semiconductor fin of each of the fin field-effect transistors; and

insulating fins each disposed in a second gap defined between the fin field-effect transistors disposed in the rows, wherein the insulating fins at least partially define furrows in which gates of each of the fin-field effect transistors are disposed.

3. The device of claim 2, wherein at least a portion of the insulating fins is disposed under the gates.

4. The device of claim 2, wherein each row comprises at least two of the fin field-effect transistors.

5. The device of claim 2, wherein the fin field-effect transistors comprise dual-gate fin field-effect transistors.

6. A device, comprising:

a plurality of rows of transistors, each transistor comprising:

a semiconductor fin, comprising a generally U-shaped distal portion with two legs comprising a source and a drain, wherein the two legs define a gap therebetween, wherein the two legs and the gap are aligned such that a drive current generated between the source and the drain flows in a direction parallel to alignment of the rows; and

a gate, at least part of which is disposed adjacent the semiconductor fin;

an insulator disposed solely in the gap of the semiconductor fin of each transistor; and

insulating fins each disposed in a second gap defined between each transistor of a pair of rows of transistors among the plurality of rows of transistors.

7. A device, comprising:

a plurality of rows of transistors, each transistor comprising:

a semiconductor fin, comprising a generally U-shaped distal portion with two legs comprising a source and a drain, wherein the two legs define a gap therebetween; and

a gate, at least part of which is disposed adjacent the semiconductor fin;

an insulator disposed solely in the gap of the semiconductor fin of each transistor; and

insulating fins each disposed in a second gap defined between each transistor of a pair of rows of transistors among the plurality of rows of transistors, wherein the insulating fins are disposed at a height greater than a height of the semiconductor fin.

8. The device of claim 7, wherein each insulating fin among the insulating fins comprises a base, and wherein the base is disposed at least partially under at least one of gates.

9. The device of claim 7, wherein the insulating fins extend along at least a substantial portion of a length of the plurality of rows of transistors.

10. The device of claim 7, wherein each insulating fin among the insulating fins comprises a liner disposed between itself and a substrate.

11. The device of claim 7, wherein each row of transistors among the plurality of rows of transistors comprises a pair of gates disposed on opposite sides of the row of transistors.

12. A device, comprising:

a first transistor of a first row of transistors and a second transistor of a second row of transistors each of the first and second transistors comprising:

a semiconductor fin having a width and having a length greater than the width and having a height extending generally perpendicularly from a substrate; and

a pair of gates formed on either side of the semiconductor fin and extending generally parallel to the semiconductor fin;

an insulator disposed solely in a gap defined by a source and a drain of the semiconductor fin of each of the first transistor and the second transistor, wherein the source, the drain, and the gap are aligned such that a drive current generated between the source and the drain flows in a direction parallel to alignment of the first row and the second row; and

an insulating fin disposed in a second gap defined between the first transistor and the second transistor and extending generally parallel to the semiconductor fin of each of the first and second transistors.

13. A device, comprising:

a first transistor of a first row of transistors and a second transistor of a second row of transistors each of the first and second transistors comprising:

a semiconductor fin having a width and having a length greater than the width and having a height extending generally perpendicularly from a substrate; and

a pair of gates formed on either side of the semiconductor fin and extending generally parallel to the semiconductor fin;

an insulator disposed solely in a gap defined by a source and a drain of the semiconductor fin of each of the first transistor and the second transistor; and

an insulating fin disposed in a second gap defined between the first transistor and the second transistor and extending generally parallel to the semiconductor fin of each of the first and second transistors, wherein the insulating fin, the semiconductor fin of the first transistor, and the semiconductor fin of the second transistor define a pair of furrows on either side of the insulating fin, wherein a gate among the pair of gates of the first transistor is disposed in a furrow among the pair of furrows and a gate among the pair of gates of the second transistor is disposed in the other furrow among the pair of furrows.

14. The device of claim 13, wherein the semiconductor fin comprises a pair of legs separated by a trench as the source and the drain.

15. The device of claim 13, comprising a liner disposed at least partially under the insulating fin.

16. The device of claim 13, wherein the first transistor and the second transistor each comprises

an upper doped region and a lower doped region, wherein the upper doped region is doped different from the lower doped region.

17. A device, comprising:

a semiconductor fin having a width and having a length greater than the width and having a height extending generally perpendicularly from a substrate, wherein the semiconductor fin comprises a source and a drain of a transistor;

an insulator disposed solely in a gap defined by the source and the drain of the transistor;

a gate comprising a first side formed on a first side of the semiconductor fin and extending generally parallel to the semiconductor fin; and

an insulating fin directly contacting a second side of the gate opposite the first side of the gate, wherein the insulating fin and the second side of the gate extend generally parallel to the semiconductor fin, and a liner disposed at least partially under the insulating fin.

18. The device of claim 17, wherein the semiconductor fin comprises a pair of legs separated by a trench.

19. The device of claim 17, wherein the pair of legs comprises the source and the drain of the transistor.

20. The device of claim 17, comprising an upper doped region and a lower doped region of the transistor, wherein the upper doped region is doped different from the lower doped region.

21. The device of claim 17, wherein the insulating fin is disposed at a height greater than the height of the semiconductor fin.